

**TECHNICAL MANUAL**

**DIRECT SUPPORT, GENERAL SUPPORT, AND DEPOT MAINTENANCE MANUAL**

**RADIO SET**

**AN/GRC-144**

**(NSN 5820-00-926-7356)**

This copy is a reprint which includes current pages from Changes 1 through 5.

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**HEADQUARTERS, DEPARTMENT OF THE ARMY**

**AUGUST 1971**

**WARNING**

**DEATH or SERIOUS INJURY** may result from hazards in this equipment, unless the proper safety measures are observed. **READ and OBSERVE** the referenced warnings concerning the following hazards in this equipment.

115 vac (para 3-4, 3-6, 3-12, 3-25, and 3-48)

Change

No. 6

HEADQUARTERS  
DEPARTMENT OF THE ARMY  
WASHINGTON, DC, 13 MAY 1985

Direct Support, General Support and

Depot Maintenance Manual

RADIO SETS AN/GRC-144(V)1 (NSN 5820-01-048-9110)

AN/GRC-144(V)2 (NSN 5820-01-061-7029)

AN/GRC-144(V)3 (NSN 5820-01-100-3093)

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**DS, GS, AND DEPOT MAINTENANCE MANUAL**

**RADIO SET  
AN/GRC-144(V)1  
(NSN 5820-00-926-7356)**

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**5**

**SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK**

**1**

**DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL**

**2**

**IF POSSIBLE, TURN OFF THE ELECTRICAL POWER**

**3**

**IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH, OR LIFT THE PERSON TO SAFETY USING A DRY WOODEN POLE OR A DRY ROPE OR SOME OTHER INSULATING MATERIAL**

**4**

**SEND FOR HELP AS SOON AS POSSIBLE**

**5**

**AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION**

**WARNING  
HIGH VOLTAGE  
is used in this equipment  
DEATH ON CONTACT  
MAY RESULT IF SAFETY PRECAUTIONS  
ARE NOT OBSERVED  
DO NOT SERVICE OR ADJUST ALONE**

Maintenance adjustments of this equipment are made with power applied. Be careful when working near the interior of the equipment, or near the ac power distribution.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid or resuscitation, is present.

A periodic review of safety precautions in TB 385-4, safety precautions for Maintenance of Electrical/Electronic Equipment, is recommended. When the equipment is operated with covers removed, DO NOT TOUCH exposed connections or components. MAKE CERTAIN you are not grounded when making connections or adjusting components inside the test instrument.

**DON'T TAKE CHANCES!!**

Operator and maintenance personnel should also be familiar with the requirements of TB SIG 291 before attempting installation or operation of the equipment covered in this manual. Failure to follow the requirements of TB SIG 291 could result in injury or DEATH.

**WARNING**

**Fumes of TRICHLOROTRIFLUOROETHANE are poisonous. Provide adequate ventilation whenever you use TRICHLOROTRIFLUOROETHANE. Do not use solvent near heat or open flame. TRICHLOROTRIFLUOROETHANE will not burn, but heat changes the gas into poisonous, irritating fumes. DO NOT breathe the fumes or vapors. TRICHLOROTRIFLUOROETHANE dissolves natural skin oils. DO NOT get the solvent on your skin, use gloves, sleeves and an apron which the solvent cannot penetrate. If the solvent is taken internally, consult a physician immediately.**

**Change 5 b**

Direct Support, General Support and  
 Depot Maintenance Manual  
 RADIO SETS AN/GRC-144(V)1 (NSN 5820-01-048-9110)  
 AN/GRC-144(V)2 (NSN 5820-01-061-7029)  
 AN/GRC-144(V)3 (NSN 5820-01-100-3303)  
 AND AN/GRC-144(V)4 (NSN 5820-01-099-7798)

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## CHAPTER 1 INTRODUCTION

### 1-1. Scope

a. This manual contains detailed functioning of the equipment (chapter 2) and instructions covering direct support (chapter 3) and depot maintenance (chapter 4) for Radio Sets AN/GRC-144(V), DDM (digital data modem) and ADDM (asynchronous digital data modem) operating modes; AN/GRC-144(V)3, HI-CAP LOS (high capacity line-of-sight) and AN/GRC-144(V)4, SRWBR (short range wideband radio) configurations. It includes instructions for periodic checks and calibration, troubleshooting; testing, aligning and repairing the equipment. It also lists tools materials, and test equipment to perform the maintenance of the equipment.

b. The complete manual for this equipment includes TM 11-5820-695-12, Operator and Organizational Maintenance Manual Including Repair Parts and Special Tools Lists for Radio Sets AN/GRC-144(V), AN/GRC-144(V)3 and AN/GRC-144(V)4.

### 1-2. Consolidated Index of Army Publications and Blank Forms

Refer to the latest issue of DA Pam 310-1 to determine whether there are any new editions, changes or additional publications pertaining to the equipment.

### 1-3. Reporting Errors and Recommending Improvements

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter or DA Form 2028 (Recommended Changes to Publications and Blank Forms) direct to: Commander, US Army Communications Electronics Command and Fort Monmouth, ATTN: AMSEL-ME-MP, Fort Monmouth, New Jersey 07703 -5007. In either case, a reply will be furnished direct to you.

### 1-4. Maintenance Forms, Records, and Reports

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by DA Pam 738-750 as contained in the Maintenance Management Update.

b. Report of Packaging and Handling Deficiencies. Fill out and forward SF 364 (Report of Discrepancy (ROD)) as prescribed in AR 735-11-2/DLAR 4140.55/NAVMATINST 4355.73A/AFR 400-54/MCO 4430.3F.

c. Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33C/AFR 75-18/MCO P4610.19D/DLAR 4500.15.

### 1-5. Reporting Equipment Improvement Recommendations (EIR)

If your Radio Set AN/GRC-144(V) needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design. Put it on an SF 368 (Quality Deficiency Report). Mail it to Commander, US Army Communications Electronics Command and Fort Monmouth, ATTN: AMSEL -ME-MP, Fort Monmouth, New Jersey 07703-5007. We'll send you a reply.

### 1-6. Administrative Storage

Administrative Storage of equipment issued to and used by Army activities will have preventive maintenance performed in accordance with the PMCS Charts before storing. When removing the equipment from administrative storage the PMCS should be performed to assure operational readiness. Disassembly and

repacking of equipment for shipment or limited storage is covered in paragraphs 6-1 and 6-2.

#### 1-7. Destruction of Army Electronics Materiel

Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

#### NOTES

Radio Set AN/GRC-144 has been renomenclatured as AN/GRC-144(V) with variations as follows:

- AN/GRC-144(V)1 48 channel synchronous operation Digital Data Modem (DDM) with MK-1835/GRC-144(V) installed.
- AN/GRC-144(V)2 48/96 channel asynchronous operation Digital Data Modem (ADDM) with MK-1836/GRC-144(V) installed.

AN/GRC-144(V)3 HI-CAP LOS (high capacity line-of-sight) consisting of Radio Set Transmitter T-1054(P)/GRC-144(V) equipped with Digital Data Combiner OB-93/GRC-144(V) and Radio Set Receiver R-1467(P)/GRC-144(V). AN/GRC-144(V)4-HI-

CAP LOS/SRWBR (shortrange wideband radio) consisting of Radio Set Transmitter T-1054(P)/GRC-144(V) equipped with Digital Data Combiner 08-93/GRC-144(V) and Radio Set Receiver R-1467(P)/GRC-144(V) equipped with Converter Multiplier Assembly CV-3633/GRC-144(V).

Radio Set Transmitter T-1054(GC-144 is now nomenclatured T-1054(P)/GRC-144(V) and Receiver R-1467/GRC-144 is now nomenclatured R-1467(P)/GRC-144(V) for (V)1 and (V)2 configurations.

Equipment delivered under contract DAAB-5-72-C05507 differs slightly from those delivered under contracts DAAB05-68-C-0027, DA28-043-AMC -02614(E), and DA36-039-AMC-03282.

\*References to the AN/GRC-144(V)1 and AN/GRC-144(V)2 configurations are shown throughout this manual as AN/GRC-144 or AN/GRC-144(V). Radio Set AN/GRC-144(V)1 and AN/GRC-144(V)2 Transmitter and Receiver designations throughout this manual will appear as either T-1054/GRC-144 or T-1054(P)/GRC-144(V) and R-1467/GRC-144 or R-1467(P)/GRC-144(V) respectively.

## CHAPTER 2

## FUNCTIONING OF EQUIPMENT

## Section I. FUNCTIONS OF RADIO SETS AN/GRC-144(V), AN/GRC-144(V)3 and AN/GRC-144(V)4

## 2-1. General

This section describes the major functions of Radio Sets AN/GRC-144(V), AN/GRC-144(V)3 and AN/GRC-144(V)4 configurations at the block diagram level. The basic Radio Set AN/GRC-144(V) consists of two equipment cabinets: Transmitter, Radio T-1054(P)/GRC-144(V) and Receiver, Radio R-1467(P)/GRC-144(V). Radio Sets AN/GRC-144(V)3 and AN/GRC-144(V)4 are AN/GRC-144(V) Radio Sets modified to high capacity line-of-sight and short range wide band radio (SRWBR) configurations respectively, by making wiring modifications and adding new upgraded or modified modules to AN/GRC-144(V) Radio Sets. The AN/GRC-144(V)3 Radio Set configuration also consists of two equipment cabinets: Transmitter, Radio T-1054(P)/GRC-144(V) and Receiver, Radio R-1467(P)/GRC-144(V). The AN/GRC-144(V)4 Radio Set configuration consists of the identical equipment cabinets used with (V)3 configuration with the addition of Converter Multiplier Assembly CV-3633/GRC-144(V). This section describes the major functions of Radio Sets AN/GRC-144(V), AN/GRC-144(V)3 and AN/GRC-144(V)4 at a block diagram level and the major signal paths and significant controls within Transmitters, Radio T-1054(P)/GRC-144(V) and T-1054(P)/GRC-144(V), Receivers, Radio R-1467(P)/GRC-144(V) and R-1467(P)/GRC-144(V) and Converter-Multiplier Assembly CV-3633/GRC-144(V). Also, covered in this section are explanations of the operating relationships between functional elements of AN/GRC-144(V) Radio Sets. Paragraphs 2-2, 2-2.1 and 2-2.2 contain block diagram descriptions of Radio Sets AN/GRC-144(V), AN/GRC-144(V)3 and AN/GRC-144(V)4 respectively.

## 2-2. Block Diagram Descriptions of Radio Set AN/GRC-144(V)

a. Standard Cable Terminal Configuration (fig. 5-2). In the standard cable terminal configuration, the AN/GRC-144(V) is the radio link between the cable system and the antenna system and also provides internal pcm processing for the digital interface between cable and radio. In the transmit direction, the signal is received by cable (FROM CABLE) and transmitted through the antenna (cable-to-radio). In the receive direction, the signal is received at the antenna and sent by cable (TO CABLE) to the next link in the network (radio-to cable). Pcm signals require regeneration and retiming at the interface between cable and radio. The cable terminal configuration utilizes digital data modem 1A12 in Transmitter, Radio T-1054(P)/GRC-144(V) to regenerate and retime the pcm signals. Digital data modem 1A12 is functionally divided into two parts, one part (cable-to-radio circuits) processes signals in the transmit direction, the other part (radio-to-cable circuits) processes signals in the receive direction. The cable terminal configuration uses both functional parts of digital data modem 1A12. Radio Set AN/GRC-144(V) is connected in the cable terminal configuration by making the CABLE TERMINAL MODE OF OPERATION connection at the radio patch panel in Transmitter, Radio T-1054(P)/GRC-144(V). The CABLE TERMINAL OPERATION indicator on the radio patch panel lights when this connection is completed. The transmit (cable-to-radio) and receive (radio-to-cable) signal paths through the AN/GRC-144(V) for the cable terminal configuration are described in the following subparagraphs.

(1) Transmit path. The cable system input signal consisting of pcm, orderwire, and direct current is applied to the FROM CABLE input of Transmitter, Radio T-1054(P)/GRC-144(V). The three signals are separated in the cable-to radio circuits of digital data modem 1A12. The distorted pcm signal is reshaped, retimed, and converted to a level compatible with the radio system. The orderwire signal is amplified. The direct current portion of the signal is routed back from the FROM CABLE input to the TO CABLE output through the cable-to radio and radio-to-cable circuits of digital data modem 1A12. The cable current from the input cable is looped back to the output cable so that power is provided to operate Restorer, Pulse Form TD-206 placed at 1 mile intervals in the synchronous cable transmission path or to operate Restorer, Pulse Form TD-982/U placed at 1/2 mile intervals in the asynchronous cable transmission path. The regenerated pcm output signal from the cable-to-radio

circuits is applied to the radio modulator circuits through attenuator assembly 1A3, and af-rf amplifier 1A4. The orderwire signal output (thru ow rec) from the cable-to-radio circuits is applied through the radio patch panel to orderwire assembly 1A13 where it is amplified and distributed to attenuator assembly 1A3 (to radio ow), Handset H-156/U, the remote phone, and the loudspeaker. The orderwire circuits operate on a partyline basis by interconnecting signals between the four sources (thru ow, Telephone Set TA-312/PT, Handset H-156/U, and the radio equipment. For example, a signal originating at Telephone Set TA-312/PT (remote voice send) is amplified and is distributed to Handset H-156/U, thru ow send, attenuator assembly 1A3 (to radio), and to the speaker. The to radio ow signal is applied to the radio modulator circuits through attenuator assembly 1A3 and af-rf amplifier 1A4. The pcm and orderwire signals are combined at the output of af-rf amplifier 1A4



and are applied to the modulator circuits as a combined baseband signal. The combined baseband signal frequency modulates a 1.50 MHz carrier in the modulator circuits. This signal is translated up to the 4.4 to 5.0 GHz band and is applied to the antenna through the RF OUTPUT waveguide connector on the T-1054/GRC-144, Switch, Waveguide SA-1679/GRC, Diplexer CU-1891/GRC, and associated waveguide assemblies. A portion of the rf output from the T-1054/GRC-144 can be applied to Receiver, Radio R-1467/GRC-144 through the radio test set, the TEST OUTPUT (RCVR) connector on the T-1054/GRC-144, and Coupler, Directional OU-1890/GRC. The radio test set provides a receiver test signal to check the operation of Radio Set AN/GRC-144.

(2) *Receive path.* The 4.4 to 5.0 GHz rf receive signal is coupled from the antenna to Receiver, Radio R-1467/GRC-144 through Diplexer CU-191/GRC, Coupler, Directional OU-1890/GRC, RF INPUT waveguide connector on the R-1467/GRC-144, and associated waveguide assemblies. The rf input signal is amplified and demodulated in the R-1467/GRC-144. The composite pcm and orderwire output signal is coupled to the T-1054/GRC-144 through the TRAFFIC OUTPUT connector on the R-1467/GRC-144, the TRAFFIC INPUT (RCVR) connector on the T-1054/GRC-144, and an associated interconnecting cable. The combined pcm and orderwire signal is applied to the radio-to-cable circuits of digital data modem 1A12 through orderwire assembly 1A13 and the radio patch panel. The pcm and orderwire signals are separated in the radio-to-cable circuits. The distorted pcm signal is reshaped, retimed, and reformatted for cable system compatibility. The separated orderwire signal (recovered ow) and an orderwire sensing signal (recovered ow sense) are sent back from the radio-to-cable circuits of 1A12 to 1A13 through the radio patch panel. For normal conditions, the recovered ow sense signal, generated in the radio-to-cable circuits, keeps a relay in 1A13 energized allowing the recovered ow signal to be amplified and distributed to the remote phone, Handset H-166/ U, the loud speaker, and back to 1A12 (thru ow send). The thru ow send signal is combined with the regenerated pcm signal and the cable direct current in the radio-to-cable circuits of 1A12. The combined pcm/orderwire/dc signal is applied to the cable system through the TO CABLE connector on the T-1054/GRC-144. If a pcm traffic failure is detected in the radio-to-cable circuits of 1A12, the recovered ow sense signal causes the relay in 1A13 to become deenergized. For this condition, the orderwire signal

from Receiver, Radio R-1467/GRC-144 is routed through contacts of the relay and is amplified and distributed to Telephone Set TA-312/PT, Handset H-156/U, the loudspeaker, and to 1A12 (thru ow send). Thus, orderwire communication is maintained when a pcm traffic failure occurs.

b. *Nonstandard Cable Terminal Configuration* (fig. 5-3). In the nonstandard cable terminal configuration, the AN/GRC-144 is the radio link between the cable system and the antenna system; however, this configuration utilizes external equipment to process the pcm signals at the interface between cable and Radio Set AN/GRC-144. Multiplexer TD-203/U (radio combiner) and Multiplexer TD-204/U (cable combiner) provide the interface between cable and Radio Set AN/GRC-144, by regenerating and retiming the pcm signals. Radio Set AN/GRC-144 is connected in the nonstandard cable terminal configuration by making the CABLE TERMINAL (NONSTANDARD) MODE OF OPERATION connection at the radio patch panel in Transmitter, Radio T-1054/GRC-144. This connection bypasses digital data modem 1A12. Two Multiplexer TD-204/U's with separate cable systems must be connected to Multiplexer TD-203/U for 96 channel (biternary) operation. The transmit (cable-to-radio) and receive (radio to-cable) signal paths through the external pcm processing equipment and the AN/GRC-144 are described in the following subparagraphs.

(1) *Transmit path.* The cable system input signal consisting of pcm and orderwire is applied to the FROM CABLE input of the TD-204/U (cable combiner) where the pcm and orderwire signals are separated. The pcm signal is reshaped and retimed and applied to the TD-203/U (radio combiner). The pcm signal is converted to a level compatible with Radio Set AN/GRC-144 and is coupled from the TD-203/U to attenuator assembly 1A3 in the T-1054/GRC-144 through the TO RADIO connectors and associated cable and the radio patch panel. The FROM CABLE orderwire signal is routed (send ow) to 1A13 through the PATCH THRU connector on the TD-204/U, the HANDSET connector on the T-1054/GRC-144, and the associated cable. The send voice signal is amplified in 1A13 and distributed to Telephone Set TA312/PT, thru ow send terminals, Headset Microphone H-91A/U on Multiplexer TD-204/U, and to attenuator assembly 1A3 (to radio ow).

Since the thru ow send output terminals and the thru ow rec input terminals of 1A11 are not used in this configuration, they are terminated in 620 ohms. The signal distribution within 1A13 is the same as shown in figure 5-2 for the cable terminal configuration. Also, the remainder of the transmit signal path from attenuator assembly 1A3 to the antenna is the same as that described in a(1) above for the cable terminal configuration.

(2) *Receive path.* The receive path from the antenna to the input of orderwire 1A13 is the same as described in a(2) above for the cable terminal configuration. The combined pcm and orderwire output of 1A13 is applied to the TD203/U through the radio patch panel, the FROM RADIO connectors on the T-1064/GRC-144 and the TD-203/U, and the associated cable. The distorted FROM RADIO pcm signal is separated from the orderwire signal. Then it is reshaped and retimed and applied to the TD-204/U where it is reformatted for cable system compatibility. The separated orderwire signal (recovered ow) and the orderwire sensing signal (recovered ow sense) are fed back from the TD203/U to 1A13 in the T-1064/GRC-144 through the RECOVERED ORDERWIRE connector and associated cable and the radio patch panel. The recovered ow signal is amplified and distributed to the Converter, Telegraph Telephone Signal CV-425/U, the thru ow send terminals, Headset-Microphone H-91A/U, and the loud speaker. The receive orderwire output (rec voice) is coupled to TD-204/U through the HANDSET connector on T-1064/GRC-144, the PATCH THRU connector on the TD-204/U, and the associated cable. The ow signal and the reformatted pcm signal are then applied to the cable system through the TO CABLE connector on the TD-204/U.

c. *Standard Radio Repeater Configuration* (fig. 5-4). In the standard radio repeater configuration, two AN/GRC-144's are connected back-to-back to function as a radio relay station. Pcm signal processing is required at the interface between radio sets. This is accomplished internally by digital data modem 1A12 in each AN/GRC-44. For radio repeater operation, only the radio-to-cable circuits in each digital data modem are utilized. The two AN/GRC-144's are connected in the radio repeater configuration by making the RADIO REPEATER MODE OF OPERATION connections, at the radio patch panel of each AN/GRC-144 and the appropriate cross connections at the shelter patch panel. The RADIO REPEATER indicator on each radio patch

panel lights when the RADIO REPEATER MODE OF OPERATION connection is completed. Signal paths through the AN/GRC-144's are described in the following subparagraphs.

(1) *Radio set A to radio set B signal path.* The rf signal from distant radio station A is received by antenna system A and is applied to Receiver, Radio R-1467/GRC-144 in radio set A. The rf receive signal is demodulated and amplified in the R-1467/GRC-144. The resulting output signal (combined pcm and orderwire) is applied to the radio-to-cable circuits in 1A12 of Transmitter, Radio T-1054/GRC-144 by the orderwire assembly 1A13 and the radio patch panel. The pcm and orderwire signals are separated in the radio-to-cable circuits. The pcm signal is reshaped and retimed and is applied to attenuator assembly 1A3 of radio set B through the RADIO REPEATER OUTPUT connector on radio set A, the shelter patch panel, the RADIO REPEATER INPUT connector on radio set B, and the radio patch panel in radio set B. The recovered ow and recovered ow sense signals are fed back to 1A13 through the radio patch panel. The recovered ow signal is amplified and distributed within 1A13 to Telephone Set TA312/ IPT, Handset H-166/U, the thru ow send output terminals, and the loud speaker (w(2) above). The thru ow send output of 1A13 in radio set A is applied to the thru ow rec input of radio set B through the radio patch panel and the THRU ORDERWIRE send connection in radio set A, the shelter patch panel, and the THRU ORDERWIRE receive connection in radio set B. The thru ow rec input to 1A13 in radio set B is amplified and distributed. The to radio ow output of 1A13 is applied to attenuator assembly 1A3 in radio set B. The remainder of the transmission path from 1A3 to antenna B is identical to that previously described in a(1) above. The rf is transmitted from antenna B to distant radio station B.

(2) *Radio set B to radio set A signal path.* The rf signal from distant radio station B is received by antenna B, processed by radio set B, and transmitted to distant radio station A through the radio circuits in radio set A and antenna A. Signal processing and transmission is identical to that described in (1) above except in the reverse direction.

d. *Nonstandard Radio Repeater Configuration* (fig. 5-5). In the nonstandard radio repeater configuration, two AN/GRC-144's are connected back-to-back to function as a radio relay

station. This configuration utilizes external equipment to process the pcm signals at the interface between radio sets. Two TD-203/U's (radio combiners) are connected back-to-back at the interface between radio sets to process the FROM RADIO and TO RADIO pcm signals. The two AN/GRC-144's are connected in the nonstandard radio repeater configuration by making the RADIO REPEATER (NONSTANDARD) MODE OF OPERATION connections at each set's radio patch panel. The connection bypasses digital data modem 1A12. Also, the THRU ORDERWIRE cross connections at the shelter patch panel and the TD-203 INTERCONNECTS to the external TD-203/U's must be completed. Signal processing and transmission is identical to that described in c above for the radio repeater configuration, except that the radio-to-cable circuits in 1A12 are bypassed and pcm processing is accomplished by the external TD-203/U's. Also, the TD-203 INTERCONNECTS cable connections are used in place of the RADIO REPEATER INPUT AND OUTPUT cable connections. For 96 channel (biter)ary operation, the applicable controls on Multiplexer TD-203/U must be set for 96 channels.

### 2-2.1. Block Diagram Descriptions of Radio Set AN/GRC-144(V)3 (fig. 5-2)

a. General. Radio Set AN/GRC144(V)3 is the radio link between the cable system and the antenna system and it provides data and orderwire signal processing and routing. Data signals from the DGM and orderwire signals from the orderwire control unit (OCU) and digital line encryption device (DLED) are processed in the transmit direction and transmitted to the distant site. In the receive direction, signals from the distant site are processed and routed to the DGM, DLED and OCU. The data and orderwire signals require various processing (regeneration, descrambling, retiming, multiplexing, demultiplexing); these functions are performed in digital data combiner 1A12. The circuits of digital data combiner 1A12 are functionally divided into cable-to-radio for transmit direction processing and radio-to-cable for receive direction processing (para 2-4.1 and 2-5.1).

b. Transmit Path. Input signals (data from the DGM and orderwire from the OCU and DLED) are applied to the cable-to-radio circuits of digital data combiner 1A12 in Transmitter, Radio T-1054(P)A/GRC-144(V). The orderwire input is either two digital orderwire signals (DOW and DVOW) or one analog orderwire signal (AVOW). When operating in the analog orderwire mode, the AVOW signal is level adjusted in digital data combiner 1A12 and routed to orderwire assembly 1A13 where it is processed as described in paragraph 2-2a(1). When operating in the digital orderwire mode, digital orderwire signals are processed only in digital data combiner 1A12; orderwire assembly 1A13 processes analog orderwire signals but not digital orderwire. The data signal is scrambled, retimed and regenerated, and the digital orderwire (DOW and DVOW) signals are retimed and multiplexed into a single bitstream (CVDOW) in digital data combiner 1A12. The data and CVDOW (multiplexed DOW and DVOW) signals are then combined in a linear summing amplifier and applied to the radio modulator circuits through attenuator 1A3 and af-rf amplifier 1A4. When operating in the analog orderwire mode, this signal is the data signal only and the analog orderwire signal (AVOW) comes from orderwire assembly 1A13. From this point on, signal processing is the same as that described in paragraph 2-2a(1).

c. Receive path. The 4.4 to 5.0 GHz rf receive signal is coupled from the antenna to Receiver, Radio R-1467(P)A/GRC-144(V) through Duplexer CU-1891/GRC, Coupler, Directional CU-1890/GRC, RF INPUT waveguide connector on the R-1467(P)A/GRC-144(V), and associated waveguide assemblies. The rf input signal is amplified and demodulated in the R-1467(P)A/GRC-144(V). The composite data and orderwire output signal is coupled to the T-1054(P)A/GRC-144(V) through the TRAFFIC OUTPUT connector on the R-1467(P)A/GRC-144(V), the TRAFFIC INPUT (RCVR) connector on the T-1054(P)A/GRC-144(V), and an associated interconnecting cable. The combined data and orderwire signal is applied to the

radio-to-cable circuits of digital data combiner 1A12 through orderwire assembly 1A13 and the radio patch panel. The data and orderwire signals are separated in the radio-to-cable circuits. The scrambled data signal is reshaped, retimed, descrambled and reformatted for cable system compatibility, and routed to the DGM. When operating in the analog orderwire mode, the separated orderwire signal (recovered ow) and an orderwire sensing signal (recovered ow sense) are sent back from the radio-to-cable circuits of 1A12 to 1A13 through the radio patch panel. For normal conditions, the recovered ow sense signal, generated in the radio-to-cable circuits, keeps a relay in 1A13 energized allowing the recovered ow signal to be amplified and distributed to the remote phone, Handset H-156/U, the loudspeaker, and back to 1A12 (thru ow send). The thru ow send signal is routed to the OCU. If a data traffic failure is detected in the radio-to-cable circuits of 1A12, the recovered ow sense signal causes the relay in 1A13 to become deenergized. For this condition, the orderwire signal from Receiver, Radio R-1467(P)A/GRC-144(V) is routed through contacts of the relay and is amplified and distributed to Telephone Set TA-312/PT, Handset H-156/U, the loudspeaker, and to 1A12 (thru ow send). Thus, orderwire communication is maintained when a data traffic failure occurs. When operating in the digital orderwire mode, the separated orderwire signal (referred to above) is the CVDOW signal. This signal is demultiplexed into DOW and DVOW signals in digital data combiner 1A12. The DOW and DVOW signals are then routed to the OCU and DLED.

### **2-2.2. Block Diagram Descriptions of Radio Set AN/GRC-144(V)4 (fig. 5-2.1)**

Radio Set AN/GRC-144(V)4 operates in either of two bands: 4.4 to 5.0 GHz 1 (C-band) or 14.4 to 15.0 GHz (K-band). Two antennas (AS-1425/GRC C-band and

AS-3398/GRC-144(V), K-band) are used. Waveguide switches route the transmit and receive signals to/from the appropriate antenna, according to the operating band. The transmitter (T-1054(P)A/GRC-144(V) and receiver (R-1467(P)A/GRC-144(V) are the same as those used with Radio Set AN/GRC-144(V)3. When operating in C-band, T-1054(P)A/GRC-144(V) is routed by waveguide switch 1 through diplexer CU-1891/GRC, waveguide switch 2, and Directional Coupler CU-1890/GRC into the receiver. When operating in K-band, the transmit rf output signal is routed through waveguide switch 1 and Adapter UG-1883/GRC into Converter-Multiplier CV-3633/GRC-144(V). In the CV-3633/G(C-144(V), the transmit signal is up converted to the K-band range and routed to the K-band antenna. The receive path is from the K-band antenna to CV-3633/GRC-144(V), where the signal is down converted to the C-band range. The C-band output of CV-3633/GRC-144(V) is routed through Adapter UG-1883/GRC, waveguide switch 2, and Directional Coupler CU-1890/GRC to the receiver. When operating in either C-band or K-band, the transmit and receive paths in the transmitter (T-1054(P)A/GRC-144(V) and the receiver (R-1467(P)A/GRC-144(V) are the same as those described for Radio Set AN/GRC-144(V)3 (para 2-2.1). Refer to section VI of this chapter for functional descriptions of Converter-Multiplier CV-3633/GRC-144(V) circuits.

### **2-3. Overall Block Diagram Description of Transmitter, Radio T-1054(P)/GRC-144(V) (fig. 5-6)**

Transmitter, Radio T-1054(P)/GRC-144(V) operates in the 4.4 to 5.0 GHz frequency range with a continuous wave (cw) power output of 250 milliwatts nominal. Figure 5-6 illustrates the major signal flow (heavy lines on the diagram)

and the control and alarm signals between assemblies in the T-1054(P)/GRC-144(v). The processing of signals within complex assemblies such as digital data modem 1A12, orderwire assembly 1A13, and electrical frequency synthesizer 1A14 are explained in subsequent paragraphs. The radio patch panel in the T-1054(P)/GRC-144(V) permits connecting Radio Set AN/GRC-144 in any one of four configurations. Figure 5-6 illustrates the connections for the cable terminal configuration (CABLE TERMINAL OPERATION indicator on radio patch panel is lighted). Both the radio-to-cable circuits and the cable-to-radio circuits in digital data modem 1A12 are used in the cable terminal configuration. In the other configuration, the radio patch panel is used to connect external equipment in the signal path and to bypass the cable-to-radio circuits in digital data modem 1A12 or to completely bypass digital data modem 1A12 (para 2-2b, c, and d). The following subparagraphs describe the transmit (cable-to-radio) and the receive (radio-to-cable) signal paths through the T-1054(P)/GRC-144(V). The control and alarm signals in the T-1054(P)/GRC-144(V) are also described.

#### NOTES

1. In both radio repeater modes of operation and in the cable terminal (nonstandard) mode, the external traffic in and traffic out indicators are not lighted.
2. In both nonstandard modes of operation, the CABLE TO RADIO MODEM and RADIO TO CABLE MODEM indicators are not lighted.

### 3. In the radio repeater mode of operation, the CABLE TO RADIO MODEM indicator is not lighted.

a. Transmit Path. The transmit (cable-to-radio) signal path through the T-1054(P)/GRC-144(V) is shown with the FROM CABLE signal entering the T-1054(P)/GRC-144(V) on the left and the RF OUTPUT signal leaving on the right-hand side of figure 5-6.

(1) The FROM CABLE Input (a combined pcm, ow, and de signal) is applied to the cable to-radio circuits of digital data modem 1A12. The CABLE TO RADIO MODEM indicator on meter panel assembly 1A15A8 and a remote traffic in indicator are controlled by the cable-to-radio circuits in 1A12 through the radio patch panel. For normal input pcm traffic conditions, the CABLE TO RADIO MODEM and the traffic in indicators are lighted green. If an input pcm traffic failure is detected by the cable-to-radio circuits in 1A12, the CNTRL ALARM and the external traffic in indicators light red. The CABLE TO RADIO MODEM indicator lights red only when a functional failure exists in 1A12 and actual pcm traffic is present. If pcm traffic is not present, this alarm is inhibited (remains green) even if a functional failure exists. The pcm, ow, and dc portions of the input signal are separated in the cable-to-radio circuits. The cable-to-radio circuits reshape, retime, and convert the pcm train to a level compatible with the radio circuits. The regenerated pcm output (to radio pcm) is routed through the radio patch panel to attenuator assembly 1A3. The ow signal is amplified in the cable-to-radio circuits. The amplified ow signal output (thru ow rec) is routed through the radio patch panel to orderwire

assembly 1A13. The direct current portion of the input signal is looped back to the TO CABLE output of T-1064/GRC-144 by way of the cable-to-radio and the radio-to-cable circuits of 1A12 (para 22a(1)).

(2) The thru ow rec signal is amplified in orderwire assembly 1A13 and distributed to Handset H-156/U, Telephone Set TA-12/PT, attenuator assembly 1A3 (to radio ow), and to the loudspeaker on 1A15A8. The loudspeaker level is controlled by the SPEAKER VOLUME control. The RING pushbutton on 1A15A8 provides in-band tone signaling to locally initiate ow communications. The RING indicator on 1A15A8 lights amber when the RING pushbutton is depressed or when a ring signal is received from a remote ow station. The CNTRL ALARM indicator on meter panel assembly 1A15A8 is controlled by alarm circuits in 1A13. Normally, the CNTRL ALARM indicator is lighted green. If an alarm condition (pcm aim, transmitter aim, receiver aim, or remote traffic in aim) is detected, the CNTRL ALARM indicator lights red and an audible alarm is heard over the loudspeaker. The RESET pushbutton on 1A15A8 or the external alarm disable switch is used to silence the audible alarm; however, the red CNTRL ALARM indication will remain until the alarm condition is removed. The WAVEGUIDE SW indicator on 1A15A8 is lighted green when Switch, Waveguide SA-1679/GRC is set to the ANTENNA (NORMAL) position and lights red when the SA-1679/GRC is set to the TO LOAD (TEST) position.

(3) Attenuator assembly 1A3 provides attenuation and phase shift circuits for the to radio pcm and attenuation to ow signals. A detected ow test signal from 1A3 is applied to the metering circuits on 1A15A8. The pcm and ow output signals from 1A3 are combined at the output of af-rf amplifier 1A4. The pcm signal is amplified in 1A4 and the combined pcm and ow output is applied to 45 MHz low pass filter 1A6. The 4.6 MHz low pass filter shapes the pcm signal before it is applied to radio transmitter modulator 1A8. A detected traffic level signal (representative of the input to 1A8) is fed back to the alarm monitor 1A5 through attenuator assembly 1A8. If the traffic level signal is present (normal condition), alarm monitor 1A6 causes the TRAF indicator on 1A15A8 to light green. If the traffic level signal is absent (alarm condition), 1A5 causes the TRAF and CNTRL ALARM indicators to light red. The traffic

level signal is also routed to the metering circuits in 1A15A8 through alarm monitor 1A5.

(4) The combined pcm and ow signal frequency modulates a 150 MHz carrier in 1A8. Electronic frequency control 1A7 provides automatic frequency control (afc) of the 150 MHz carrier. Frequency control and modulator signal levels from 1A7 and 1A8 are applied to the metering circuits in 1A15AB. The 150 MHz frequency modulated output of 1A8 is applied to transmitter frequency mixer stage 1A9 where it is mixed with a 4.55 to 4.856 GHz local oscillator signal which is produced by electrical frequency synthesizer 1A14 and a times 16 multiplier chain. The electrical frequency synthesizer generates a highly stable frequency in the range of 284.375 to 308.125 MHz. The detected output level (synth level) is applied to metering circuits on 1A15A8. The SYNTH OVEN lamp (press-to test) on meter panel assembly 1A15A8 lights white when the standard radio frequency oscillator oven in 1A14 is at the correct temperature. In addition, a synthesizer monitor signal is applied from 1A14 to alarm monitor 1A5. This signal indicates if the radio frequency oscillator and the standard radio frequency oscillator contained in 1A14 are phase locked. If an in-phase lock condition exists, the SYNTH LOCK indicator on 1A15A8 lights green. An out-of-phase lock condition causes the SYNTH LOCK and CNTRL ALARM indicators to light red. The 284.375 to 303.125 MHz output from 1A14 is applied to the times 16 multiplier chain which is comprised of transmitter amplifier-frequency multiplier 1A11, coaxial circulator 1HY1, and transmitter frequency multiplier group 1A10. The signal is amplified and multiplied to 1137-1213 MHz in 1A11. The signal is then coupled through 1HY1 to 1A10. Coaxial circulator 1HY1 provides isolation between the frequency multiplier circuits. Transmitter frequency multiplier group 1A10 multiplies the 1137 to 1213 MHz signal up to the 4.55 to 4.85 GHz local oscillator frequency for application to transmitter frequency mixer stage 1A9. Detected signal levels in the times 16 multiplier chain are applied to the metering circuits in 1A15A8. The 1137 to 1213 MHz output of 1A11 is detected (ampl-mult) within 1HY1 and applied to the metering circuits. The 2275 to 2425 MHz signal generated by the 2nd frequency multiplier circuits in 1A10 is detected (2nd mult) and applied to the metering circuits. The 4.55 to 4.85 GHz output generated by the 3rd frequency multiplier circuits in 1A10 is detected

(3rd mult) within 1A9 and applied to the metering circuits.

(6) The 4.55 to 4.85 Hz signal is mixed with the 150 MHz frequency modulated signal (containing the pcm signal and orderwire) in transmitter frequency mixer stage 1A9 to produce the 4.4 to 5.0 GHz carrier output signal which is applied to rf bandpass filter 1FL3. The bandpass filter is set to the required carrier frequency. The lower side band frequency (local oscillator minus 150 MHz) is selected for the low band of carrier output frequencies (4400 to 4699.9 MHz). The upper sideband frequency (local oscillator plus 150 MHz) is selected for the high band of output frequencies (4.7 to 5.0 GHz). The selected carrier frequency is passed through rf low pass filter 1FL4 to directional coupler 1DC1. The main output of the directional coupler is applied to Switch, Waveguide SA1-679/GRC. A secondary output is sent to the radio test set. The RADIO TEST SET indicator on 1A15A8 lights red when the radio test set is turned on and green when it is turned off. In addition, detected forward and reflected rf power signals are sent from 1DC1 to alarm monitor 1A5 and to the metering circuits in 1A15A8. For normal conditions, the RF POWER and REFL RF POWER indicators are lighted green. A loss of rf power output or a high level of reflected power will cause the associated indicator and the CNTRL ALARM indicator to light red.

*b. Receive Path.* In the receive (radio-to-cable) signal path through the T-1054/GRC-144, the combined pcm and ow signal from Receiver, Radio R-1467/GRC-144 is applied to the radio to-cable circuits of 1A12 through orderwire assembly 1A13 and the radio patch panel. Note also in figure 5-6 that the radio patch panel is used to connect the radio-to-cable circuits of 1A12 in the signal path for the radio repeater mode of operation.

(1) The radio-to-cable circuits separate the pcm reshaped and retimed for application to the cable system. The recovered ow signal is amplified and fed back to 1A13 through the radio patch panel along with the recovered ow sense signal. The recovered ow signal is amplified in 1A13 and distributed to Handset H-156/U, Telephone Set TA-12/PT, the loudspeaker, and back (thru ow send) to the radio-to-cable circuits in 1A12. The pcm and ow signals are then combined with the direct current (from the cable-to-radio circuits) and the composite signal is applied to the cable system. The radio-to-cable circuits also provide a pcm output

signal to radio repeater for the radio repeater mode of operation.

(2) The RADIO TO CABLE MODEM indicator on meter panel assembly 1A15A8 and an external traffic out indicator are controlled by the radio-to-cable circuits of 1A12 through the radio patch panel. For normal output pcm traffic conditions, the RADIO TO CABLE MODEM and the external traffic out indicators are lighted green. If an output pcm traffic failure is detected by the radio-to-cable circuits in 1A12, the CNTRL ALARM and external traffic out indicators light red. The RADIO TO CABLE MODEM indicator lights red only when a functional failure exists in 1A12 and actual pcm traffic is present. If pcm traffic is not present, this alarm is inhibited (remains green) even if a functional failure exists.

(3) A normally energized relay in orderwire assembly 1A13 is controlled by the recovered ow sense signal from the radio-to-cable circuits in 1A12. If the pcm portion of the input signal from Radio, Receiver R-1467/GRC-144 is missing, the relay becomes deenergized. With the relay deenergized, the orderwire signal received from the R-1467/R-144 is applied to the orderwire circuits in place of the recovered ow signal from 1A12. Thus, orderwire communication is maintained when the pcm traffic portion of the signal from the R-1467/GRC-144 is lost.

(4) A receiver alarm signal is also applied to the alarm circuit in 1A13 from the R-1467/GRC-144. If an alarm condition is present in the R-1467/GRC-144, this signal will cause the CNTRL ALARM indicator on 1A15A8 to light red and the loudspeaker to sound an audible alarm.

(5) The pcm aim signal from digital data modem 1A12 summarizes the alarm conditions within 1A12. It is applied to the alarm circuits in 1A13 along with the transmitter and receiver alarm signals to control the CNTRL ALARM indicator and audible alarm. Since the cable-to radio circuits in 1A12 are not used in the radio repeater configuration, a cable-to-radio alarm inhibit signal is applied to the radio patch panel. When the radio patch panel is connected in the RADIO REPEATER MODE OF OPERATION, this signal inhibits the cable-to-radio alarm circuits in 1A12 from activating the CNTRL ALARM indicator and the audible alarm.

*c. Metering Circuits.* Signals from various components in the T4064/GRC-144 are monitored at meter panel assembly 1A15A8. The metering

circuits consist of a meter selector switch and a meter. A signal is monitored by setting the meter selector switch to the appropriate position. Meter calibration resistors are provided for certain meter indications. The metering circuit also provides a test position which allows component test lead monitoring.

d. Power Supply Circuits. Power supply 1A1 produces regulated +28 vdc, +15 vdc, +12 vdc, -12 vdc, -6 vdc and +5 vdc voltages required to operate the circuits and indicators in Transmitter, Radio T-1054(P)/GRC-144(V).

### **2-3.1. Overall Block Diagram Description of Transmitter, Radio T-1054(P)/GRC-144(V) (fig. 5-6.1)**

Transmitter, Radio T-1054(P)/GRC-144(V) operates in the 4.4 to 5.0 GHz frequency range with a continuous wave (cw) power output of 250 milliwatts nominal. Figure 5-6 illustrates the major signal flow (heavy lines on the diagram) and the control and alarm signals between assemblies in the T-1054(P)/GRC-144(V). The processing of signals within complex assemblies such as digital data combiner 1A12, orderwire assembly 1A13, and electrical frequency synthesizer 1A14 are explained in subsequent paragraphs.

a. Transmit Path. The transmit (cable-to-radio) signal path through the T-1054(P)/GRC-144(V) is shown with the FROM CABLE signal entering the T-1054(P)/GRC-144(V) on the left and the RF OUTPUT signal leaving on the right-hand side of figure 5-6.

(1) The FROM CABLE input (data signal from the DGM and orderwire signal from the OCU and CLED) is applied to the cable-to-radio circuits of digital data combiner 1A12. The CABLE TO RADIO MODEM indicator on meter panel assembly 1A15A8 and a remote traffic in indicator are controlled by the cable-to-radio circuits in 1A12 through the radio patch panel. For normal input data traffic conditions, the CABLE TO RADIO MODEM and the traffic in indicators

are lighted green. If an output data traffic failure is detected by the cable-to-radio circuits in 1A12, the CNTRL ALARM and the external traffic in indicators light red. The CABLE TO RADIO MODEM indicator lights red only when a functional failure exists in 1A12 and actual data traffic is present. If data traffic is not present, this alarm is inhibited (remains green) even if a functional failure exists. The orderwire input is either two digital orderwire signals (DOW and DVOW) or one analog orderwire signal (AVOW). When operating in the analog orderwire mode, the AVOW is routed to orderwire assembly 1A13 where it is processed as described in (2) below. When operating in the digital orderwire mode, digital orderwire signals are processed only in digital data combiner 1A12; orderwire assembly 1A13 processes analog orderwire signals but not digital orderwire. The data signal is scrambled, retimed and regenerated, and the digital orderwire (DOW and DVOW) signals are retimed and multiplexed into a single bitstream (CVDOW) in digital data combiner 1A12. The data and CVDOW (multiplexed DOW and DVOW) signals are then combined in a linear summing amplifier and applied to the radio modulator circuits through attenuator 1A3 and af-rf amplifier 1A4. When operating in the analog orderwire mode, this signal is the data signal only; the analog orderwire signal (AVOW) comes from orderwire assembly 1A13.

(2) The thru ow rec signal is amplified in orderwire assembly 1A13 and distributed to Handset H-156/U, Telephone Set TA-312/PT, attenuator assembly 1A3 (to radio ow), and to the loudspeaker on 1A15A8. The loudspeaker level is controlled by the SPEAKER VOLUME control. The RING pushbutton on 1A15A8 provides in-band tone signaling to locally initiate ow communications. The RING indicator on 1A15A8 lights amber when the RING pushbutton is depressed or when a ring signal is received from a remote ow station. The CNTRL alarm indicator on meter panel assembly 1A15A8 is controlled by alarm circuits in 1A13. Normally, the CNTRL ALARM indicator is lighted green. If an



alarm condition (data alm, transmitter alm, receiver alm, or remote traffic in alm) is detected, the CNTRL ALARM indicator lights red and an audible alarm is heard over the loudspeaker. The RESET pushbutton on 1A15A8 or the external alarm disable switch is used to silence the audible alarm; however, the red CNTRL ALARM indication will remain until the alarm condition is removed. The WAVEGUIDE SW indicator on 1A15A8 is lighted green when Switch, Waveguide SA-1679/GRC is set to the ANTENNA (NORMAL) position and lights red when the SA-1679/GRC is set to the TO LOAD (TEST) position.

(3) Attenuator assembly 1A3 provides attenuation and phase shift circuits for the to radio data and digital ow signal and attenuation to analog ow signals. A detected analog ow test signal from 1A3 is applied to the metering circuits on 1A15A8. The data and analog ow output signals from 1A3 are combined at the output of af-rf amplifier 1A4. The data signal is amplified in 1A4 and the combined data and ow output is applied to 4.5 MHz low pass filter 1A6. The 4.5 MHz low pass filter shapes the data signal before it is applied to radio transmitter modulator 1A8. A detected traffic level, (representative of the input to 1A8) is fed back to the alarm monitor 1A8 through attenuator assembly 1A3. If the traffic level signal is present (normal condition), alarm monitor 1A5 causes the TRAF indicator on 1A15A8 to light green. If the traffic level signal is absent (alarm condition), 1A5 causes the TRAF and CNTRL ALARM INDICATORS TO LIGHT WRD. The traffic level signal is also routed to the metering circuits in 1A15A8 through alarm monitor 1A5.

(4) The combined data and ow signal frequency modulates a 150 MHz carrier in 1A8. Electronic frequency control 1A7 provides automatic frequency control (afc) of the 150 MHz carrier. Frequency control and modulator signal levels from 1A7 and 1A8 are applied to the metering circuits in 1A15A8.

The 150 MHz frequency modulated output of 1A8 is applied to transmitter frequency mixer stage 1A9 where it is mixed with a 4.55 to 4.85 GHz local oscillator signal, which is produced by electrical frequency synthesizer 1A14 and a times 16 multiplier chain. The electrical frequency synthesizer generates a highly stable frequency in the range of 284.375 to 303.125 MHz. The detected output level (synth level) is applied to metering circuits on 1A15A8. The SYNTH OVEN lamp (press-to-test) on meter panel assembly 1A15A8 lights white when the standard radio frequency oscillator oven in 1A14 is at the correct temperature. In addition, a synthesizer monitor signal is applied from 1A14 alarm monitor 1A5. This signal indicates if the radio frequency oscillator and the standard radio frequency oscillator contained in 1A14 are phase locked. If an in-phase lock condition exists, the SYNTH LOCK indicator on 1A15A8 lights green. An out-of-phase lock condition causes the SYNTH LOCK and CNTRL ALARM indicators to light red. The 284.375 to 303.125 MHz output from 1A14 is applied to the times 16 multiplier chain which is comprised of transmitter amplifier frequency multiplier 1A11, coaxial circulator 1HY1, and transmitter frequency multiplier group A10. The signal is amplified and multiplied to 1137-1213 MHz in 1A11. The signal is then coupled through 1HY1 to 1A10. Coaxial circulator 1HY1 provides isolation between the frequency multiplier circuits. Transmitter frequency multiplier group 1A10 multiplies the 1137 to 1213 MHz signal up to the 4.55 to 4.85 GHz local oscillator frequency for application to transmitter frequency mixer stage 1A9. Detected signal levels in the times 16 multiplier chain are applied to the metering circuits in 1A15A8. The 1137 to 1213 MHz output of 1A11 is detected (ampl-mult) within 1HY1 and applied to the metering circuits. The 2275 to 2425 MHz signal generated by the 2nd frequency multiplier circuits in 1A10 is detected (2nd mult) and applied to the metering circuits. The 4.55 to 4.85 GHz output generated by the 3rd frequency multiplier circuits in 1A10 is detected

(3rd mult) within 1A9 and applied to the metering circuits.

(5) The 4.55 to 4.85 Hz signal is mixed with the 150 MHz frequency modulated signal (containing the data signal and orderwire) in transmitter frequency mixer stage 1A9 to produce the 4.4 to 5.0 GHz carrier output signal which is applied to rf bandpass filter 1FL3. The bandpass filter is set to the required carrier frequency. The lower side band frequency (local oscillator minus 150 MHz) is selected for the low band of carrier output frequencies (4400 to 4699.9 MHz). The upper sideband frequency (local oscillator plus 150 MHz) is selected for the high band of output frequencies (4.7 to 5.0 GHz). The selected carrier frequency is passed through rf low pass filter 1FL4 to directional coupler 1DC1. The main output of the directional coupler is applied to Switch, Waveguide SA-1679/GRC. A secondary output is sent to the radio test set. The RADIO TEST SET indicator on 1A15A8 lights red when the radio test set is turned on and green when it is turned off. In addition, detected forward and reflected rf power signals are sent from 1DC1 to alarm monitor 1A5 and to the metering circuits in 1A15A8. For normal conditions, the RF POWER and REFL RF POWER indicators are lighted green. A loss of rf power output or a high level of reflected power will cause the associated indicator and the CNTRL ALARM indicator to light red.

b. Receive Path. In the receive (radio-to-cable) signal path through the T-1054(P)/A/GRC-144(V), the combined data and ow signal from Receiver, Radio R-1467(P)/A/GRC-144(V) is applied to the radio-to-cable circuits of 1A12 through orderwire assembly 1A13 and the radio patch panel.

(1) The radio-to-cable circuits separate the reshaped and retimed data for application to the cable system. The recovered ow signal is amplified and fed back to 1A13 through the radio patch panel along with the recovered ow sense signal. The recovered ow signal is amplified in 1A13 and distributed to Handset H-

156/U, Telephone Set TA-312/PT, the loudspeaker, and back (thru ow send) to the radio-to-cable circuits in 1A12.

(2) The RADIO TO CABLE MODEM indicator on meter panel assembly 1A15A8 and an external traffic out indicator are controlled by the radio-to-cable circuits of 1A12 through the radio patch panel. For normal output data traffic conditions, the RADIO TO CABLE MODEM and the external traffic out indicators are lighted green. If an output data traffic failure is detected by the radio-to-cable circuits in 1A12, the CNTRL ALARM and external traffic out indicators light red. The RADIO TO CABLE MODEM indicator lights red only when a functional failure exists in 1A12 and actual data traffic is present. If data traffic is not present, this alarm is inhibited (remains green) even if a functional failure exists.

(3) A normally energized relay in orderwire assembly 1A13 is controlled by the recovered ow sense signal from the radio-to-cable circuits in 1A12. If the data portion of the input signal from Radio, Receiver R-1467(P)/A/GRC-144(V) is missing, the relay becomes deenergized. With the relay deenergized, the orderwire signal received from the R-1467(P)/A/GRC-144(V) is applied to the orderwire circuits in place of the recovered ow signal from 1A12. Thus, orderwire communication is maintained when the pcm traffic portion of the signal from the R-1467(P)/A/GRC-144(V) is lost.

(4) A receiver alarm signal is also applied to the alarm circuit in 1A13 from the R-1467(P)/A/GRC-144(V). If an alarm condition is present in the R-1467(P)/A/GRC-144(V), this signal will cause the CNTRL ALARM indicator on 1A15A8 to light red and the loudspeaker to sound an audible alarm.

(5) The data alarm signal from digital data combiner 1A12 summarizes the alarm conditions within 1A12. It is

applied to the alarm circuits in 1A13 along with the transmitter and receiver alarm signals to control the CNTRL ALARM indicator and audible alarm.

c. Metering Circuits. Signals from various components in the T-1054(P)A/GRC-144(V) are monitored at meter panel assembly 1A15A8. The metering circuits consist of a meter selector switch and a meter. A signal is monitored by setting the meter selector switch to the appropriate position. Meter calibration resistors are provided for certain meter indications. The metering circuit also provides a test position which allows component test lead monitoring.

d. Power Supply Circuits. Power supply 1A1 produces regulated +28 vdc, +15 vdc, +12 vdc, -12 vdc,

-6 vdc and +5 vdc voltages required to operate the circuits and indicators in Transmitter, Radio T-1054(P)A/GRC-144(V).

**2-4. Overall Block Diagram Description of Digital Data Modem 1A12 (fig. 2-1 and 2-1.1)**

a. Digital Data Interface. Digital data modem 1A12 interfaces the cable systems and Radio Set AN/GRC-144. It has two modes of operation: synchronous (48-channel only) and asynchronous (48-channel or 96-channel). The complement of plug in components used depends on the operating mode as shown in the chart below. In addition, when the 96-channel mode is used, 1.0 MHz low pass filter 2A3 must be replaced with 3.8 MHz low pass filter 2A17 for digital data interface.

48-channel synchronous (DDM)	Description	48 channel asynchronous (ADDM)	96 channel asynchronous (ADDM)
1A12A1 (4608 KHz).....	Voltage controlled oscillator.....	1A12A17 ..... (Dummy Panel).....	1A12A17 (Dummy Panel)
1A12A2 .....	Cable digital regenerator .....	1A12A13.....	A12A13
1A12A3 .....	Cable control-compactor .....	1A12A14.....	1A12A14
1A12A4 .....	Cable digital processor.....	1A12A4.....	1A12A4
1A12A5 .....	Alarm monitor.....	1A12A15.....	1A12A15
1A12A6 .....	Af amplifier.....	1A12A6.....	1A12A6
1A12A7 .....	Radio amplifier-detector .....	1A12A7.....	1A12A7
1A12A8(w/Y1).....	Radio digital regenerator .....	1A12A8(w/Y2).....	1A12A8(w/Y2)
1A12A9 .....	Radio control-comparator.....	1A12A9.....	1A12A9
1A12A10 .....	Radio digital processor.....	1A12A16.....	1A12A16
1A12A11 (4608 KHz).....	Voltage controlled oscillator.....	1A12A18 (9..... (9 830400 MHz).....	1A12A18 (9.830400 MHz)
2A3 (10 MHz).....	Low pass filter.....	2A3 (1.0 MHz).....	2A17 (3.8 MHz)

(1) In the radio receive direction (radio-to-cable), digital data modem 1A12 receives the combined pcm and orderwire signal from Receiver, Radio R-1476/RC-144 and separates the pcm signal from the orderwire signal. The pcm signal is processed by digital data modem 1A12 into a form which is compatible with the cable system. This is explained in (3) below. The recovered orderwire signal is applied to orderwire assembly 1A13 for further processing. Before applying the processed pcm signal to the cable, digital data modem 1A12 recombines it with the orderwire signal from orderwire assembly 1A13. There is a continuous direct current path between the cable input terminal of digital data modem 1A12 and the cable output terminal, so the output signal is comprised of pcm/orderwire/dc.

(2) the radio transmit direction (cable-to-radio), digital data modem 1A12 receives a combined pcm/orderwire/dc signal from the cable system. Digital data modem 1A12 separates the two signal components and loops the direct current back to the cable output terminal to complete the closed circuit direct current path. The extracted pcm signal is processed by digital data modem 1A12 into the form required for radio transmission. This is explained in (3) below. The from cable orderwire signal is applied to orderwire assembly 1A13 for further processing.

(3) In the synchronous mode, Radio Set AN/GRC-144 transmits and receives information in a 48-channel pulses code modulation (pcm) system. The signal is in the form of a serial stream of voltage pulses (bits) representing the

pcm code. The pcm code bits are either logic one, represented by a positive voltage level, or logic zero, represented by a zero voltage level. The time allotted for each bit is referred to as a baud. When a logic one bit is represented by the plus voltage level for the entire baud time, the signal is designated full baud. If it is

represented by the plus voltage level for only one-half the baud time and the signal level is zero volts for the other half of baud time, the signal is designated one half baud. In Radio Set AN/GRC-144(V), one baud is 434 nanoseconds corresponding to a frequency of 2304 kHz. In the cable-to-radio direction, the signal received from

the cable is half-baud; this signal is converted to full baud for radio transmission (fig. 5-32, waveforms B and E). In the radio-to-cable direction, the signal from Receiver, Radio R-1467(P)/GRC-144(V) is full baud; this signal is converted to half-baud for cable transmission (fig. 5-38, waveform A and D).

(3.1) In the asynchronous mode, Radio Set AN/GRC-144 transmits and receives information in a 48-channel or 96-channel pulse code modulation system. In this mode the "to cable" (TOCX) and "from cable" (FRCX) signals are similar to the corresponding signals in the synchronous mode, except that bipolar signal coding at a bit rate of 4.9152 MHz (1 baud is 203.45 nanosec) is used for the pcm component of the signal. The cable signals (TOCX and FRCX) are transmitted at the same pulse width and pulse rate for both 48-channel and 96-channel data rates. When operating at the 96-channel data rate, a 1/2-baud pulse is transmitted for each binary 1 and succeeding pulses are alternately positive and negative (bipolar); when operating at the 48-channel rate, two 1/2-baud bipolar pulses (one of each polarity) are transmitted for each binary 1. No pulses are transmitted for binary 0. The waveforms for the asynchronous mode pcm signals are illustrated in figure 2-1.1. The "to radio" (TRPCM) and "from radio" (FRPCM) signals are similar for both synchronous and asynchronous modes of operation; they are full baud binary and are transmitted at either the 48- or 96-channel data rate, as selected.

(4) The basic signal mnemonics used in digital data modem 1A12 block diagram descriptions are listed in the following chart. As used on the diagrams, and in the descriptions the mnemonics have a prefix 1 for logic one or 0 for logic zero to indicate the active logic state of the signal at the point. The mnemonics listed in the chart do not have the prefix 1 or 0, as the basic meaning of the mnemonic is the same for either prefix. Thus, 1RRIFAIL (output pin 10, fig. 5-36) means that logic one at this point indicates a radio receiver interface failure. ONOR (output pin F, fig. 5-38) means that logic zero at this point indicates a radio traffic failure.

Mnemonic	Meaning
BP	Full baud data pulse
BPØW	Bypass orderwire
CCEXØW	Cable extracted orderwire
CCFAIL	Cable comparator failure
CCØWIN	Cable orderwire in
CCRØW	Cable receive orderwire
CCTØ	Cable transmit orderwire.
CFFL	Cable-to-radio functional failure
CLPCM	Cable loopback pcm
CP	Clock pulse
CRFAIL	Cable regenerator failure
CRLFIL	Cable-to-radio logic failure
CSPCM	Cable sliced pcm

Mnemonic	Meaning
CTFL	Cable-to-radio traffic failure
CVCØI	Cable voltage controlled oscillator modulation
DCSPCM	Cable sliced pcm data
DP	Data pulse
FP	Phase pulse
FRCX	Pcm/orderwire/dc
FRCXØW	Orderwire/dc
FRPCM	Pcm/orderwire
FRFAIL	From radio pcm failure
MARY	MAJOR ALARM SUMMARY
N2304	2304 KHz Cable-to-radio clock
NCLK	Narrow clock (CTIM inverted)
NØR	To cable signal normal
Np	Negative pulse
ØW	Orderwire
ØWI	Orderwire In
PP	Positive pulse
R2304	2304 kHz radio-to-cable clock
R4608	4608 kHz radio-to-cable clock
RCFAIL	Radio comparator failure
RFFL	Radio-to-cable functional failure
RPCM	Retimed pcm
RPFAIL	Radio digital processor failure
RRIFAIL	Radio receiver interface failure
RRM	Radio repeater mode
RRØW	Radio recovered orderwire
RRPCM	Radio repeater pcm
RRPFIL	Radio repeat pcm failure
RSPCM	Reshaped pcm
RTFL	Radio-to-cable traffic failure
RVCØI	Radio voltage controlled oscillator modulation
TC1	Test control 1-not used
TC2	Test control 2-not used
T4608	4608 kHz cable-to-radio clock
TEST	Not in cable-loopback-mode
TØCX	To cable
TRPCM	To radio pcm
XCPCM	Cable traffic

(5) Digital data modem 1A12 contains plug-in components listed in paragraph 2-4a and associated chassis-mounted connectors and components. For synchronous operation, plug-in components 1A12A1, 1A12A2, and 1A12A3 are used exclusively in the cable-to-radio function; plug-in components 1A12A7, 1A12A8, 1A12A9, 1A12A10 and 1A12A11 are used exclusively in the radio-to-cable function. Plug-in components 1A12A4, 1A12A5, and 1A12A6 provide circuits for both functions. These statements apply also to asynchronous operation with the corresponding asynchronous reference designations used. Subparagraphs b and c below describe the main signal paths in digital data modem 1A12. Functional block diagram descriptions of the cable-to-radio and radio-to-cable circuits of digital data

modem 1A12 are provided in paragraphs 2-5 and 2-6.

*b. Cable-to-Radio Circuits, Synchronous Mode.* The cable-to-radio circuits (fig. 2-1, lower section) of digital data modem 1A12 provide processing of the pcm/orderwire/dc signal received from the cable system. The pcm and orderwire signals are separated for individual processing. The orderwire signal is applied to orderwire assembly 1A13. The pcm signal is processed in digital data modem 1A12. Upon completion of processing, the pcm and orderwire (from 1A13) signals are applied to the modulator circuits of Transmitter, Radio T-1054/GRC-144.

(1) The pcm/orderwire/dc signal is applied to cable digital regenerator 1A12A2 which separates the signals. The pcm signal is reshaped into a digital form (fig 2-2A and B) and applied to cable control comparator 1A12A3 as the cable sliced pcm signal. The orderwire/dc signal is applied to transformer 1A12A12A1T1 (fig. 5-29). The orderwire signal is coupled to the transformer secondary and applied to af amplifier 1A12A6. The direct current path is maintained through the primary of the transformer and other components of digital data modem 1A12 for subsequent return to the cable system (para 2-6c). The cable extracted orderwire signal is amplified by af amplifier 1A12A6 and applied to orderwire assembly 1A13.

(2) Cable control comparator 1A12A3 functions in conjunction with 4608 kHz vco 1A12A1 to develop a cable-to-radio data timing signal for internal use and for use in cable digital processor 1A12A4. Cable control comparator 1A12A3 compares the phase of the cable sliced pcm input (which is at the cable bit rate of 2304 kilobits/second) with the phase of a 2304 kHz timing signal developed from the 4608 kHz cable-to-radio clock input from 4608 kHz vco 1A12A1. If the pcm signal and the 2304 kHz timing signal are not in phase, cable control comparator 1A12A3 generates a correction voltage (cable vco modulation) that is applied to 1A12A1 and causes it to change the frequency (4608 kHz) output such that the phase of the 2304 kHz timing signal coincides with the phase of the pcm data. Thus, cable control comparator 1A12A3 and 1A12A1 form a phase-locked loop that phase-locks the 2304 kHz cable-to-radio clock output of cable control comparator 1A12A3 to the pcm data. The cable sliced pcm and the phase-locked 2304 kHz cable-to-radio clock signals are applied to cable digital processor 1A12A4 for retiming of the pcm signal.

(3) Cable digital processor 1A12A4 retimes the half-baud, cable pcm signal (fig. 5-32, waveform B) into a full-baud signal (fig. 5-32, waveform E). Using the

2304 kHz cable-to-radio clock input, cable digital processor 1A12A4 generates the timing signal used in reformatting and retiming the pcm signal. The reformatting and retimed pcm output (to radio) of cable digital processor 1A12A4 is applied to the modulator circuits of Transmitter, Radio T-1054/GRC-144 for combining with the orderwire signal and subsequent radio transmission.

(4) Cable digital processor 1A12A4 also includes a cable loopback function. When the CABLE LOOP TEST switch is in TEST position, cable digital processor 1A12A4 applies the cable sliced pcm signal input (which is received by cable digital regenerator 1A12A2 from the cable system) to the radio-to-cable circuits of digital data modem 1A12 as a cable loopback pcm signal. The radio-to-cable circuits loop the pcm signal back to the cable system for system maintenance purposes.

(5) The cable-to-radio circuits also include an alarm monitoring capability. Cable-to-radio fault conditions are detected in cable digital regenerator 1A12A2, cable control comparator 1A12A3, and cable digital processor 1A12A4 and applied to alarm monitor 1A12A5. Alarm monitor 1A12A5 generates applicable fault alarm signals that control digital data modem 1A12 and fault indicators on meter panel assembly 1A15A8. Alarm monitor 1A12A5 also generates an alarm summary which is sent to the shelter summary alarm of Radio Set AN/GRC-144.

*b.1. Cable-to-Radio Circuits, Asynchronous Mode.* The discussion of *b* above applies also for the asynchronous mode, except as noted here (see fig. 2-1.1, lower section).

(1) Voltage controlled oscillator 1A12A1 is not used. The cable-to-radio clock signal (4915.2 kHz) is generated in cable digital regenerator 1A12A13 and designated 1CTIM. It is extracted from the pcm timing inherent in the signal by means of a crystal filter resonant circuit.

(2) Cable control comparator 1A12A14 retimes the pcm signal and inverts signal 1CTIM to 1NCLK. The pcm and 1NCLK signals are applied to 1A12A4

*c. Radio-to-Cable Circuits.* The radio-to-cable circuits (fig 2-1 and 2-1.1, upper section) of digital data modem 1A12 provide processing of the pcm/orderwire signal input from Receiver. Radio R-1467(P)/GRC-144(V). The radio-to-cable circuits separate the pcm signal and the orderwire signal. The recovered orderwire signal is applied to orderwire assembly 1A13 for further

processing. After the pcm signal, has been processed, it is recombined with the orderwire signal (from orderwire assembly 1A13) and the cable direct current and applied to the cable system. The following discussion applies for the synchronous and asynchronous modes, except as follows 1. In the asynchronous mode the frequency of voltage controlled oscillator 1A12A18 is 9830.4 kHz 2. The radio-to-cable clock frequencies are 2457.6 (48-channel) and 4915.2 (96-channel)

(1) Radio traffic consisting of the pcm/orderwire signal is applied to radio digital regenerator 1A12A8 and to radio amplifier detector 1A12A7. In radio digital regenerator 1A12A8, the pcm signal is separated from the orderwire signal. The pcm signal which is distorted after radio transmission, is reshaped by generating squarewave pulses under control of the input pcm signal. The reshaped pcm signal is applied to radio control comparator 1A12A9 and radio amplifier-detector 1A12A7. Radio control comparator 1A12A9 functions in conjunction with 4608 kHz vco 1A12A11 to generate the signal voltage which controls the output frequency of 1A12A11. Radio amplifier-detector 1A12A7 uses the reshaped pcm signal (from 1A12A8) in conjunction with the pcm/orderwire signal from Receiver, R-1467(P)/GRC-144(V) to separate the radio orderwire signal from the pcm component. The orderwire signal is then applied to orderwire assembly 1A13 where it is distributed to the orderwire stations and back (thru ow send) to af amplifier 1A12A6. The ow signal is then transformer coupled (1A12A12A2T2) and combined with the direct current and applied to radio digital processor 1A12A10. The ow and direct current signals are combined with the pcm signal in 1A12A10 for application to the cable system.

(2) Radio control-comparator 1A12A9 compares the phase of the 2304 kHz radio-to-cable clock signal with the phase of the incoming pcm signal and generates a dc control voltage which is proportional to the phase difference between the two signals. The dc control signal is used to correct the frequency of the 4608 kHz radio-to-cable clock output of voltage controlled oscillator 1A12A11 to the frequency of the pcm signal. The 2304 kHz radio-to-cable clock signal is developed within 1A12A9 from the 4608 kHz radio-to-

cable clock output of 1A12A11. The retimed pcm and 2304 kHz radio-to-cable clock output from 1A12A9 are sent to radio digital processor 1A12A10. The retimed pcm output from 1A12A9 is also applied to cable digital processor 1A12A4. Cable digital processor 1A12A4 is used to process the retimed pcm signal for the radio repeater mode of operation (3) Radio digital processor 1A12A10 reformats the retimed pcm signal for cable system compatibility. Radio digital processor 1A12A10 produces a half-baud pcm signal from the full baud retimed pcm and the 2304 kHz radio-to-cable clock inputs from 1A12A9. The reformatted pcm is combined in 1A12A10 with the ow and direct current signals for application to the cable system. The cable loopback pcm signal is applied to radio digital processor 1A12A10 from cable digital processor 1A12A4 for testing purposes.

#### 2-4.1. Overall Block Diagram Description of Digital Data Combiner 1A12. (fig. 2-1.2)

a. Interface. Radio Sets AN/GRC144-V)3 and (V)4 transmit data and orderwire signals from a local DGM (data), a local DLED, a local OCU (orderwire) and return signals received by radio from the remote site to the local DGM, DLED and OCU. Digital data combiner 1A12 is the interface between the DGM/DLED/OCU and the radio set. Its function in the transmit direction is to convert balanced input signals to TTL levels for internal processing (regeneration, timing, scrambling, multiplexing, level adjustment) and route the output signals to the transmitter modulator circuits. In the receive direction, digital data combiner 1A12 retimes, regenerates, descrambles and demultiplexes the radio received signals. At the output it converts them to balanced signals at specified levels for routing by cable to the local DGM, DLED and OCU. The signals are data signals to and from the local DGM and either two digital orderwire signals (DOW at 2 kb/s and DVOW at 16 kb/s) or one analog orderwire signal (AVOW) The data signal rate (in both directions) is determined at the local and remote DGM's (both must use the same rate). When this rate has been determined, digital data combiner 1A12 is set for the selected rate by means of the front panel DATA RATE SEL (MB) switch (1A12S4). The local OCU's determine whether the orderwire signal is to be digital or analog, both must be

the same. At Digital data combiner 1A12, OW SEL switch 1A1251 must be set to DGTL or ANLG position according to the orderwire mode selected.

(1) In the transmit direction, when operating in digital orderwire mode, the digital orderwire signals (DOW and DVOW) and the data signal are combined in 1A12 and the combined signal is adjusted to the level required by the transmitter modulator circuits. For analog orderwire mode (AVOW), the orderwire signal is sent to orderwire assembly 1A13. In 1A13 it is processed as described in paragraph 2-8. In analog orderwire mode, there are no digital orderwire signals to combine with the data signal and the output from 1A12 to the transmitter circuits consists of the data signal only. The data signal and the analog orderwire signal are combined in module 1A4, as described in paragraph 2-10.

(2) In the receive direction, the radio signal

from the remote site is detected in the receiver and the recovered data/orderwire signal is routed to 1A12 through 1A13. In 1A12, the data and orderwire signals are separated, retimed, regenerated, and demultiplexed (digital orderwire), then routed to the DGM and OCU. For analog orderwire, the AVOW signal is routed to 1A13.

(3) The signals use in digital data combiner 1A12 block diagram descriptions are listed below. Status and alarm signals have a not bar, (e.g., CLB, to indicate that logic 0 is the active state and logic 1 is the inactive state). Thus, when LOOP TEST switch 1A12S3 is in the OFF or RADIO position,  $\overline{\text{CLB}}$  is logic 1 (inactive). When S3 is in the DGM position, CLB is logic 0 (active). FR FAIL is logic 0 normally and goes to logic 1 (fault) when the from radio data signal fails. For the OW SEL switch (1A1251), signal AVOW/DVOW is logic 1 for ANLG (which selects AVOW) and logic 0 for DGTL (which selects DVOW).

<u>Mnemonic</u>	<u>Meaning</u>
$\overline{\text{AVOW/DVOW}}$	Signal from OW SEL switch 1A12S1
$\overline{\text{BFRD DATA}}$	Buffered data signal from DGM
$\overline{\text{BFRD TMG}}$	Timing signal for $\overline{\text{BFRD DATA}}$ signal
$\overline{\text{BLB}}$	Signal from LOOP TEST switch 1A12S3
$\overline{\text{CDOW FAIL}}$	Data status signal from 1A12A1
$\overline{\text{CLB}}$	Signal from LOOP TEST switch 1A12S3
CLOCK	32 KHz clock for retimed data from radio CVDOW signal
CVDOW	Multiplexed DVOW and DOW signals
CVDOW RPLL FAIL	Status signal for 1A12A6



<u>Mnemonic</u>	<u>Meaning</u>
DATA IN	Data signal from DGM
DATA OUT	Retimed signal to DGM
DGMDEF	Status signal for from DGM data signal
DOW	Digital OW signal (2 kb/s)
DOW DEMUX DATA	Demultiplexed DOW signal from radio
DOW DEMUX TMG	Demultiplexed DOW signal timing
DRPLL FAIL	Status signal for 1A12A5
DSCRM DATA	Descrambled Output data
DSCRM FAIL	Status signal for descrambled data
DSCRM TMG	Timing signal for descrambled data
DT FAIL	Status signal for from radio data
DVOW	Digital OW signal (16 kb/s)
DVOW DEMUX DATA	Demultiplexed DVOW signal from radio
DVOW DEMUX TMG	Timing signal for DVOW DEMUX DATA
EQP FAULT	Status signal for data and timing
FR FAIL	Status signal for from radio signal
HBTR	Status signal from OW SEL switch (S1)
OWDMX FAIL	Status signal for 1A12A7
RCVRD DATA	Recovered (sliced and retimed) data from radio before descrambling
RCVRD TIMING	Timing signal for RCVRD DATA
RECOVERED AVOW	Filtered AVOW signal from radio
REGEN DATA	Sliced, retimed data signal from radio
SCRM DATA	Scrambled data to radio
SCRM FAIL	Status signal for scrambled data
SCRM TMG	Timing signal for scrambled data
SLICED CVDOW	Sliced from radio CVDOW
SLICED DATA	Sliced from radio data before retiming
SLICER FAIL	Data slicer status signal for 1A12A6
TMG IN	Timing signal for DATA from DGM
TMG OUT	Timing signal for retimed DATA To DGM
TR FAIL	Status signal for to radio data signal

(4) Digital data combiner 1A12 uses the plug-in components listed in the chart below and associated chassis-mounted connectors and components. Module A1, and parts of A3 and A4 are used for cable-to-radio (transmit) functions; part of modules A3 and A4, and modules A5 through A8 are used for radio-to-cable (receive) functions.

<u>Ref Desig</u>	<u>Description</u>
A1	Digital OW multiplexer
A2	Combiner, alarm-status
A3	Digital randomizer
A4	Digital buffer interface
A5	Digital traffic retimer
A6	Digital OW retimer
A7	Digital OW demultiplexer
A8	Digital regenerator

(5) Front panel switches provide control of operating modes of digital data combiner 1A12. The OW SEL switch (1A12S1) is in the DGTL position for digital orderwire (DOW and DVOW) and in the ANLG position for analog orderwire (AVOW). The DATA RATE SEL (MB) switch (1A12S4) is set to the selected data rate. The AVOW (1A12S2) and LOOP TEST (1A12S3) switches are used for test and maintenance functions. For normal operation, 1A12S2 is in NORM position and 1A12S3 in OFF (NORMAL) position.

b. Cable-to-Radio Circuits. The data and timing signals from the DGM and the digital orderwire (DOW and DVOW) or analog orderwire (AVOW) signals from the OCU and DLED are applied to the cable-to-radio circuits of digital data combiner 1A12 (fig. 5-8.2).

(1) Module A1 processes only digital orderwire signals. When the OW SEL switch is in the ANLG position, module A1 is not used and its operation is inhibited. In the digital orderwire mode of operation (OW SEL in DGTL position), the digital orderwire signals are applied to digital orderwire multiplexer 1A12A1, where they are converted from balanced to TTL level.

Module A2 provides status and fault monitoring functions for all circuits.

Paragraphs b and c provide descriptions of main signal paths in 1A12. Functional block diagrams of cable-to-radio and radio-to-cable circuits of 1A12 are provided in paragraphs 2-5.1 and 2-6.1.

The DOW signal is retimed and conditioned (para 2-5.1a) and the DOW and DVOW signals are multiplexed into a single 32 kb/s signal (CVDOW). The DOW, DVOW and clock signals are monitored to generate a status signal (CDOW FAIL). The CVDOW signal is routed to module A4.

(2) The balanced data and timing signals are applied to digital buffer interface 1A12A4 where they are converted to TTL level. They are then routed to module A3 where they are processed. In the transmit mode, at module A3 data is scrambled for application to digital interface buffer 1A12A4. Timing in the transmit mode is controlled by a phase lock loop that monitors differences in phase.

(3) In module A4, the data signal is retimed. The CVDOW signal from module A1 is gain adjusted. The gain adjustment varies according to the data bit rate in effect and is controlled by the DATA RATE SEL (MB) switch. The data and digital orderwire signals are then combined in a linear sum amplifier and routed to the transmitter modulator circuits.

(4) When operating in the analog orderwire mode, the OW SEL switch is in the ANLG position. The transmit analog orderwire signal (AVOW) is applied to digital orderwire retimer 1A12A6. In module A6 the AVOW signal is level adjusted and transformer coupled to orderwire assembly 1A13. With the OW SEL switch in ANTI' position, if the AVOW switch (1A12S2) is placed in BYPASS position, an inhibit signal is applied to the retiming circuit in module A4 and the data signal to the radio is cut off.

(5) Module A4 contains an electronic switch (cable loopback) that is controlled by a front panel manual switch (LOOP TEST, 1A12S3). When the LOOP TEST switch is placed in DGM position this switch is enabled. The data signal from the DGM is then routed through the cable loopback switch and returned to the D;M. This allows the local DCM to test the cable connection. For cable loopback mode, the data signal from the DC41 is still sent through the normal path to the transmitter. However, the from radio data signal is cut off and not used. The orderwire signal (digital or analog) is not affected by cable loopback mode; it is processed and routed in the normal manner.

c. Radio-to-Cable Circuits. The from radio signal consisting of the recovered data and orderwire signals is applied to digital regenerator 1A12A8 (fig. 5-8.3).

(1) The composite data/orderwire signal is amplified in module A8, then sliced. The balanced data signal from module A8 is converted to TTL level in

digital traffic retimer 1A12A5. The data signal is then regenerated and retimed. A clock signal is extracted from the data signal by the action of a phase lock loop to generate the cable data timing signal. The retimed data and the clock signal are routed to module A3. The regenerated data signal is also returned to module A8 for use in the orderwire extraction circuits. At module A3 the data signal is descrambled and retimed. Descrambled data and timing are routed to module A4. In A4 the data signal is retimed and the data and clock signals are routed through line drivers to the local DGM.

(2) When the LOOP TEST switch is placed in RADIO position, the radio loopback switch is enabled. The from radio data is then routed through the radio loopback switch to the transmitter circuits and returned to the remote radio site. The from radio data signal is still processed as described in (1) above but the data signal from the local DGM is cut off and not used. Orderwire signal processing is not affected.

(3) In module A8, the amplified from radio data signal is passed through a low pass filter to remove high frequency data component and is then applied to a subtractor. The regenerated, retimed data signal from module A5 is passed through a low pass filter, a multiplier and an AGC circuit and then applied to the subtractor circuit. In the subtractor circuit, the filtered data only signal from A5 is subtracted from the composite data/ orderwire signal leaving the orderwire signal as the output. In analog orderwire mode, this is the AVOW signal; it is routed through a low pass filter. The output AVOW signal is sent to orderwire module 1A13. In digital orderwire mode, the output of the subtractor is the CVDOW signal; it is sent to module A6.

(4) In digital orderwire retimer 1A12A6, the phase detector extracts a timing signal from the CVDOW signal in a phase lock loop to generate

the digital orderwire 32 kHz clock signal. The clock and retimed CVDOW signals are routed to module A7.

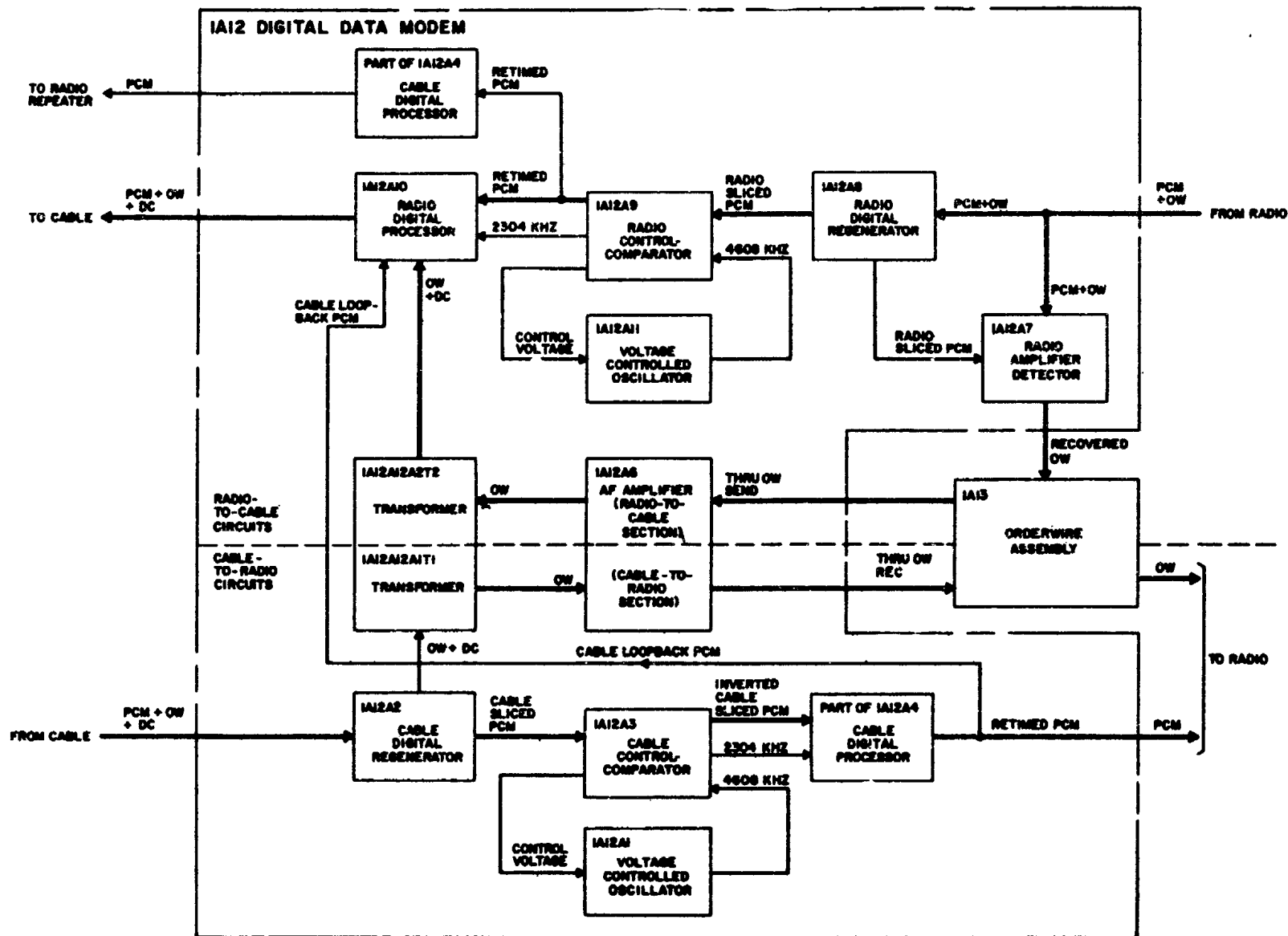
(5) Alternate bits in the CVDOW signal are DOW and DVOW. Those bits have known characteristics and are therefore detectable. The DOW detector in digital orderwire demultiplexer 1A12A7 adjusts the phase of the 16 kHz clock so that the DOW and DVOW demultiplexer each operate on the proper sequence of alternate bits. The DOW and DVOW data and timing signals are applied to line drivers and routed to the local OCU and DLED.

2-5. Digital Data Modem 1A12 Cable-to-Radio Circuits Functional Block Diagram Description (fig. 5-7 and 5-7.1)

The functional relationships between the cable-to-radio plug-in components and chassis circuits in digital data modem 1A12 are shown in figure 5-7 for the synchronous mode and in figure 5-7.1 for the asynchronous mode. Each plug-in component is functionalized and the main signal paths (heavy lines through each plug-in component and between plug-in components) are shown. In addition the control and alarm functions are shown. The operation of the synchronous mode plug-in components is described in a through f and the operation of the asynchronous plug-in components is described in a.1, b.1, and g.

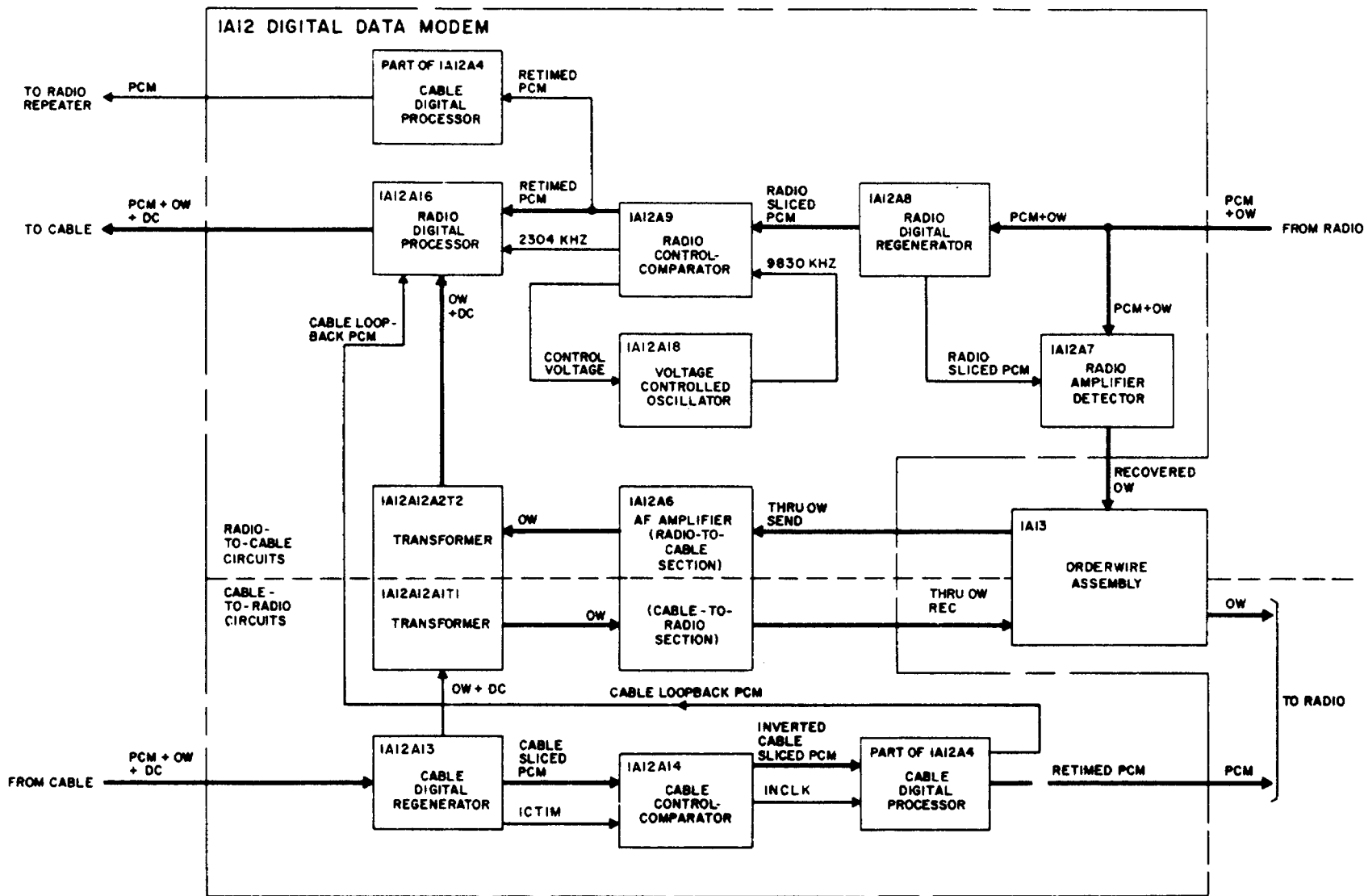
a. *Cable Digital Regenerator 1A12A2 (Synchronous Mode)* (fig 5-7 and 5-30).

(1) The input signal to cable digital regenerator 1A12A2 is designated FRCX (pcm/ orderwire/dc) Since the length of cable through which the signal is transmitted may vary up to a maximum of one mile, a cable simulation net



EL5820-695-35-TM-6

Figure 2-1. Digital data modem 1A12, overall block diagram, synchronous mode.  
Change 1 2-10.2



EL5820-695-35-C2-TM-1

Figure 2-1.1. Digital data modem 1A12, overall block diagram, asynchronous mode.  
Change 2 2-10.3

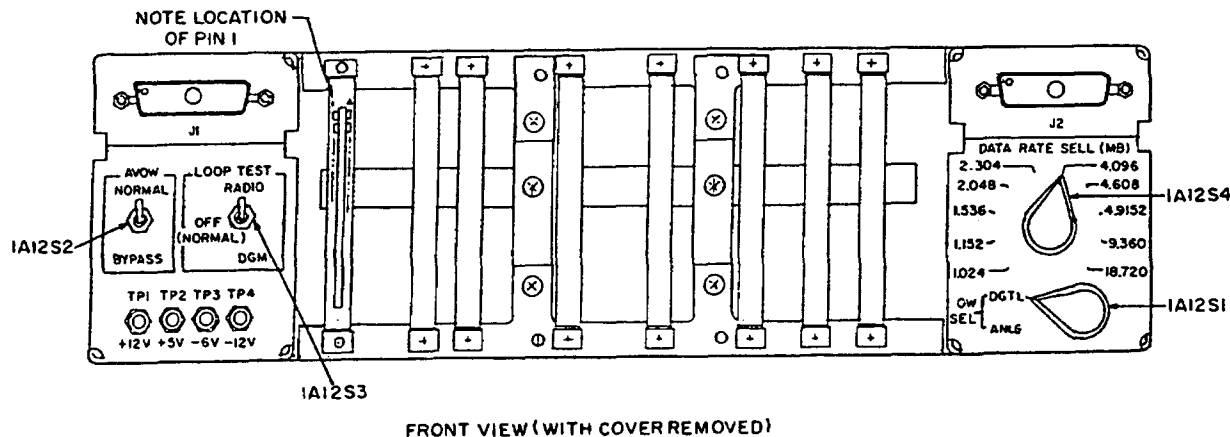
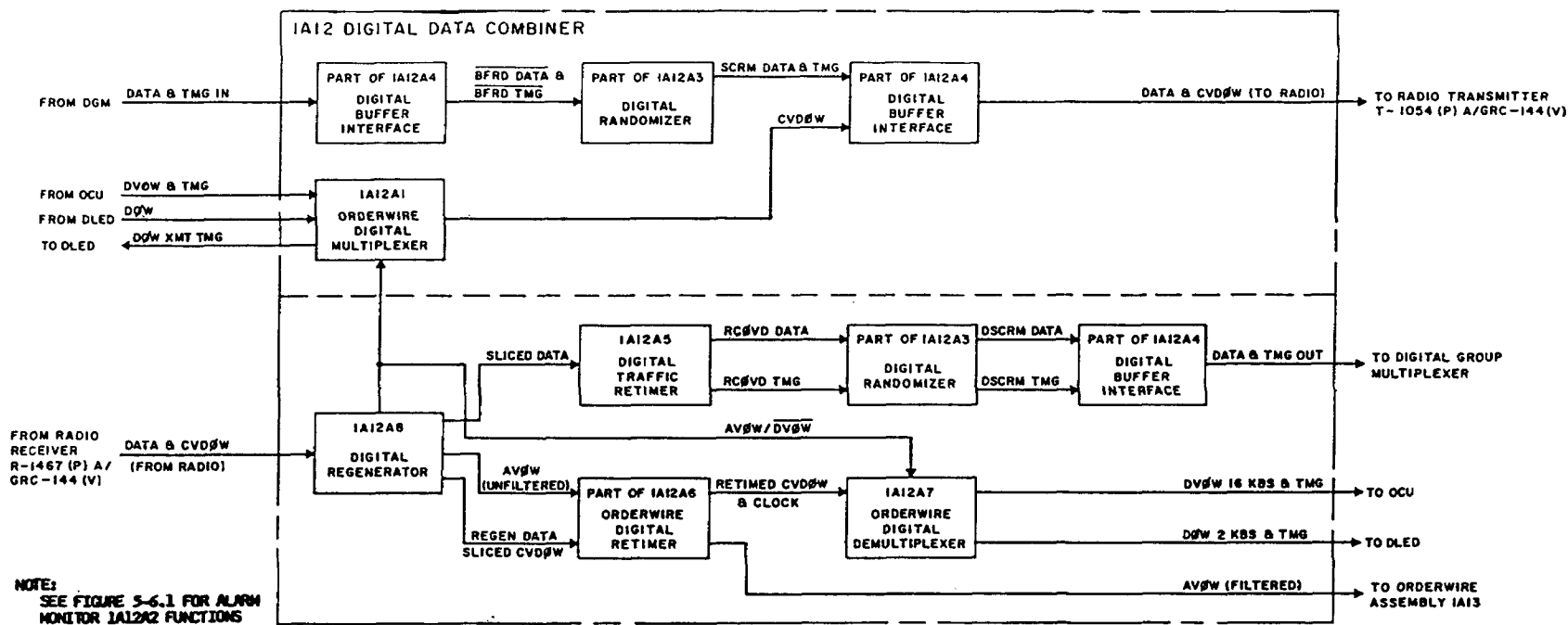


Figure 2-1.2. Digital data combiner 1A12 overall block diagram.  
Change 6 2-10.4

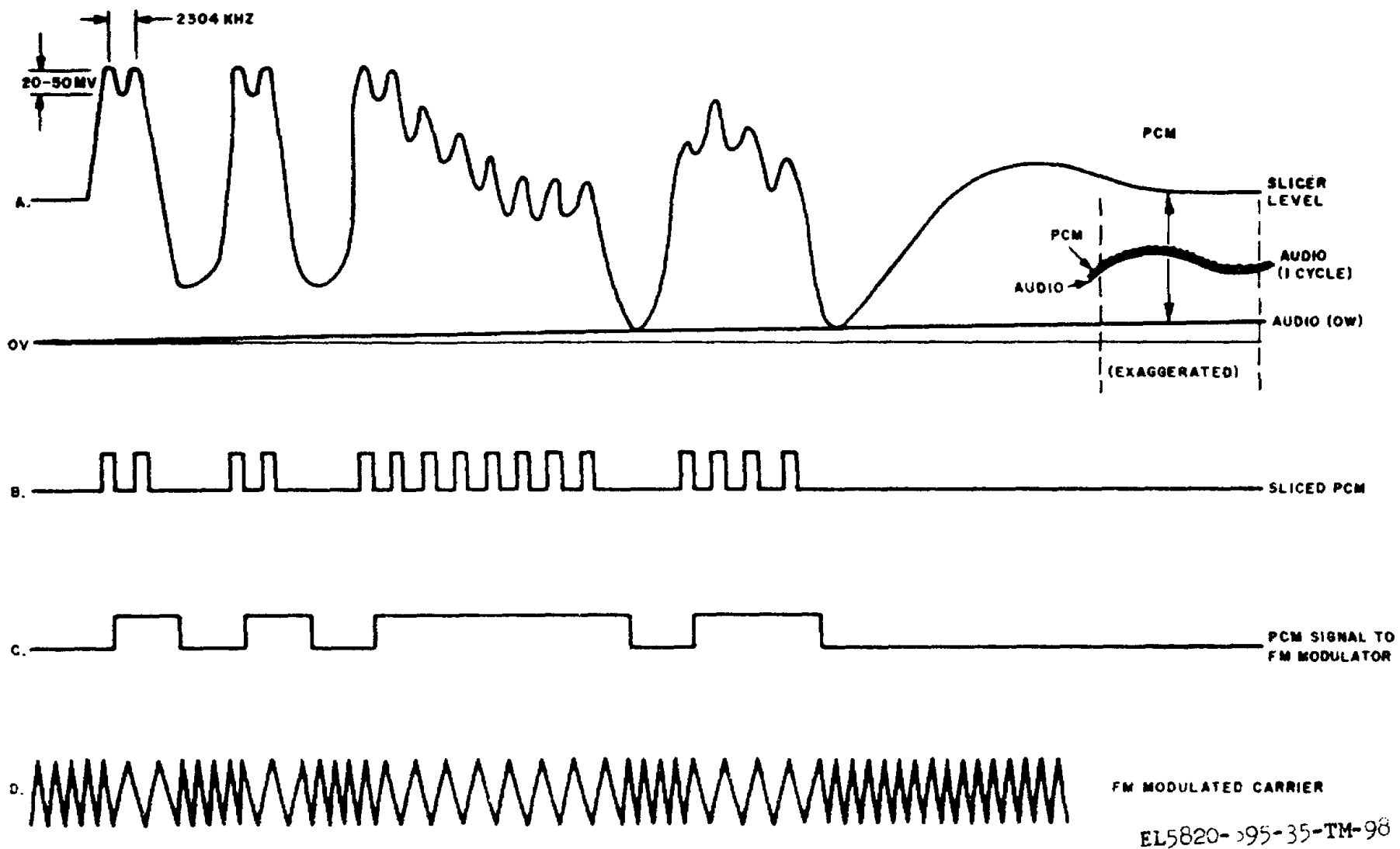


Figure 2-2. Cable digital regenerator 1A12A2, pcm signal waveforms, synchronous mode.  
 Change 1 2-11



work, variable in increments which provide attenuation equivalent to one-quarter mile of cable, is provided to terminate the line. This consists of three one-quarter mile sections which can be selected by the operator. The section or sections selected modify the input signals to an equivalent that would be delivered by one mile of cable.

(2) The original FRCX signal from the source end of the cable is comprised of a dc signal plus squared voltage pulses representing the one bits in the pcm modulation code. When the orderwire circuit is in use, the orderwire audio signal is the third component of the FRCX signal. This signal, at the input to 1A12A2, is greatly degraded in quality after transmission through one mile of cable (or equivalent). A typical input FRCX signal is illustrated in figure 2-2, waveform A.

(3) The pcm portion of the input signal is coupled to the cable simulation networks and transformer T1. Transformer T1 provides a voltage gain of two. The dc is blocked from this path by capacitor C1 and the orderwire is rejected by highpass filter C1/L7. Overvoltage protection for following amplifiers is provided by diodes CR1-CR4 which limit the maximum amplitude of the input signal. The orderwire and dc signals go through low pass filter L1, L2 and L3 and are sent to chassis mounted transformer 1A12A15AIT1 as the FRCX $\emptyset$ W signal.

(4) The pcm signal at the secondary of transformer T1 is degraded because of high frequency losses during cable transmission. The pcm voltage pulses are no longer clearly defined and square and are low in amplitude. Circuit Q1, of the 2304 kHz peaking circuit, amplifies the pcm voltage pulses to provide a more sharply defined signal. In the 2304 kHz peaking circuit, circuit Q1 is tuned to 2304 kHz which is the frequency used to time pcm voltage pulses for cable transmission. Circuit Q2, with a voltage gain of 35, then greatly increases the sharpness and definition of the pcm voltage pulses. The output of circuit Q2 is coupled through impedance matching emitter follower Q3 and transformer T2 to amplifier Q5A. Amplifier Q5A is a temperature compensated linear amplifier which further amplifies the signal. Peak detector circuit A7/Q8 rectifies the pcm signal output of amplifier Q5A and develops a filtered positive dc voltage across R40. The center arm of R40 is connected to the reference input of slicer A1. The pcm signal from Q5A also is connected to the other input of slicer A1. Slicer A1 is a high speed differential comparator. It produces a pulse output with a steep vertical rise for positive voltage transitions of the input and a sharp vertical drop for negative transitions. Thus,

the pcm is sliced into separate voltage pulses, logic ones, which represent the logic one bits in the pcm code as shown in figure 2-2, waveform B. The output of slicer A1 is zero for logic zero bits. The dc voltage developed by peak detector Q7/Q8 assures that the center of each voltage pulse corresponds to the peak of the pcm signal. The pcm signal, now designated 1CSPCM, is sent to cable control comparator 1A12A3 for retiming.

(5) The 1CSPCM signal is integrated by Q9 which develops a dc output signal as long as logic one bits keep occurring at the input. Lamp driver Q10 then provides a ground output and lamp DS1 lights to indicate traffic activity. In the absence of traffic, lamp DS1 does not light and signal 1CRFAIL, which goes to alarm monitor 1A12A5, switches to logic one.

#### *a.1. Cable Digital Regenerator 1A12A13, Asynchronous Mode (fig. 5-7.1 and 5-30.1)*

(1) The discussion of the FRCX signal given in paragraph 2-5 all) and (2) applies also to the asynchronous mode. The FRCX signal is illustrated in figure 2-2. 1. At the input, the pcm component of the composite FRCX signal is passed by high pass filter C12-L7 and the dc and orderwire components are routed into a second path through low pass filter L-7, L-10, L-11, R-9 s and C-35. The dc/orderwire signal, designated FRCXOW, is sent to chassis mounted transformer 1A12A12A1T1.

(2) In the pcm signal path, overvoltage protection for following circuits is provided by diodes CR5 and CR6. The signal then passes from terminal (T) to terminal (N), (passing through the variable cable equalizer via terminals (L) and (Y), if it is in the circuit), and goes through the fixed cable equalizer. Variable resistor R6 adjusts the low frequency response of the equalizer.

(3) At this point the signal is coupled through capacitor C22 to emitter follower Q4, the traffic monitor amplifier. The output of Q4, designated XCPCM, is routed through a coaxial cable to alarm monitor 1A12A15. Resistor R27 reduces the capacitive effect of the cable and prevents reflection of the signal back to Q4.

(4) An attenuator (resistors R12, R15 and R16) at the input of linear amplifier A4 reduces the input signal to prevent overloading A4. The gain of linear amplifier A4 is variable and is controlled by an agc signal developed in transistors Q1 and Q2. The output signal of A4 is coupled through a low pass

filter (R8, R5, C6, C7) to the base of Q2 and is also coupled through capacitor C10 to the base circuit of Q1. The base circuit of Q1 (CR2, R4, and C5) rectifies and filters the signal and provides, at the base of Q1, a dc signal which is proportional to the pcm signal amplitude. Diode CR3 bypasses the negative half-cycles of the signal. Transistors Q1 and Q2 comprise a voltage comparator with the reference voltage at the base of Q2 and the signal proportional voltage at the base of Q1. The signal at the base of Q2 is dc with the level adjustable by variable resistor R5. The output voltage from the collector of Q1 is coupled through capacitors C15 and C16 to linear amplifier A4. Resistor R17 provides an impedance match for the output of A4.

(5) The bipolar pcm signal is converted to standard logic (all logic ones are positive pulses) in the dual voltage comparators of A3. The pcm signal in the secondary of transformer T1 is connected through equalizing resistors (R30 and R33) to the noninverting inputs of the voltage comparators. A bias voltage (+0.3 vdc), developed by resistor R18 and diode CR7, is connected through equalizing resistors (R31 and R32) to the Inverting inputs. The pcm input signal to A3 is transformer coupled from A4, so the signals at pins 4 and 6 are 180 degrees out of phase. When the signal at pin 4 goes more positive than +0.3v (the signal on pin 6 is then negative), the output of the comparator goes positive and remains positive until the input signal falls below +0.3v. Thus the positive bipolar pulse is converted to a squared pulse. When the signal at pin 4 is negative (the negative bipolar pulse), the inverted signal at pin 6 is positive. The same action as before now occurs in the voltage comparator connected to pin 6, thus inverting and squaring the negative bipolar pulse. As the two voltage comparators operate alternately to convert and square the bipolar pulses, their outputs are combined in the OR-gate of A3 to provide the standard logic positive pulses in the same serial order as the original bipolar pulses. The output of A3 is sent through inverters A2C and A2A which provide the drive power for following circuits and reduce the loading on A3. The output of A2A, designated 1CSPCM, is routed to cable control comparator 1A12A14 and 4 to the integrator and lamp driver circuits.

(6) When the pcm signal is absent, the output of A2A is high (+5v), the base circuit of transistor Q5 has +5v applied at both sides, capacitor C32 has no charge and +5 vdc through R35 is applied to the base of Q5. With Q5 reverse biased and off, Q6 is off, lamp

DS1 is off and signal 1CRFAIL is logic 1 (Alarm). When the pcm signal is active, the output of A2A goes negative (ground) between logic ones. During these intervals (in effect, negative pulses), capacitor C32 charges through CR9 from the positive +5v supply, with negative polarity on the side connected to the base of Q5. Transistor Q5 is turned on and the +6v supply through resistor R36 and the emitter-collector circuit of Q5 forward biases Q6. Transistor Q6 and lamp DS1 are turned on and signal 1CRFAIL is logic 0 (normal).

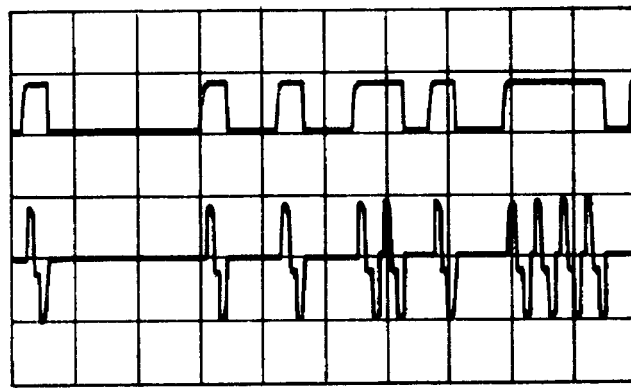
(7) The output signal of A3 is also transformer coupled to limiter Amplifier A1 in the clock generator circuit. The input circuit of the limiter amplifier is a crystal-controlled bandpass filter comprising the secondary of transformer T2, crystal Y1, capacitors C18, C19, and C23, resistor R20 and coil L9. The bandpass filter provides a 4915.2 kHz input to A1. The output of A1 is a signal of uniform amplitude at the clock frequency. Resistor R19 is the load resistor for A1; the signal developed across R19 is capacitor-coupled (C11) to buffer amplifier Q3. The output clock signal, designated 1CTIM, is passed through inverter A2B and routed to cable control comparator 1A12A14.

b. *Cable Control Comparator 1A12A3* (fig. 5-7 and 5-31).

(1) The function of cable control comparator 1A12A3 is to determine the phase difference between the clock and data signals and from this information to generate a control signal. The control signal is then used to shift the phase of the clock signal until data and clock are in phase. Cable control comparator 1A12A3 receives the 1T4608 signal (4608 kHz cable-to-radio clock) from 4608 kHz vco 1A12A1 and the 1CSPCM signal (cable sliced pcm) from cable digital regenerator 1A12A2. The 1CSPCM signal is inverted by inverter A3B. The inverted signal (OCSPCM) is sent to cable digital processor 1A12A4 and is also connected to the trigger input of flip-flop A7B which divides the signal by two. The output of A7B is connected to both inputs of AND gate A11B, directly to pin 6 and through delay inverters A11C, D and A to pin 5 (E24). Because of the propagation delay through the three inverters, the input signals to A11B are simultaneously logic one only for a short time immediately following a positive transition at the output of flip-flop A7B (1DF waveform, fig. 5-31). The resulting logic zero output of A11B sets phase comparator A10A and B. Tracing this action back to the input signal

(1CSPCM), It can be seen that it occurs at the positive going or leading edge of a data logic one. Generation of the reset pulse for the phase comparator is discussed in the following paragraph.

(2) Input signal 1T4608 (4608 kHz cable-to-radio clock) is divided by two flip-flop A7A. The logic zero output of A7A is connected to



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■ Figure 2-2.1. Cable digital regenerator 1A12A13, pcm signal waveform, asynchronous mode.

the trigger input of narrow clock pulse generator A5 which is a monostable multivibrator. It generates a negative 120 nanosecond output pulse for each input pulse. This signal is inverted by inverter A3A and designated 1N2304 (2304 kHz cable-to-radio clock). It is sent to cable digital processor IA12A4 and is also connected to inverter A3D. The output A3D is connected to both inputs of AND gate A2B, directly to pin 6 and through delay inverters A2C, D and A to pin 5. Because of the propagation delay through the three inverters, the input signals to A2B are simultaneously logic one only for a short time immediately following a positive transition at the output of A3D (1CP waveform, fig. 5-31). The resulting logic zero output of A2B resets phase comparator A10A and B. Tracing this action back to the input signal (1T4608), it can be seen that it occurs at the positive-going or leading edge of clock pulses. The difference in time between set (1DP, data pulse) and reset (1CP, clock pulse) pulses to the phase comparator is then a measure of the phase difference between the data input, 1CSPCM and clock input, 1T4608.

(3) The output (E24) of the delay circuit in the data pulse generator ((1) above) is also connected to 48 channel baud generator A1 which is a monostable multivibrator. It generates a negative output pulse each time the input signal goes to logic zero. The duration of the negative pulse is adjusted so that the total time from the start to 1DP to the end of the baud pulse is 434 nanoseconds. This signal is inverted by inverter A3C and applied as one input (1BP) to AND gate A6A (1BP waveform, fig. 5-31).

(4) The output signal of the phase comparator (1FP) (1FP waveform, fig. 5-31), which represents the phase difference between data and clock signals, is inverted by inverter A6B. The output signal of inverter A6B (1PP waveform, fig. 5-31) causes the positive pulse generator to generate the positive pulse input to differential integrator AS. The inverter output of the 48 channel baud generator (1BP) and the output of the phase comparator (1FP) are applied to AND gate A6A. The output of AND gate A6A (1NP waveform, fig. 5-31) causes the negative pulse generator to generate the negative pulse input to differential integrator A8. Thus, at the start of each data pulse (corresponding to a logic one bit in the data signal) 1DP goes Negative, 1FP goes negative, and 1PP goes positive. This condition holds and a positive pulse input to the integrator is generated until 1CP goes negative. When 1CP goes negative, 1FP goes positive and since 1BP is positive, 1NP goes

negative. This condition holds and a negative pulse input to the integrator is generated until 1BP goes negative. When zero bits occur in the input signal (1CSPCM), 1DP remains high and the phase comparator flip-flop is not set, so 1FP remains high. Thus, 1PP remains low and positive pulses to the integrator are not generated. Also 1BP remains low, so 1NP is high and negative pulses to the integrator are not generated.

(5) The output signal of differential integrator A8 is connected to the frequency control input of 4608 kHz vco 1A12A1. When the input to A8 is a positive pulse, the output is a negative-going change in voltage. When the input is a negative pulse, the output is a positive-going change in voltage. This means that the output voltage starts to rise (or fall) at a fixed rate of change (slope). When clock and data are in synchronism, positive and negative pulse inputs to A8 are approximately equal, and the positive and negative-going changes in output voltage cancel since the slopes are equal. These low amplitude excursions of the output signal are filtered at the input of 1A12A1 and the output frequency remains constant. When the positive pulses inputs to A8 are longer than the negative pulses, the negative-going output caused by the positive pulse is not entirely cancelled by the return in the zero direction caused by the following negative pulse. The net result is that the signal remains negative and will go more negative as long as this condition (longer positive pulses) holds. However, the negative output signal causes the frequency of 1A12A1 to increase, clock pulse 1CP then occurs sooner and positive pulses are shortened and the length of negative pulses is increased. This action and reaction occurs until positive and negative pulses are equal. When the negative pulses are longer than positive pulses, the same kind of action in the opposite direction takes place. The output of A8 goes positive, clock frequency is decreased and clock pulses 1CP is delayed. This shortens the negative pulses. The result is that the output of A8 always produces a frequency change at 1A12A1 that tends to equalize positive and negative pulses and when equality is established to maintain it. When the data signal has logic zero bits, neither positive nor negative pulses are sent to integrator A8, however, it has a long time constant which holds its output to bridge over these short intervals.

(6) The output of differential integrator A8 is also connected to positive/negative clamp detector A9. Normally, the output of differential

integrator A8 is close to zero volts as it holds the clock signal in synchronism with data. The output of A9 is then low. The low output from A9 is inverted twice by the lamp driver (inverters A10C and A4A), so signal 1CCFAIL is low (logic zero) and lamp DS1 is lighted. However, when correction is required, the output of A8 can vary from +3 volts to -3 volts. Positive/negative clamp detector A9 output signals of A8 that exceed the indicated limits. When either limit is exceeded the output of A9 goes high. This signal, inverted twice by the lamp driver, is sent to alarm monitor 1A12A5 and also turns off lamp DS1.

**b.1 Cable Control Comparator 1A12A14, Asynchronous Mode**(fig. 5-7.1 and 5-31.1) In the asynchronous mode, the cable control comparator 1A12A14 retimes the 1CSPCM signal and monitors the pcm traffic signal and the clock signal.

(1) The traffic signal 1CSPCM is applied to the D input of data retiming flip-flop A1A and the clock signal 1CTIM is applied to the T input. Flip-flop A1A triggers on the positive-going transitions of clock pulses. Each time A1A is triggered, the logic 0 output (pin 6) takes on the logic state of the signal present at input D (pin 2). Thus the half-baud input data pulses are converted to full baud at the output of A1A. The output data signal is precisely and uniformly retimed because triggering of A1A is controlled by the clock signal 1CTIM. This signal, which is inverted since it is taken from the 0 output of A1A, is designated OCSPCM and is routed to cable digital processor 1A12A4.

(2) The clock signal 1CTIM is inverted by clock inverter A2A which also reshapes the clock pulses to standard logic levels. The output signal, designated 1NCLK is routed to cable digital regenerator 1A12A4.

(3) The two output signals OCSPCM and 1NCLK are monitored by the traffic detector A3A and the clock detector A3B. The detector circuits are the same and their operation is the same. The circuit is a monostable multivibrator with an AND gate trigger input. Since the AND gate has one input (pins 1 and 9) tied permanently to logic 1, triggering occurs regularly as long as a traffic (or clock) signal is present. Each time the detector is triggered, the output (pins 13 and 5) goes to logic 1 and remains at logic 1 for a time determined by resistor R23 and capacitor C6 (or R6-C7). The time is relatively long compared to the time between trigger inputs. So as long as the OCSPCM and 1NCLK signals are active, A3A and A3B present logic 1 inputs to A2C. The output of A2C is logic 0; this is inverted to logic 1

(+5v) by A2D. The +5v applied to the base turns on transistor Q1, so the collector voltage is zero. Signal 1CCFAIL is logic 0 (normal) and lamp DS1 is lighted. If either the traffic or the clock signal fails, the corresponding detector times out and its output goes to logic 0. The outputs of A2C and A2D are then logic 1 and logic 0, respectively Transistor Q1 is cut off, lamp DS1 turns off and the 1CCFAIL signal is logic 0 (alarm). This signal is routed to the alarm monitor 1A12A15.

**c. Cable Digital Processor 1A12A4** (fig. 5-7 and 5-32). The cable-to-radio circuits of cable digital processor 1A12A4 receive the inverted cable sliced pcm signal (OCSPCM) from 1A12A3 (or 1A12A14) and retime it, using cable-to-radio-clock signal (1N2304 or 1NCLK) from 1A12A3 (or 1A12A14). The retimed pcm signal levels are then converted to logic levels required by the radio modulator circuits.

(1) The cable sliced pcm signal (OCSPCM) is applied to data retimer flip-flop A2A through inverter A5A. The cable-to-radio clock signal is applied to data retimer flip-flop A2A through digital buffer 1. Data retiming flip-flop A2A triggers on the positive-going transition of clock (trigger) pulses. Each time A2A is triggered (waveform C, fig. 5-32), the logic one output (pin 5) takes on the logic state of the signal present at input D (pin 2) at that, time. The logic state of output pin 6 is always the complement (logical opposite) of the output at pin 5. The output state of A2A is then maintained until the next trigger pulse. As a result, the half-baud data pulses at the D input (typical waveform B, fig. 5-32) are converted to full baud pulses at the output (waveform D, fig. 5-32). The output signal of A2A is inverted since it is taken at the logic zero output (pin 6). It is inverted again by inverter A4A (waveform E, fig. 5-32), converted to voltage levels required by the modulator circuits and applied to the modulator circuits of Transmitter, Radio T-1054/GRC-144.

(2) The retimed pcm signal is also applied to alarm circuit 1. Each time monostable multivibrator A6 is triggered by the negative-going transition of a logic one from A4A, the output signal (pin 8) goes to logic one and holds for 72 microseconds (approximately). If A6 receives another trigger pulse before it times out (72 microseconds), the timing cycle starts over again. Thus, as long as pcm trigger pulses occur at least once every 72 microseconds, the output of A6 is held at logic one. The logic one (+5v) keeps Q1 forward biased and it provides a logic zero output. Lamp DS1 is lighted (green) and logic

zero is sent to alarm monitor 1A12A5 (or 1A12A15) to indicate the presence of the pcm signal. If the pcm signal fails, A6 times out and the output goes to logic zero Q1 is then cut off, lamp DS1 goes out and the output signal (ICRLFAL) is at logic one.

(3) When CABLE LOOP TEST switch 1A12A12A1S1 is in NORMAL position, the output signal of inverter A3B is logic zero, and the output signal of cable loopback sample gate A3C is logic zero. When CABLE LOOP TEST switch is in TEST position, the output of A3B provides a logic one at one input of A3C. The other two inputs are the pcm signal (typical waveform B, fig. 5-32) and the clock signal (waveform C, fig 5-32). Whenever both signals (waveforms B and C) are at logic one, the output signal of A3C is logic zero (waveform A, fig. 5-32). Thus, the output of A3C is logic zero whenever the pcm signal is logic one but the duration of the logic one is reduced to 80 nanoseconds by the 80 nanosecond clock pulses. The output of A3C (OCLPCM) is applied to the cable system through radio digital processor 1A12A10 (or 1A12A16) in the radio-to-cable circuits and is used to test the cable system.

*d. Orderwire and Direct Current Path* (fig. 5-7 and 5-29) The from cable orderwire (FRCXOW) and direct current signal are separated from the pcm signal in cable digital regenerator 1A12A2 (a above). The two signals are then routed to the primary of transformer 1A12A12A1T1

(1) The ow portion of the signal is coupled to the secondary of transformer 1A12A12A1T1 and the THRU OW RECEIVE LEVEL ADJ potentiometer to the cable-to-radio circuits portion of amplifier 1A12A6. The THRU OW RECEIVE LEVEL ADJ control (1A12A12A1R1) on the front panel of digital data modem 1A12 is used to set the ow input level to 1A12A6.

(2) The direct current portion of the signal from 1A12A2 is routed to the radio-to-cable circuits of 1A12 through the primary of transformer 1A12A12A1T1, inductor 1A12A12A1LI and capacitors C1 and C2 of the orderwire filter, and a jumper connection through FAULT LOCATOR POWER SUPPLY INTERCONNECT J20 and plug P3 on top of electrical equipment cabinet IA15. The from cable ow (FRCXOW) signal is removed from the direct current path by the orderwire filter. The direct current path is connected

to the cable system through the radio-to-cable circuits (para 2-6e).

e. *AF Amplifier 1A12A6 (fig. 5-7 and 5-34).*

The cable-to-radio circuits of af amplifier 1A12A6 amplify the orderwire signal. The cable-to-radio circuits of 1A12A6 are comprised of an input amplifier, a low pass filter with cutoff frequency of 2000 Hz, and a power amplifier. The amplified output cable receive orderwire (CCROW) of 1A12A6 is applied to the "thru ow rec" input of orderwire assembly 1A13. A level detector circuit at the output generates a dc voltage when the orderwire signal is active. The dc voltage is available at a test point for monitoring and testing purposes.

f. Alarm Monitor Synchronous Mode 1A12A (fig. 5-7 and 5-33). Alarm monitor 1A12A5 receives alarm signals from other circuits of digital data modem 1A12 and uses logic combinations of these alarm signals to generate traffic and functional alarm indications for the radio-to-cable and cable-to radio circuits. The summarized alarm signals activate green and red status indicators, a major alarm relay, and control a bypass orderwire relay. The cable-to-radio circuits of alarm monitor 1A12A5 control the CABLE-TO-RADIO MODEM indicator on meter panel assembly 1A16A4 and the shelter mounted traffic in indicator. Two kinds of signals are monitored by the cable-to-radio circuits-functional alarm signals from 1A12A2 (1CRFAIL), 1A12A3 (1CCFAIL,) and 1A12A4 (1CRFAIL); and the cable traffic signal (XCPCM) from 1A12A2. When a functional failure occurs in 1A12A4, alarm signal 1CRLFAIL, is activated (logic one). Since the pcm signal is processed in sequence in 1A12A2, 1A12A3 and 1A12A4, a functional failure in 1A12A3 causes both 1CCFAIL and 1CRLFAIL signals to switch to logic one, and a functional failure in 1A12A2 causes all three signals to switch to logic one. Also, if there is a failure of the cable traffic signal, all three functional failure signals switch to logic one because each circuit (1A12A2, 1A12A3 and 1A12A4) then loses the pcm signal. Alarm monitor 1A12A5 uses these four inputs to the cable-to-radio circuits to distinguish which kind of failure has occurred, functional failure or cable traffic failure.

(1) *Cable Traffic Normal.* When cable traffic (XCPCM) is being detected, the output of inverter A3E is logic zero (high) and lamp driver Q10 is turned on. The logic zero from A3E is inverted by A3F and lamp driver Q11 is turned off. Output OCTFL is logic one, 1CTFL is logic zero and the traffic in indicator is lighted green.

(2) *Cable Traffic Failure.* When loss of the cable traffic signal (XCPCM) occurs, the output of inverter A3E is low and lamp driver Q10 is turned off. The low from A3E is inverted by A3F and lamp driver Q11 is turned on. Output OCTFL is logic zero, 1CTFL is logic one and the traffic in indicator is lighted red.

(3) *No Functional Failure.* The 1CRFAIL, 1CCFAIL and 1CRLFAIL signals are inverted by inverters A7B, A7C and A7F, and the resulting output signals are applied to negative OR gate A1B. When there is no functional failure, these signals are all low (logic zero) and all inputs to A1B are high. A1B then applies a low (logic zero) to NAND gate A4C.

(4) *Functional Failure.* If any functional failure exists, A1B has at least one input which is low. If a cable traffic failure occurs, all inputs to A1B are low. In either case, A1B applies a high (logic one) to A4C.

(5) *Cable Traffic Normal-No Functional Failure.* When cable traffic is normal and there is no functional failure, the conditions of (1) and (3) above exist and operation is as follows:

(a) The inputs to A4C are low from A1B and high from A3E. The output of A4C is then high, and as a result, lamp driver Q9 is turned on and output signal 1CFFL is logic zero. The output of A4C, inverted to a low by A3C, turns off lamp driver Q8 and output signal OCFFL is logic one. The CABLE TO RADIO MODEM indicator is lighted green.

(b) The output of negative OR gate A2A is applied to NAND gate A2B. The logic action at A2B depends on the operating mode in use. When Radio Set AN/GRC-144 is being used in radio repeater mode, the cable-to-radio circuits of digital data modem 1A12 are not used and signal ORRM is logic zero. The output of A2B is then always high because it is inhibited by the logic zero (ORRM) at pin 5. This prevents erroneous application of a cable-to-radio fault indication to negative OR gate A1A when in radio repeater mode. When Radio Set AN/GRC-144 is being used in the cable terminal mode, signal ORRM is logic one. NAND gate A2B then has logic one at pin 5 and it acts as an inverter for the -signal at pin 6. When a functional failure occurs, negative OR gate A2A has high inputs from A4C and A3E and it applies a logic zero (low) to A2B. The low is inverted to high by A2B, and applied to negative OR gate A1A. This is the

summary alarm output signal for cable-to-radio circuits (para 2-6h).

(c) The output of A3E is high, lamp driver Q10 is turned on and output signal 1CTFL is logic zero. The high from A3E is inverted to low by A3F, lamp driver Q11 is turned off and output signal OCTFL is logic one. The traffic in indicator is lighted green.

(6) *Cable Traffic Normal-Functional Failure.* When cable traffic is normal and there is a functional failure, the conditions of (1) and (4) above exist and operation is as follows:

(a) The inputs to A4C, from both A B and A3E, are high and the output is low Lamp driver Q9 is turned off and output signal 1CFFL is logic one. The output of A4C, inverted to high by A3C, turns on lamp driver Q8 and output signal OCFFL is logic zero. The CABLE TO RADIO MODEM indicator is lighted red

(b) Negative OR gate A2A receives a low from A4C and its output is high ((5)(b) above). The high from A2A is inverted to low by A2B and applied to A1A (para 2-6h).

(c) The output A3E is still high and Q10, Q11, 1CTFL and OCTFL are as explained in (5)(c) above The traffic in indicator is still lighted green.

(7) *Cable Traffic Failure.* When a cable traffic failure occurs (loss of the XCPCM signal), all functional failure signals are also affected and change to logic one (high). The conditions of (2) and (4) above then exist and operation is as follows:

(a) The inputs to A4C are high from A1B and low from A3E. The output of A4C is high and operation is as explained in (5)(a) above.

(b) Negative OR gate A2A receives a low from A3E and its output is high. The high output from A2A is inverted to low by A2B and applied to A1A (para 2-6h).

(c) The output of A3E is low, lamp driver Q10 is turned off and output signal 1CTFL is logic one. The low from A3E is inverted to high by A3F; lamp driver Q11 is turned on and output signal OCTFL is logic zero. The traffic in indicator is lighted red.

g. *Alarm Monitor 1A12A15, Asynchronous Mode (fig. 5-7.1 and 5-33.1).* Alarm monitor 1A12A15 receives alarm signals from other circuits of digital data modem 1A12 and uses logic combinations of these alarm signals to generate traffic and functional alarm

indications for the radio-to-cable and cable-to-radio circuits. The summarized alarm signals activate green and red status indicators, a major alarm relay, and control a bypass orderwire relay. The cable-to-radio circuits of alarm monitor 1A12A6 control the CABLE-TO-RADIO MODEM indicator on meter panel assembly 1A16A4 and the shelter mounted traffic in indicator. Two kinds of signals are monitored by the cable-to-radio circuits functional alarm signals from 1A12A13 (1CRFAIL), 1A12A14 (1CCFAIL), and 1A12A4 (1CRLFAIL), and the cable traffic signal (XCPCM) from 1A12A2: When a functional failure occurs in 1A12A4, alarm signal 1CRLFAIL is activated (logic one). Since the pcm signal is processed in sequence in 1A12A13, 1A12A14 and 1A12A4, a functional failure in 1A12A14 causes both 1CCFAIL and 1CRLFAIL signals to switch to logic one, and a functional failure in 1A12A13 causes all three signals to switch to logic one Also, if there is a failure of the cable traffic signal, all three functional failure signals switch to logic one because each circuit (1A12A13, 1A12A14 and 1A12A4) then loses the pcm signal. Alarm monitor 1A12A15 uses these four inputs to the cable-to-radio circuits to distinguish which kind of failure has occurred--functional failure or cable traffic failure.

(1) *Cable Traffic Normal.* When cable traffic (XCPCM) is being detected, and signal OPSALM is normal (high), both inputs to NOR gate A7A are high and its output is low. The output of inverter A6A is then logic zero (high) and lamp driver Q10 is turned on. The logic zero from A6A is inverted by A6B and lamp driver Q11 is turned off. Output OCTFL is logic one, 1CTFL is logic zero and the traffic in indicator is lighted green.

(2) *Cable Traffic Failure* When loss of the cable traffic signal (XCPCM) occurs, or signal OPSALM is logic 0, the output of inverter A6A is low and lamp driver Q10 is turned off. The low from A6A is inverted by A6B and lamp driver Q11 is turned on. Output OCTFL is logic zero, 1CTFL is logic one and the traffic in indicator is lighted red.

(3) *No Functional Failure.* The 1CRFAIL, 1CCFAIL and 1CRLFAIL signals are inverted by inverters A9B, A9A and A9C, and the resulting output signals are applied to NOR gate A8B. Signal OPSALM is inverted successively by inverters A9F and A9D The output of A9D is connected to NOR gates A7A and A8B When there is no functional failure, input signals 1CRFAIL, 1CCFAIL and 1CRLFAIL are low (logic zero) and OPSALM is high (logic zero) and all inputs to A8B are high. A8B then applies a low (logic zero) to NAND gate A7B.



(4) *Functional Failure.* If any functional failure exists, A8B has at least one input which is low. If a cable traffic failure occurs, all inputs to A8B except the input from A9D are low. In either case, A8B applies a high (logic one) to A7B.

(5) *Cable Traffic Normal-No Functional Failure.* When cable traffic is normal and there is no functional failure, the conditions of (1) and (3) above exist and operation is as follows.

(a) The inputs to A7B are low from A8B and high from A6A. The output of A7B is then high, and as a result, lamp driver Q9 is turned on and output signal 1CFFL is logic zero. The output of A7B, inverted to a low by A6D, turns off lamp driver Q8 and output signal OCFFL is logic one. The CABLE TO RADIO MODEM indicator is lighted green.

(b) The output of NOR gate A7C is applied to NAND gate A2B. The logic action at A7D depends on the operating mode in use. When Radio Set AN/GRC-144 is being used in radio repeater mode, the cable-to-radio circuits of digital data modem 1A12 are not used and signal ORRM is logic zero. The output of A7D is then always high because it is inhibited by the logic zero (ORRM) at pin 13. This prevents erroneous application of a cable-to-radio fault indication to NOR gate A8A when in radio repeater mode. When Radio Set AN/GRC-144 is being used in the cable terminal mode, signal ORRM is logic one. NAND gate A7D then has logic one at pin 13 and it acts as an inverter for the signal at pin 12. When a functional failure occurs, NOR gate A7C has high inputs from A7B and A6A and it applies a logic zero (low) to A7D. The low is inverted to high by A7D and applied to NOR gate A8A. This is the summary alarm output signal for cable-to-radio circuits (para 26h).

(c) The output of A6A is high, lamp driver Q10 is turned on and output signal 1CTFL is logic zero. The high from A6A is inverted to low by A6B, lamp driver Q11 is turned off and output signal OCTFL is logic one. The traffic in indicator is lighted green.

(6) *Cable Traffic Normal Functional Failure.* When cable traffic is normal and there is a functional failure, the conditions of (1) and (4) above exist and operation is as follows:

(a) The inputs to A7B, from both A8B and A6A, are high and the output is low. Lamp driver Q9 is turned off and output signal 1CFFL is logic one. The output of A7B, inverted to high by A6D, turns on lamp driver Q8 and output signal OCFFL is logic

zero. The CABLE TO RADIO MODEM indicator is lighted red.

(b) NOR gate A7C receives a low from A7B and its output is high (see (5)(b) above). The high from A7C is inverted to low by A7D and applied to A8A (para 2-6h).

(c) The output of A6A is still high and Q10, Q11, 1CTFL and OCTFL are as explained in (5)(c) above. The traffic in indicator is still lighted green.

(7) *Cable Traffic Failure.* When a cable traffic failure occurs (loss of the XCPCM signal), all functional failure signals are also affected and change to logic one (high). The conditions of (2) and (4) above then exist and operation is as follows:

(a) The inputs to A7B are high from A8B and low from A6A. The output of A7B is high and operation is as explained in (5)(a) above.

(b) NOR gate A7C receives a low from A6A and its output is high. The high output from A7C is inverted to low by A7D and applied to A8A (para 2-6h).

(c) The output of A6A is low, lamp driver Q10 is turned off and output signal 1CTFL is logic one. The low from A6A is inverted to high by A6B; lamp driver Q11 is turned on and output signal OCTFL is logic zero. The traffic indicator is lighted red.

### 2-5.1 Digital Data Combiner 1A12 Cable-To-Radio Circuits Functional Block Diagram Description

The functional relationships between cable-to-radio plug-in components and chassis circuits of digital data combiner 1A12 are shown in figure 5-8.2. Each plug-in component is functionalized and the main signal paths (heavy lines) are shown in figure 5-8.2, as well as control and alarm functions.

a. Digital Orderwire Multiplexer 1A12A1 (fig. 5-8.2 and 5-38.3). Digital orderwire multiplexer 1A12A1 is used only when operating in digital orderwire mode. A control signal from OW SEL switch 1A12S1 enables it for digital orderwire and inhibits it for analog orderwire. Input signals to module A1 are digital orderwire signals from the OCU: 1) 16 KB/s DVOW with 16 KHz timing signal DVCLK; and 2) 2KB/s DOW signal. These are all balanced signals. Output signals are the CVDOW signal to module A4 and a status signal to module A2.

(1) The balanced DVOW signal at P1-R, -L and -N is converted to TTL level in one section of U10B. Resistors R1 and R2 provide an impedance matching termination for the input line. Bias voltages for U10B are provided through resistors R7 and R8. The DVCLK signal at P1-M, -K and -S, and the DOW signal at P1-D, -F and -E are similarly processed by line receivers U10A and U4A, providing TTL level outputs at U10A-4 and U4A-4. The TTL level OVOW signal is applied to the second section of U10B. If the OW SEL switch is in the ANLG position, the AVOW/DVOW signal (P1-5) is high (AVOW active) and  $V_{cc}$  through R13 applies a high at pin 9 of inverter U7D. The AVOW/DVOW (U7D-8) signal is then low (AVOW active) and operation of module A1 is inhibited. The signal from U7D-8 is applied to U10B, U10A, U15A, U13C, and U13B. When the OW SEL switch is in the DGTL position, the AVOW/DVOW (U7D-8) signal is high and module A1 becomes operational. This is the condition considered in discussions of module A1 below.

(2) The DVOW and DVOW CLK are applied to an automatic phasing network. One-shot U1A pin 2 is triggered by DVOW and samples the DVOW clock after a delay of 12  $\mu$ sec. The sampling is done by U14A. The output of U1A triggers U1B pin 10. The output of U1B pin 12 samples DVOW clock after 8  $\mu$ sec. The sampling is done by U148. J-K flip-flop U16A then decides which phase of the DVOW clock the DVOW signal should be retimed with. If U14A-5 and U14B-9 are both high, the J input of U16A pin 3 is high and the flip-flop sets on the next falling edge of DVOW clk. If U14A-6 and U16B8 are both high, the K input of U16A pin 2 is high and the flip-flop resets. Any other combination of inputs causes no change to the output of U16A. U16A pin 5 controls whether DVOW clk is inverter or not by U11D. U11D pin 11, 16kHz, is the clock that is used by U15A to retime the DVOW signal which then appears at U15A pin 5.

(3) The 2 kb/s DOW signal (fig. 2-2.2, waveform M) U4A-4 is retimed in U15 and applied to U11B-5. The 8 kHz signal is applied to U11B-4. The retimed DOW signal (waveform N) at a rate of 2 kb/s provides a logic 1 or a logic 0 at U11B-5 for four cycles of the 8 kHz (waveform L) clock. When DOW is logic 0, the 8 kHz signal is passed through Exclusive OR gate U11B unchanged. When DOW is logic 1, the 8 kHz signal appears at U11C-8 inverted. The output at U11C-8 is designated CONDITIONED DOW (waveform P). In converting the DOW signal into the CONDITIONED DOW signal, each bit in the DOW signal is converted to four cycles of the 8 kHz signal. In the CONDITIONED DOW signal, logic 0's and logic 1's of the DOW signal are distinguishable; the 8 kHz signal is inverted for logic 1 but not for logic 0.

#### NOTE

The **CONDITIONED DOW** signal can be viewed as a 16 kb/s signal consisting of alternating logic 1's and logic 0's. In this case, logic 0 in DOW is represented in **CONDITIONED DOW** as 01010101 and logic 1 as 10101010 (fig. 2-2.2, waveforms N and P). **CONDITIONED DOW** is thus viewed as consisting of alternating I's and O's, except DOW transitions. For a DOW logic 0 to logic 1 transition, there are two consecutive logic 1's in the **CONDITIONED DOW** signal, and for a logic 1 to logic 0 transition, there are two consecutive logic 0's (waveform P). This is the way the **CVDOW** signal (multiplexed DVOW and **CONDITIONED DOW**) is analyzed for purpose of demultiplexing the **CVDOW** signal (para 2-6.1).

(4) The 8 kHz clock required for the DOW conditioning is generated by dividing the 16 kHz clock by 2 using

flip-flop U16B. This flip-flop is synchronized to the transitions of the DOW signal by detecting transitions with exclusive OR U11A. The sync signal, U11A-3 is applied to U16B pin 11 as a synchronizing input.

(5) Counter U2 divides the 16 kHz clock by 8 to obtain 2kHz DOW CLK. This clock is applied to line driver U17A pin 1. U17A converts the signal from TTL logic levels to a MIL-188 balanced signal. This signal exits the board at pins P1-A and P1-B.

(6) The DVOW signal from U15A-5 is passed through Exclusive OR gate U3A and applied to UEB-4. The effect of the signal at U3A-2 is explained in (9) below. Gates U6C, U6B and U6D are the multiplexer that combined the DVOW and DOW (in the form CONDITIONED DOW (8 kHz) from U1B-6) into the CVDOW signal (U13C-8). The 16 kHz signal (fig. 2-2.2 waveform K) at U6C-9 and the 16 kHz at U6B-5 alternately gate the DVOW signal (waveform R) through U6B and the CONDITIONED DOW (8 kHz) (waveform P) J through U6C and they are combined in OR gate U6D. Since bits of the two signals are passed through U68 and U6C by alternate halves of the 16 kHz clocks, the multiplexed signal (waveform S) has a bit rate of 32 kB/s (waveform J). The output of U6D-11 is retimed in U9A and gated through U13C as the CVDOW signal (waveform S). The CVDOW signal is routed through P1-4 to module A4.

(7) The 32 kHz clock is generated using a frequency doubling circuit consisting of U5A, U5B and U11C. The 16 kHz clock is applied to U11C-10 and is Exclusive OR'ed with a delayed version of the 16 kHz clock at U11C-9. The delay is provided by U5A, U5B, R27 and C22.

(8) The DVOW signal from U10B-9 is routed from P1-1 to P1-V and applied to U12A-2 and

U7E-11. The CVDOW signal is routed through P1-4 and P1-14 and applied to U8A-2. The DVCLK signal is applied to U12B-10. The 8 kb/s DOW signal from U13D-11 is routed through P1-U and P1-6 and applied to U88-10. Activity detectors U12A and B and U8A and B and associated circuits provide the status monitoring function for module A1. The four activity detectors are retriggerable and are in the set state (Q output at Logic 1) as long as the signal they monitor is active. As long as they receive an input pulse at least once every 150 ms, they remain set (normal condition). U12B-11, U8A-3 and U8B-11 are reset inputs. When any of these three activity detectors has a logic 0 (low) at the reset input, it is put in the reset state as long as the reset signal is low. As long as the monitored signals are active, all activity detectors remain set. The signal at U7C-6 is then logic 1 and the traffic fault indicator (CXR1) is off. The signal at U7B-4 (CDOW FAIL) is low and U7A-2 is high, so the functional fault indicator (CR2) is off. The CDOW FAIL signal is routed through P1-17 to module A2.

(9) If the DVOW signal fails, U12A-4 goes to logic 1 and U13A-3 goes to logic 0. The logic 0 from U13A-3 at U12B-11 resets U12B. Logic 1 at U12B-12, inverted to logic 0 in U7C causes traffic fault indicator CR1 to light. Logic 0 from U12B-5 then resets UA8 which resets U88 with logic 0 at pin 11. The resulting logic 1 from U8B-12, through U12B and U7B, changes the CDOW FAIL signal to logic 1 (fault). This signal, inverted in U74, lights functional fault indicator CR2. If a known failure of DVOW signal at the OCU exists, the signal sent on the DVOW line is a constant logic 1. This logic 1, inverted in U7E, inhibits U12A and the chain of actions described above does not take place; no fault indications occur. Thus, the signal at U12B-12 remains low (normal). This signal is also applied at U116-5. However, now U11B-4 is receiving a low from U10B-9, so U10B-6 is held at a constant high.

This enables U6C to pass the 16 kHz signal which is then multiplexed with the CONDITIONED DOW signal.

(10) Action of the other activity detectors is similar to that described in (9) above for DVOW and U12A. In summary, the monitor circuits produce the following actions.

(a) If DVOW fails both indicators CR1 and CR2 light.

(b) If a known DVOW failure exists at the OCU, a logic 1 is sent on the DVOW line and no fault indications occur.

(c) If a CVDOW, DVCLK or 8 KBPS DOW failure occurs, the corresponding activity detector causes the functional fault (CR2) indicator to light.

(d) Whenever CR2 lights, CDOW FAIL is logic 1.

b. Combiner, Alarm-Status 1A12A2 (fig. 5-8.2 and 5-38.4). Cable-to-radio input signals to combiner, alarm-status 1A12A2 are: EQPT FAULT (P1-M, from module A4); )GMDEF (P1-U, from module A4); TR FAIL (P1-E, from module A4); CDOW FAIL (P1-A, from module AI); and XMT PLL LOCK (P1-B, from module A3). These signals are logic 0 (normal) or logic 1 (fault). A control signal (BBLB, P1-1) from LOOP TEST switch 1A12S3 is logic 1 (normal) when 1A12S3 is not in RADIO position and logic 0 when 1A1253 is in RADIO position. Module A2 monitors these cable-to-radio signals and generates output status signals that are routed to meter panel 1A15A8, to orderwire assembly 1A13, and to external monitoring locations.

(1) The EQPT FAULT signal is applied to U11B-3, U10B-5 and U5A-1. Inverter U11B applies logic 1 (normal) or logic 0 (fault) at U8A-2 ((4), below). When signal DGMDEF is logic 0 (normal), logic 1 at U10B-4 enables U10B. When signal DQMDEF is logic 1 (fault), logic 0 at U10B-4 inhibits U10B. Thus the

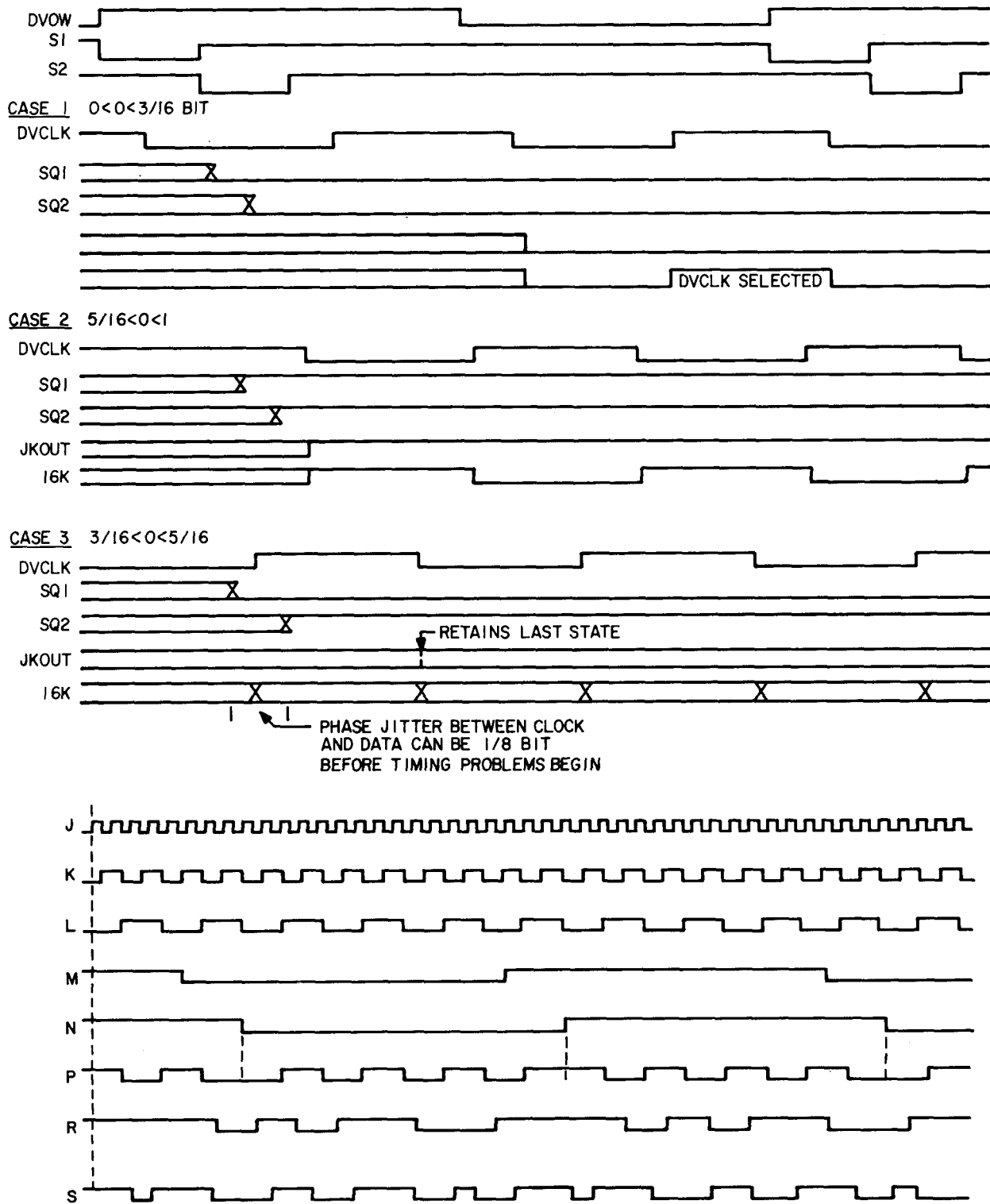
signal at U10B-6 is in fault status (logic 0) only when EPT FAULT is logic 1 (fault) and signal DGMDEF is logic 0 (normal).

(2) Signals TR FAIL, CDOW FAIL, and XMT PLL LOCK are monitored by the IC's shown in the chart below. The status of these signals is summed at U2B-6. The chart shows the logic states of indicated IC's for three conditions of the monitored signals and for both positions of LOOP TEST switch 1A12S3. As the chart indicates, when the LOOP TEST switch is not in RADIO position, U5C is inhibited and U5A is enabled. Then U5A-12 indicates a fault (logic 0) only when EPT FAULT signal at U5A-1 is logic 1 (normal). When LOOP TEST is in RADIO position, U5A is inhibited and U5C is enabled. Then U5C-8 indicates a fault (logic 0) only when the FR FAIL signal applies logic 1 (normal) at U5C-10. Thus the summary signal at U2B-6 is normally logic 0. When one of the monitored signals at P1-A, -3 or -E fails (logic 1): 1. Logic 0 at USA-12 switches U2B-6 to logic 1 (fault) if LOOP TEST switch is not in RADIO position and EQPT FAULT signal is normal; or 2. logic 0 at U5C-8 switches U2B-6 to logic 1 (fault) if LOOP TEST switch is in RADIO position and FR FAIL signal is normal. FR FAIL is a radio-to-cable monitor signal and it is discussed in paragraph 2-61a.

(3) The signal from U2B-6 is inverted in U7B and routed to meter panel 1A15A8 through P1-J. The signal is also inverted in U6E and applied to U8A-13, U8C-11 and U7A-1. The signal at U7A-16 is routed to 1A15A8 through P1-K. Thus signal OCFFL is logic 0 for normal status and logic 1 (open circuit) for fault

LOOP TEST Switch	Monitored Signal Status	U4D-13 or U4C-10		U5A				U5C			
		1	2	13	12	9	10	11	8		
Not in RADIO Position	Normal	1	1	1	0	1	Inhibited by logic 0 at pin 9. U5C-8 is logic 1.				
	Fault	0	1	1	1	0					
	Fault	0	0	1	1	1					
IN RADIO Position	Normal	1	Inhibited by logic 0 at pin 2. U5A-12 is logic 1.				1	1	0	1	
	Fault	0					1	1	1	0	
	Fault	0					1	0	1	1	

AUTO-PHASE CIRCUIT TIMING DIAGRAM



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Figure 2-2.2. Digital data combiner 1A12, waveforms.

status and signal 1CFFL is the reverse. For the normal status, these signals cause CABLE to RADIO MODEM Indicator 1A15A8DSI (green) to light and 1A15A8DS3 (red) to be off. For the fault status, the indicator conditions are reversed. The input signals at U8C are all normally logic 1 as discussed above (U6E at U8C-11), in (1) above (U8C-10) and in paragraph 2-6.1a (U8C-9). Thus, normally U8C-8 is logic 0 and U10A-3 is logic 1. The signal at U10A-1 is normally logic 1 ((2), above). When U10A-3 is logic 1, the +5 VDC supply charges capacitor C6 through R1 and R2 and applies logic 1 at U12F-6. Logic 0 at U12F-11 provides a ground from the coil of relay K2 and K2 is energized (normal). Contacts 1 and 3 of K2 are then open and a logic 1 (open circuit) signal is routed through P1-R and -S to the OCU. When the FR FAIL signal at U10A-1 is normal (logic 1), if any input signal at U8C switches to fault status (logic 0), U10A-3 switches to logic 0. Capacitor C6 then discharges through R2, and after a slight delay, the signal at U12F-6 is logic 0 and at U12F-11 is logic 1. Relay K2 is deenergized and the logic 0 (closed circuit) at P1-R and -S indicates fault status.

(4) The signal (TFC IN) from U11B-4 ((1) above) is inverted in U12C so signal 1CTFL is normally logic 0. TFC-IN is twice inverted in U11A and U12D so OCTFL is normally logic 1. These signals are routed through P1-15 and -16 to external monitoring locations. The signals at U8A-2 and -13 (paragraphs (1) and (3) above) are normally logic 1. The signal at U8A-1 is a radio-to-cable signal (para 2-6.1a) and is normally logic 1. Operation of +5 VDC through R3, R4 and C7 with logic states at U8A-12 is similar to that described for U10A in (3) above. For normal status U8A-12 is logic 0, U12E-12 and signal OMARY are logic 1 and indicator CR2 is off. If any input at U8A changes to fault (logic 0)

status, these conditions reverse and CR2 turns on. Signal OMARY is routed through P1-14 to ,orderwire assembly A13 and applied to module A13A2 (para 2-8). Signal DOM (P1-T) is an input signal from LOOP TEST switch 1A12S3 and from AVOW switch 1A1252. When S3 is in OFF position and S2 is in NORMAL position, signal DOM is logic 1 and has no effect. If S3 is placed in either DGM or RADIO position or if S2 is placed in BYPASS position, signal DOM is logic 0. Signal OMARY is then clamped to ground (logic 0) and indicator CR2 turns on. Signal OMARY is also clamped to ground if signal FR FAIL is in fault status. Relay K1 is then energized (para 2-5.2b below), and ground is applied to U12E-12/P1-14 from K1-6 and 7.

c. Digital Randomizer 1A12A3 (fig. 5-8.2 and 5-38.5). Digital randomizer 1A12A3 is comprised of a scrambler circuit that operates on the data signal in the transmit direction, a descrambler circuit that operates on the data signal in the receive direction, and monitor circuits. An INHB/OPR Jumper plug P2 on the digital randomizer inhibits scrambler and descrambler circuits when the AN/GRC-144(V)3 or (V)4 operate with radio sets without randomizer circuits. The purpose of the scrambler is to change the characteristics of the transmit data stream so that the probabilities that any bit will be a logic 1 or logic 0 are approximately even (50%). Since the transmit data signal is ac coupled to the radio modulator, if a long string of 1's or 0's occurs, the average level of the signal varies substantially and causes the modulator to drift. Also, in the receive direction, recovery of the clock signal depends on detection of data signal transitions; scarcity of transitions makes the recovered clock signal less dependable. So the scrambled transmit data signal, with logic 1 and logic 0 distribution approximating

.50 percent, minimizes the effect on the modulator and improves recovered clock reliability. The descrambler circuit, J similar in operation to the scrambler circuit, operates on the receive signal that was scrambled at the remote end of TMG, P1-U) is applied to the shift register

through U11B. The data signal is clocked through the shift register and the output at U4B-9 is passed through buffer/driver U12A to P1-S. In the "shift register, U8A, U8B and U4B are

EXCLUSIVE OR GATE U11D						
INPUT			OUTPUT			
U8B-9 (B <sub>7</sub> )	U11D-12 (B <sub>15</sub> )	U11D-13 ( $\overline{B_7}$ )	U11D-11	$\overline{\text{BFRD DATA}}$	SHIFT REGISTER INPUT	ACTION ON $\overline{\text{BFRD DATA}}$ INPUT
1	0	0	0	0	0	No change when B <sub>7</sub> and B <sub>15</sub> are logical opposites
0	1	1	0	1	1	
0	0	1	1	0	1	$\overline{\text{BFRD DATA}}$ signal inverted when B <sub>7</sub> and B <sub>15</sub> are logical equals
1	1	0	1	1	0	
			U11A-1	U11A-2	U11A-3	
			INPUT		OUTPUT	
EXCLUSIVE OR GATE U11A						

the transmission link. It performs a functionally reverse operation and outputs the original signal unscrambled. Failure monitors track activity of the transmit and receive data streams and provide alarm signals when a failure occurs. In addition, when the randomizer is inhibited a monitor circuit is activated causing CR2, a yellow digital randomizer LED, to illuminate.

(1) The scrambler circuits consists of a 15-stage shift register (U8A, U3, U8B and U4B) with feedback from U4B-9 and U8B-8 through exclusive OR gates U11D and U11A. The BFRD DATA input signal (P1-T) is applied through U11A to the first stage (U8A) of the shift register. The clock signal (BFRD

D-type flip-flops and U3 and U1 are 8-stage shift registers. Only the first five stages of U3 are used and only the first seven stages of U1. The shift register always contains 15 bits, B1 is the output at U8A-5; B6 is at U3-10; B7 is at U8B-9 and B15 at U4B-9. Bits B7 (U8B-8) and B15 (44B-9) are fed back through exclusive OR gates U11D and U11A to control the data input at U8A-2. For every clock cycle, each data bit is shifted forward one stage (B1 becomes B2, etc); B14 becomes B15, the new output bit. At the same time a new B1 is shifted in a U8A-2; it is the next BFRD DATA bit fed through U11A. The action of U11A on the BFRD DATA bit at U11A-2 is determined by the logic state of signals

B7 and B15. If B7 and B15 are logical opposites (0, 1 or 1,0), the data bit at U11A-2 appears at U11A-3 unchanged and is clocked into U8A-2. If B7 and B15 are logical equals (0,0 or 1,1, the data bit U11A-2 is inverted and then clocked into U8A-2. The logic action is explained in the truth tables above for exclusive OR gates U11D and U11A. Columns 1 and 2 show the possible logic states for B7 and B15. Columns 2 and 3 show the inputs to U11D and column 4 shows the corresponding output at U11D-11. The input signal at U11D-13 is B7 instead of B15. The output at U11D-11 is the input at U11A-1. Column 5 shows the BFRD DATA input and column 6 shows the resulting output at U11A-3 which is the input to the 15-stage shift register. When the randomizer is inhibited, the scrambler feedback at U11A-1 is not effective (open) and U11A-1 is grounded causing the BFRD DATA to remain unchanged at U11A-2 and U11A-3 when clocked into U8A-2.

(2) The descrambler circuit is similar to the scrambler circuit. The RCOVD DATA (P1-1) and RCOVD TMG (P1-2) signals are applied to a 15-stage shift register (U10, 6 stages; U2A, 1 stage; U7, 7 stages; and U2B, 1 stage) through buffers U15A and U15B. The data input signal at U10-1 is clocked through the shift register. Bit B15 (U28-8) and B7 (U2A-5) through exclusive OR gate U15C control the logic action at exclusive OR gate U15D. The input data signal (U15A-3) is also applied to U15D and it is inverted or not by U15D depending on the logic state of the signal at U15C-6. The truth table for the logic action that occurs is the same as that given above for the scrambler, substituting U15C for U11D and U15D for U11A. The descrambled output signal at U15C-8 is then shifted through flip-flop U6A and buffer U13A to P1-M. When the randomizer is inhibited the feed forward bits at U15D-9 are not effective and U15D-9 is grounded

causing the RCOVD DATA to remain unchanged when clocked into U6A-2.

(3) An individual flip-flop may be set or reset when power is first turned on; the initial state is random unless means are provided to predetermine it. Thus for the flip-flop of the 15-stage shift register, any distribution of 1's or 0's could result at power turn-on, including a state of all 1's or all 0's. A state of all 1's or all 0's is called a lockup state because if it occurred, and the data input signal was also all 1's or all 0's, the data randomizing function would not take place. The SETUP signal is used to avoid the possibility. At power turn-on, the input at P1-13 supplies the +5 vdc Vcc operating voltage. This voltage is also applied through R12 to U8A-4, the PRE-SET input. Logic 0 is the active input signal level. The circuit wiring has capacitance to ground and this capacitance must charge to the logic 1 level before a logic 1 is applied at U8A-4. During the resultant delay time, U8A-4 has in effect a logic 0 input and since it has operating Vcc applied, it is set, with logic 1 at U8A-5. After the initial delay time, U8A-4 is logic 1 and the PRESET input is inactive. In a similar manner, the SETUP signal applies logic 0 at the CLE input U1-9 during the delay time and the flip-flop in U1 are reset. Thus the SETUP signal prevents an initial state of all 1's or 0's in the shift register.

(4) Monostable retriggerable multi-vibrators (failure monitors) U9A, U9B and U5A are set at power-up by pullup resistors R20 and R14. The failure monitors have a timed output of 150 msec provided by external RC networks consisting of capacitors C4, C5 and C6 and resistors R15, R16 and R17. When the monitored input signal at U9A, U9B or U5A pins 1 or 9 is active and



Randomizer Section	Status	1A12A3 Connector		U11C-8
		5	6	
Scrambler	Normal	0	1	1
	Fault	1	1	0
Descrambler	Normal	0	1	1
	Fault	0	0	0

provides a logic 1 input at least once every 150 msec, the monostable is maintained in the set state (Q at logic 1, Q at logic 0). If the monitored signal fails, the monostable times out after 150 msec and is reset. When all randomizer circuits are operating normally the levels at U14C-9 and U14C-10 are a logic 1 and the SCRM FAIL (pin 5) and the DSCRM FAIL (pin 6) levels are as give below. The output signal at U14C-8 is a logic 0 when randomizer circuits are operating normally. Pullup resistor R14 provides a logic 1 at U11C-10. With a logic 1 and logic 0 at U11C-9 and U11C-10 respectively, the signal at U11C-8 is a logic 1 and the status indicator CR1 is off (normal). With a SCRAM DATA or DSCRM DATA failure the logic inputs to U14C change. The logic level at U14C-8 is changed to a logic 1 and U11C-8 is changed to a logic 0; these conditions turn on CR1 (fault). If the SCRM DATA signal (from U4B through U12A) is active, U9A is held in the set state and the signal at U14C-9 is logic 1. If the SCRM DATA fails, U9A times out and resets (Q at logic 0, Q at logic 1) and applies a logic 0 at U14C-9 and logic 1 at U9A-4. The logic 1 at U9A-4 is the SCRM FAIL signal

to alarm-status combiner 1A12A2 module. The outputs of failure monitors U9B and U5A are applied at U14D pins 12 and 13 so that a RCVOD DATA or DSCRM DATA failure will time out U5A or U9B respectively and change the logic condition at the input to U14C, turning on CR1 (fault) as described above. The logic 0 at U14D-11 is the DSCRM FAIL signal to alarm status combiner 1A12A2 module. Failure monitor U5B is used to monitor the INHB/OPR jumper P2 positions. When jumper P2 is in the OPR position, operation of U5B is identical to that of U5A, except that the output at U5B-5 is a logic 1 and the status indicator CR2 is off. When jumper P2 is in the INHB position a ground is applied to U5B-9 and the failure monitor times out (Q goes to a logic 0) turning on status indicator CR2, indicating that randomizer operation is inhibited.

d. Digital Interface Buffer 1A12A4 (fig. 5-8.2 and 5-38.6). Digital interface buffer 1A12A4 is the interface for data signals to and from the DGM and it combines the CVDOW signal from module A1

with the retimed data signal. Input signals are: 1) data and timing signals from the DGM; 2) radio recovered and descrambled data and timing signals from module A3; CLB and BLB signals from LOOP TEST switch 1A12S3; 4) 1HIBTR signal from AVOW switch 1A12S2; and 5) signals from DATA RATE SEL (MB) switch 1A12S4.

(1) Signals DATA and TMG from the DGM are applied to level converter U4. Resistors R3, R4, R10 and R11 are impedance matching line terminations. Bias voltages for U4 are applied through resistors R2, R6, R8 and R13. Capacitors C1 and C2 are for supply voltage bypass. The TTL level BFRD DATA AND BFRD TMG signal outputs of U4 are applied through inverter line buffers (U6E, U6D) to digital randomizer module 1A12A3. Voltage levels for the logic 1 state are applied through resistors R5 and R9. The outputs at U4-4 and -9 are also applied to multiplexer U7.

(2) Multiplexer U7 is a quadruple 2-pole electronic switch; switching operation is controlled by the B/A input at pin 1. Logic 1 levels for the signal inputs to U7 (and U12) at pins 2, 3, 5 and 6 are provided through pull-up resistors R14, R15, R20 and R23. Resistors R24 through R27 perform a similar function for U12. Only two of the four switches in U7 are used. When LOOP TEST switch (S3) is in either the OFF (NORMAL) or RADIO position, the input at P1-J and at U7-1 is logic 1 (via pull-up resistor R12). The DSCRM DATA signal (from module A5) at U7-3 is then connected to output 1Y (pin 4), and the DSCRM TIMING signal at U7-6 is connected to output 2Y (pin 7). When LOOP TEST switch is in DGM position, the signal at U7-1 is logic 0 and the signals at U7-2 (BFRD DATA) and U7-5 (BFRD TMG) are connected to the outputs at U7-4 and U7-7, respectively. The selected outputs at U7-4 and U7-7 are routed to the DGM

(3) below). Thus multiplexer U7 acts as the cable loopback switch. In normal operation, the DSCRM DATA and TIMING signals from the remote site are passed by U7 and routed to the DGM (fig. 5-8.2, solid lines in U7). In cable loopback mode, the DATA IN and TMG IN signals from the DGM are passed by U7 and returned to the DGM (fig. 5-8.2, dashed lines in U7).

(3) The DATA output at U7-4 is retimed in U11 and converted to a balanced signal in line driver U10. The timing signal from U7-7, twice inverted in U6B and U6A, is similarly converted in U10. U6A and U6B are used to provide a time delay to compensate for the delay the data signal encounters in passing through U11B. Resistors R17, R18, R19, R21, R22 with C4 and CR1 comprise a balancing and impedance matching network.

(4) Three pairs of input signals are applied to multiplexer U12: 1) RCOVD DATA at pins 5 and 6 from module A5 and TIMING at pins 10 and 11 from DSCRM or BFRD TMG; 2) BFRD DATA and TIMING at pins 4 and 12, from U4; 3) SCRM DATA and TMG at pins 3 and 13 from module A3. Multiplexer U12 is a dual 4-pole electronic switch; switching operation is controlled by signals at pins 14 (A) and 2 (B). The A (pin 14) logic 1 level signal is supplied by pull-up resistor R56. The B (pin 2) signal is supplied by LOOP TEST

switch (53). Multiplexer U12 connects one of the three pairs of input signals to outputs 1Y (pin 7) and 2Y (pin 9) according to the logic states of signals A and B. The three possible combinations of logic states for signals B/A (U7), A and B are listed in the chart below along with the corresponding positions of the LOOP TEST switch in column 1. Columns 4, 5 and 6 indicate which input pins are connected to output pins 7 and 9 and the signals passed by U12 for each logic state of signals A and B. Thus U12 functions as the radio loopback switch: it selects the signal to be sent to the radio transmitter ((5) below) under control of the LOOP TEST switch.

(5) The data output signal at U12-7 is applied to U11A-2. U11A is operational as long as the signal at reset input pin 4 is logic 1. When this signal is logic 0, U11A is locked in reset and the data signal from U12 is blocked. Signal 1HIBTR (P1-A) is controlled by OW SEL switch S1 and AVOW switch S2. Signal 1HIBTR is inverted in U6F and applied at U11A-4 as signal 0HIBTR. The switch positions and the corresponding logic state of the signal at U11A-4 are given in the chart on the following page. As indicated in the chart, the signal at U11-4 is logic 0 only when the switches select the analog orderwire bypass mode. For other switch positions U11A is operational. The data signal from U12 is retimed in U11A. The output

LOOP TEST SWITCH	INPUTS					OUTPUTS	
	U7 B/ $\bar{A}$	U 12				DATA (Pin 7)	TIMING (Pin 9)
		A	B	DATA PIN	TMG PIN		
DGM	0	1	1	6,5	10,11	FROM RADIO (RCOVD)	
OFF	1	1	1	3	13	SCRM	
RADIO	1	1	0	4	12	BFRD	

signal at U11A-5 is inverted in U3 and applied to U14.

(6) The CVDOW signal from module A3 is applied to inverters U13C and U13D. It is gain-adjusted according to the data rate in use by U13C, U13D, buffers and gain of Q1 are highest. For the

highest rate group, ground at U15E cuts R40 and R42 out of the circuit and the bias and gain of Q1 are lowest. When CVDOW is logic 0, U13D-11 and U13C-8 provide a high impedance output, isolating U13D and U13C from the bias network. The rate group

SWITCHES		SIGNALS	
OW SEL (S1)	AVOW (S2)	IHIBTR (P1-A)	OHIBTR (U11A-4)
DGTL	NORM	0	1
ANLG	NORM	0	1
DGTL	BYPASS	0	1
ANGL	BYPASS	1	0

U15 and transistor Q1, under control of signals from DATA RATE SEL (MB) switch S4, in three rate groups. The rate groups and the CVDOW signal levels are as follows:

Rate Group	Data Rate	Level
A (P1-R)	9.36 or 18.72	2.2v
B (P1-S)	2.048 to 4.9152	3.3v
C (P1-P)	1.024 to 1.536	4.4v

U13 and U15 are open collector type IC's that is, a logic 1 output is a high impedance (open circuit) instead of a logic 1 level voltage. Logic 0 is applied to the U15 buffer corresponding to the rate group in which the operating data rate falls. Logic 1 is applied through pull up resistors R37, R39 and R41. The buffer corresponding to the selected rate has logic 0 output. It grounds the junction of R38/R40 (U15E) or R40/R42 (U15D) or it grounds R42 at U15F. These resistors with CR2 and R35 determine the bias and therefore the gain of Q1 when it is turned on. For the lowest rate group (U15F), all resistors are in the bias network and bias signals (A, B, C) then determine the bias and gain of Q1

and therefore of the GACVDOW signal level at the emitter of Q1. This signal level is given in the chart above. When CVDOW is logic 1, U13D-11 and U13C-8 are logic 0, Q1 is cut off and the GACVDOW signal is logic 0. The GACVDOW signal is connected through a 3-pole Butterworth filter (R35/C5, L1, R33/C6) to the input of buffer amplifier U14. The data signal from inverter U3 ((5) above) is also applied to U14. The two signals are linearly added in R44 which is used to adjust the gain of U14 to unity. The output of U14, approximately 2 v peak-to-peak, is reduced to 1 v peak-to-peak in a T-network attenuator (R45, R46, R49) and routed to the radio (P1-18 and -V).

(7) IC's U1, U2, U5, U6, U8 and U9 comprise the status monitoring circuits. U2A and B and U9A and B are retriggerable monostables with a timed output of 150 msec. When the monitored input signal at pin 2 or pin 9 is active and provides a logic 1 input at least once every 150 msec, the monostable is maintained in the set state (Q at logic 1, Q at logic 0). If the monitored signal fails, the monostable times out after 150 msec and is reset

(8) When DATA IN and TMG IN signals (from U4) are active, U2A and U2B are held in the set state. The signal at U5B-5 is then logic 0 and U5B-6 applies logic 1 at U8C-8, so U8C-10 applies logic 0 at U8A-2. At the same time U2A-4 applies logic 0 at U8A-3. With logic 0 at both inputs, the signal at U8C-1 is logic 1 and status indicator CR4 is off (normal). The EQP FAIL signal is then logic 0 (normal) and signal DGMDEF (U8C-10) is logic 0 (normal). For this condition signal DATA IN (U2B-10) is also active (normal). If signal DATA IN fails, U2A times out and resets and U2A-4 applies logic 1 at U8A-3. Logic 0 at U8A-1 then causes status indicator CR4 to light and signal EQP FAIL changes to logic 1 (fault). If TMG IN

signal fails, U2B times out and resets and U2B-5 applies logic 0 at reset input U2A-3. U2A is then reset and held in reset as long as U2B is in reset. Logic 1 from U2A-4 then produces the same changes as described above for failure of DATA IN. If a known failure of the DATA IN signal at the DGM exists (but TMG IN signal is still active), a constant logic 1 is sent on the DATA IN line. U2A then times out and U5B has logic 1 at both inputs, so U5B-6 applies logic 0 at U8C-8. Since TMG IN is active, U2B is still applying logic 0 at U8C-9 so U8C-10 U changes to logic 1. Logic 0 at U8A-1 then turns on indicator CR4 and status signals DGMDEF and EQP FAIL are both logic (fault).

(9) Under normal operating conditions, the signals at U5D-12 and U5C-9 and -10 are logic 0, and the signal at U5D-13 is logic 1. U5D-11 and U5C-8 then apply logic 1 at U1B-4 and U1A-2, respectively. When signals DATA (TO RADIO) at U9B-10 and DATA (TO DGM) at U9A-2 are active, the signals at U9B-12 and U9A-4 are logic 0. U1C-8 then applies logic 0 at U1B-5 and U9A-4 applies logic 0 at U1A-1. U1B-6 and U1A-3 are then logic 0, signals TR FAIL and DT FAIL are logic 0 (normal), and status indicator CR3 is off. If the DATA (TO RADIO) signal fails, U9B times out and resets, and U9B-12 applies logic 1 at U1C-9. The 0HIBTR signal at U11C-10 is normally logic 1 (see chart in para (5) above) so U1C-8 applies, logic 1 at U1B-5. Since the signal at U1B-4 is normally logic 1, the signal at U1B-6 changes to logic 1 and signal TR FAIL is in the fault state. The logic 1 from U1B-6 changes the signal at U8B-4 to logic 0 and indicator CR3 turns on. In a similar manner, failure of the DATA (TO DGM) signal changes the DT FAIL signal to logic 1 (fault) and lights indicator CR3. U50 has two logic 1 inputs and logic 0 output (U5D-11) only when signal DGMDEF is logic 1 (fault) and LOOP TEST switch is not in RADIO position. For this condition, U1B is inhibited and a TR FAIL fault indication cannot occur. U5C has two logic 1 inputs only when signal DGMDEF is logic 1 (fault) and LOOP TEST switch is in DGM position. For this condition, U1A inhibits a DT FAIL fault indication.

## 2-6. Digital Data Modem 1A12 Radio-to-Cable Circuits Functional Block (fig. 5-8 and 5-8.1)

The functional relationships between the radio-to-cable plug-in components and chassis circuits in digital data modem 1A12 are shown in figure 5-8 for the synchronous mode and in figure 5-8.1 for the asynchronous mode. Each plug-in component is functionalized and the main signal paths (heavy lines through each plug-in component and between plug-in components) are shown. In addition, the control and alarm functions are shown. The operation of the synchronous mode plug-in components is described in a through h and the operation of the asynchronous plug-in components is described in *b.1*, *c.1*, and *i*.

*a. Radio Digital Regenerator 1A12A8* (fig. 5-8 and 5-36). Radio digital regenerator 1A12A8 receives the pcm plus orderwire signal (FRPCM) from Receiver,

Radio R-1467/C-144; separates the pcm signal from the orderwire signal; reshapes and amplifies this signal and applies output signals to 1A12A7 and 1A12A9 (1RSPCM-1 and 1RSPCM-2).

### (1) *Pcm recovery circuits.*

(a) Signal FRPCM is applied to differential amplifier Q1A, B which generates a signal proportional to the difference between the input signal and a fixed reference. Linear buffer 1 (Q2, Q3) provides a signal with a low impedance source to drive the following peak detectors. The peak detectors consist of two half-wave diode rectifiers and filter circuits. The time constants of the filter circuits allow the capacitors to charge to the positive and negative peak excursions of the input signal.

(b) The detected signals are applied to a voltage divider which derives the algebraic average of the peak-detected voltages. Linear buffers 2 and 3 (Q4 and Q5) provide a high impedance buffer between the peak detector circuits and the input of voltage comparator A4. Voltage comparator A4 compares the inputs from linear buffers 2 and 3. The output of linear buffer 3 (Q4B, Q5B) is the reference signal for the voltage comparator. When the amplified FRPCM output of linear buffer 2 (Q4A, Q5A) is more positive than the reference, the voltage comparator output is high; when the amplified FRPCM signal is more negative than the reference, the voltage comparator output is low. The output signal from the voltage comparator is the reshaped pcm signal.

(c) Digital buffer A3A inverts the output (pcm signal) of the voltage comparator for application to digital buffers A3B and A3C. These reinvert the signal and provide parallel outputs (1RSPCM-1) and (1RSPCM-2).

(d) The output signal of digital buffer A3C (1RSPCM-2) is also connected to transition detector 1 (A9) which is a monostable multivibrator. Each time monostable multivibrator A9 is triggered by the negative-going transition of a logic one and holds for 350 microseconds (approximately). If A9 receives another trigger

pulse before it times out (350 microseconds), the timing cycle starts over again. Thus, as long as pcm trigger pulses occur at least once every 960 microseconds, the output of A6 is held at logic one (pin 8). The logic one output at pin 8 is inverted by lamp driver A1 and provides a logic zero (low) at lamp DS1. Lamp DS1 is then lighted. Pin 6 of A9 of this time has logic zero output. This signal (1RRFAIL) is sent to alarm-monitor 1A12A5. If A9 times out, the outputs become logic zero (pin 8) and logic one (pin 6). Lamp DS1 goes out and 1RRFAIL indicates failure (logic one).

(2) *Traffic alarm circuits.*

(a) The FRPCM signal is applied to slicer 1 (A7) which has a fixed reference voltage at the other input. A7 is a high speed differential comparator and it compares the signal (FRPCM) with the reference voltage. It produces a pulse output with a steep vertical rise for negative going voltage transitions at the input and a sharp vertical drop for positive-going transitions. Thus, the input signal is sliced into separate voltage pulses corresponding to the logic ones in the FRPCM signal.

(b) The square wave output of A7 is applied to both inputs of nand gate A4C in the leading edge pulse generator; directly to pin 9 and through delay inverters A5A, A5B and A5C so pin 8. Because of the propagation delay through the three inverters, the input signals to A4C are logic one simultaneously only for a short time immediately following a positive going transition at the output of A7. The output signal of A4C is a series of short duration pulses (logic one) that correspond in frequency with transitions of the input signal (FRPCM).

(c) The output pulses from A4C are applied, through inverters A4D and A1, to a tuned circuit with a crystal filter. The resonant frequency of the tuned circuit and crystal is the pcm signal frequency, 2304 kHz. The applied pulses cause the tuned circuit to ring or oscillate, but only at its own frequency, and if the frequency of the pulses differs too much from the tuned circuit frequency, oscillation is not sustained. Thus, the tuned circuit rejects small timing errors caused by noise pulses and distinguishes between the normal pcm signal and a random noise-pulse-only condition that exists when the pcm signal is lost.

(d) The output signal from the tuned circuit is applied to slicer 2 (A6) which is similar to slicer 1 (A7). The square wave output of A6 is applied to transition detector 2 (A10) which has a time constant

of 420 nanoseconds and is otherwise similar to transition detector 1 (A9). A10 provides a low (logic zero) output at pin 6, as long as it receives input signals from A6. Voltage comparator A8 then provides a logic one output and this is inverted to logic zero by A3E. When the pcm signal fails, the tuned circuit no longer receives inputs with the timing required to sustain oscillation, A10 times out and the output at pin 6 goes to logic one. Output signal 1FRFAIL then becomes logic one to indicate failure of the FRPCM signal.

b. *Radio Control-Comparator 1A12A9, Synchronous Mode* (fig. 5-9 and 5-37). Radio control-comparator 1A12A9 synchronizes the frequency of the 4608 kHz radio-to-cable clock signal with the frequency of the pcm signal and it retires the pcm signal.

(1) *Synchronizing.* Radio control-comparator 1A12A9 receives the 4608 kHz radio-to-cable clock signal from 4608 kHz vco 1A12A11 and the reshaped pcm signal from radio digital regenerator 1A12A8.

(a) The 4608 kHz radio-to-cable clock signal (OR4608) is applied to the trigger input of clock counter flip-flop A9 which triggers on the positive-going transition of clock pulses (waveform A, fig. 5-37). Each time A9 is triggered, the logic one output (pin 5) takes on the logic state of the signal present at input D (pin 2) at that time. The output at pin 6 is always the complement (logical opposite) the output at pin 5. The output state of A9 is then maintained until the next trigger pulse. As a result, A9 divides the input signal by two and provides output signal 2304 kHz cable-to-radio clock (waveform B, fig. 5-37) which is sent to radio digital processor 1A12A10 and to NAND gate A5C. Gates A5C, A5D and A4C and flip-flop A9B are included for use in a future application. A9B and A5D are not used and A5C and A4C act as inverters. The 2304 kHz radio-to-cable clock signal from pin 6 of A9 is inverted by A6C, A4C and A4B and applied to the trigger input of pcm retiming flip-flop A8 and to the clock pulse generator (waveform C, fig. 5-7).

(b) Signal 1RSPCM-2 is applied directly to one input (pin 5) of NAND gate A5B in the data pulse generator and to the other input (pin 6) through delay inverters A5A, A4D and A4A. Because of the propagation delay through the three inverters, the input signals to A5B are simultaneously logic one only for a short time immediately following a positive-going transition of the pcm signal (ODP waveform, fig. 5-7). The resulting logic zero output of A5B sets

phase comparator A2B, A2C (waveform OFF, fig. 5-37). The 2304 kHz radio-to-cable clock signal is applied directly to one input (pin 1) of NAND gate A3A in the clock pulse generator and to the other input (pin 2) through inverters A3C, A3D and A3B. Because of the propagation delay through the three inverters, the input signals to A3A are simultaneously logic one only for a short time immediately following a positive-going transition at the output of A4B. The resulting logic zero output of A3A resets phase comparator A2B, A2C (waveform OFF, fig. 5-37). Thus, phase comparator A2B, A2C is set by the leading edge (positive-going transition) of data pulses and reset by the leading edge of clock pulses. The difference in time between set (ODP) and reset (OCP) pulses to the phase comparator is a measure of the phase difference between data input 1RSPCM-2 and clock input OR4608.

(c) The output (E7) of the delay circuit in the data pulse generator (6(b) above) is also connected to baud generator A6 which is a nonstable multivibrator. It generates a positive output pulse each time the input signal goes to logic zero. The duration of the positive pulse is adjusted so that the total time from the start of ODP to the end of the baud pulse is 4d4 nanoseconds. This signal is applied as one input (1BP to AND gate A7B (waveform, 1B-P fig. 5-87).

(d) The output signal of the phase comparator (OFF) (waveform, OFF fig. 5-37), which represents the phase difference between data and clock signals, is inverted by inverter A7A. The output signal of inverter A7A (waveform, 1PP fig. 5-37) causes the positive pulse generator to generate the positive pulse input to differential integrator A1. The output of the baud generator (1BP) and the output of the phase comparator (OFF) are applied to AND gate A7B. The output of AND gate A7B (waveform, ONP fig. 5-37) causes the negative pulse generator to generate the negative pulse input to differential integrator A1. Thus, at the start of each data pulse (corresponding to a logic one bit in the data signal) ODP goes negative, OFF goes negative and 1PP. This condition holds and is a positive pulse goes positive. Input to the integrator is generated until OCP goes negative. When OCP goes negative, OFF goes positive and since 1BP is positive, ONP goes negative. This condition holds and a negative pulse input to the integrator is generated until 1BP goes negative. When zero bits occur in the input signal (1RSPCM), ODP remains high and the phase comparator flip-flop is not set, so OFF remains high.

Thus, 1PP remains low and positive pulses to the integrator are not generated. Also, 1BP remains low, so ONP is high and negative pulses to the integrator are not generated.

(e) The output signal of differential integrator A1 is connected to the frequency control input of 4608 kHz vco 1A12A11. When the input to A1 is a positive pulse, the output is a negative-going change in voltage. When the input is a negative pulse, the output is a positive going change in voltage. This means that the output voltage starts to rise (or fall) at a fixed rate of change (slope). When clock and data are in synchronism, positive and negative pulse inputs to A1 are approximately equal, and the positive and negative-going changes in output voltage cancel since the slopes are equal. These low amplitude excursions of the output signal are filtered at the input of 1A12A11 and the output frequency remains constant. When the positive pulse inputs to A11 are longer than the negative pulses, the negative-going output caused by the positive pulse is not entirely canceled by the return in the zero direction caused by the following negative pulse. The net result is that the signal remains negative and will go more negative as long as this condition (longer positive pulses) holds. However, the negative output signal causes the frequency of 1A12A11 to increase, clock pulse OCP then occurs sooner and positive pulses are shortened and the length of negative pulses is increased. This action and reaction occurs until positive and negative pulses are equal. When the negative pulses are longer than positive pulses, the same kind of action in the opposite direction takes place. The output of A1 goes positive, clock frequency is decreased and clock pulse OCP is delayed. This shortens the negative pulses. The result is that the output of A1 always produces a frequency change at 1A12A11 that tends to equalize positive and negative pulses and when equality is established to maintain it. When the data signal has logic zero bits, neither positive nor negative pulses are sent to integrator A1, however, it has a long time constant which holds its output to bridge over these short intervals.

(f) The output of differential integrator A1 is also connected to positive/negative clamp detector A10. Normally, the output of differential integrator A1 is close to zero volts as it holds the clock signal in synchronism with data. The output of A10 is then low. The low output from



A10 is inverted twice by the lamp driver (inverter A2A and Q4), so signal 1RCFAIL is low (logic zero) and lamp DS1 is lighted. However, when correction is required, the output of AI can vary from +3 volts to -3 volts. Positive/negative clamp detector A10 detects output signals of AI that exceed the indicated limits. When either limit is exceeded the output of A10 goes high. This signal, inverted twice by the lamp driver, is sent to alarm monitor 1A12A5 and also turns off lamp DS1.

(2) *Retiming.* The 2304 kHz radio-to-cable clock signal (waveform C, fig. 5-37) is applied to the trigger input of pcm retiming flip-flop A8 and the 1RSPCM-2 signal (waveform D, fig.

5-37) is applied to the D input. Operation of flipflop A8 is similar to operation of A9 ((1) (a) above). Signal 1RSPCM-2 is retimed by the 2304 kHz radio-to-cable clock. The output signal (waveform E, fig. 5-37) is sent to radio digital processor 1A12A10.

b. *Radio Control-Comparator 1A12A9, Asynchronous Mode (fig. 5-8.1 and 5-37.1).* Radio control-comparator 1A12A9, synchronizes the frequency of the 9830.4 kHz radio-to-cable clock signal with the frequency of the pcm signal and it retimes the pcm signal.

(1) *Synchronizing.* Radio control comparator 1A12A9 receives the 9830.4 kHz radio-to-cable clock signal from 9830.4 kHz vco 1A12A11 and the reshaped pcm signal from radio digital regenerator 1A12A8. The 9830.4 kHz radio-to-cable clock signal (0R98304) is applied to the trigger input of clock counter flipflop A9A which triggers on the positive-going transition of clock pulses (waveform A, fig. 5-37.1). Each time A9A is triggered, the logic one output (pin 5) takes on the logic state of the signal present at input D (pin 2) at that time. The output at pin 6 is always the complement (logical opposite) the output at pin 5. The output state of A9A is then maintained until the next trigger pulse. As a result, A9A divides the input signal by two and provides output signal 4915.2 kHz cable-to-radio clock (waveform B, fig. 5-37.1) which is sent to radio digital processor 1A12A16 and to NAND gate A5C. When the ADDM TRAFFIC SELECT switch is in the 48 CHAN position, the input signal at pin 9 is logic 1 (+5v) and the signal at pin 10 is logic 0 (grd). The clock signal is divided by two again in A9B and this 2457.6 kHz signal can now pass through NAND gate A5D, which is enabled by the logic 1 at pin 13. The 4915.2 kHz signal from A9A is blocked at A5C which has logic 0 at pin 8. When the ADDM TRAFFIC SELECT switch is in the TM 11-5820-695.-35 96 CHAN position, A5D has logic 0 at pin 13, blocking the 2457.6

kHz signal. A logic 1 signal is present at pin 8 of A5C and the 4915.2 kHz signal can pass. Thus the selected clock signal is routed through A4C and A4B to the trigger input of pcm retiming flip-flop A8 and to the clock pulse generator (waveform C, fig. 5-37.1). For the remainder of the discussion of 'synchronizing, see b(l)(b) through b(l)(f) above, which apply also to operation in the asynchronous mode.

(2) *Retiming.* The 2457.6 kHz clock (48 CHAN) or the 4915.2 kHz clock (96 CHAN) whichever is selected by the ADDM TRAFFIC SELECT switch is applied to the trigger input of pcm retiming flip-flop A8 (waveform C, fig. 5-37.1). The 1RSPCM-2 signal (waveform D, fig. 5-37.1) is applied to the D input. Operation of flip-flop A8 is similar to operation of A9 ((1) above). Signal 1RSPCM-2 is retimed by the 2457.6 kHz or 4915.2 kHz clock. The output signal (waveform E, fig. 5-37.1) is sent to radio digital processor 1A12A16.

(3) *Baud Generators.* The duration of the baud pulse generated by 48-channel ddm baud generator A6 is determined by the current drive supplied by the +5vdc supply and time constant components C13, R32 and R33. For asynchronous operation, the baud pulse duration is changed to 407 nanoseconds (48 CHAN) or 203 nanoseconds (96 CHAN). This is accomplished by enabling the 48-channel addm baud generator Q5 or the 96-channel baud generator Q6. These addm baud generators supply additional drive current to the 48-channel ddm baud generator and thus change the duration of the baud pulse output of A6 as required. When the ADDM TRAFFIC SELECT switch is in the 48 CHAN position, the input at pin 4 is +5v, diodes CR15 and CR16 are reverse biased and there is no current flow in resistor R28. Transistor Q6 has +5vdc at base and emitter and is at cutoff. The input at pin 5 is 0v (ground) and current flow through diodes CR13, CR14, R25, and R26 forward biases transistor Q5. Transistor Q5 delivers current through resistors R30 and R31 to A6 to change the baud pulse duration. When the ADDM TRAFFIC SELECT switch is in the 96 CHAN position the input at pin 4 is 0vdc and the input at pin 5 is +5vdc. Transistor Q5 is then turned off and Q6 is turned on and the 96-channel baud pulse is generated.

c. *Radio Digital Processor 1A12A10, Synchronous Mode (fig. 5-8 and 5-38).* Radio digital processor 1A12A10 receives the full baud, retimed pcm signal (1RPCM) from 1A12A9 and

converts it to half baud for cable system compatibility. The pcm signal is then combined with the orderwire signal and applied to the cable system.

(1) When the CABLE LOOP TEST switch (1A12A12AIS1) is in the NORMAL position, signals OTEST and OCLPCM are both logic one. Signals 1RPCM (waveform A, fig. 638) and 1R2304 (waveform B) are combined by NAND gate A7B. The full baud 1RPCM signal is converted to half baud at the output of A7B (waveform C, fig. 5-38). This signal is inverted by OR gate A4D (waveform D) and applied to pulse generator A2, which is a monostable multivibrator. When the output of A4D goes negative (low), the output of A2 goes negative for 217 nanoseconds (1/2-baud), then returns to high (waveform E, fig. 5-38). The output signal from A2 is inverted by A4C and applied to the cable output amplifier (waveform F, fig. 5-38).

(2) In the cable-to-radio direction of transmission, the pcm signal is sent to the modulator circuits of Transmitter, Radio T-1054/GRC-144 for transmission after being processed in digital data modem 1A12. This signal, inverted (OCLPCM from cable digital processor 1A12A4), is applied to radio digital processor 1A12A10. When the CABLE LOOP TEST switch 1A12A15A1S1 is placed in the TEST position, this from cable signal is substituted for the from radio pcm signal through OR gate A4D. Thus, under the test condition, the signal from the cable is returned directly to the cable as a means of testing the cable system.

(3) The pcm signal from A4C is amplified by cable output amplifier Q1 and transformer coupled to the cable circuit and the traffic detector.

(a) There are three cable simulation networks; each network provides attenuation equivalent to 1/4-mile of cable. They are added in the required increments to make the total length of actual and simulated cable equal one mile. A selector plug connects the required networks and also makes a connection to the applicable CABLE LG (MILES) indicators on the front panel. A similar arrangement is provided for cable digital regenerator 1A12A2 (para 2-5a) such that when both special connectors are plugged in to simulate the same length of cable, the associated CABLE LG (MILES) indicator is lighted (para 2-39d).

(b) At the secondary side of transformer T1, the pcm signal is combined with the orderwire signal and the cable direct current. The overvoltage shunt circuit protects circuits of radio digital processor 1A12A10 against input voltage surges from the cable.

(c) The traffic detector circuit of radio digital processor 1A12A10 generates signals ONOR and 1RPFALL. When signal 1RPCM is normal, if the CABLE LOOP TEST switch is in NORMAL position, signal 1RPCM is gated through A7B and following circuits into the secondary of T1. Signal ONOR output from the traffic detector is then logic one, signal 1RPFALL is logic zero, and the radio-to-cable pcm signal is transmitted through the cable. If the CABLE LOOP TEST switch is then placed in TEST position, signal 1RPCM is inhibited at A7B (logic zero at pin 6) but signal OCLPCM is gated through A4D. Signals ONOR and 1RPFALL are the same as above but now the cable loopback pcm signal is sent to the cable. When the radio-to-cable pcm signal (LRPCM) fails, if the CABLE LOOP TEST switch is in NORMAL position, there is no pcm signal into T1. Signal ONOR switches to logic zero and signal 1RPFALL switches to logic one (traffic failure). There is no pcm signal in the cable. If the CABLE LOOP TEST switch is then placed in TEST position, signal OCLPCM is gated through A4D. Signal ONOR is logic one, signal 1RPFALL is logic zero and the cable loopback pcm signal is sent to the cable. The logic state of signal ONOR affects operation of relay 1A12A-12A2TB1K1. See e below.

(4) Switch Logic. The switch logic circuits are for future application and are not used.

c.1 . *Radio Digital Processor 1A12A16, Asynchronous Mode.* (fig. 5-8.1 and 5-38.1). Radio digital processor 1A12A16 receives the full baud, retimed pcm signal (LRPCM) from 1A12A9 and converts it to half baud for cable system compatibility. The pcm signal is then combined with the orderwire signal and applied to the cable system.

(1) The function logic switch determines the output signal provided by 1A12A16. When the CABLE LOOP TEST switch (1A12A12A1S1) is in the NORMAL position, signal OTEST is logic 1 and signal OCLPCM is inactive and the input is a constant logic 1. When the CABLE LOOP TEST is in the TEST position, signal OTEST is logic zero and signal OCLPCM is active.

(a) When signals OTEST, TC1 and TC2 are all logic, the output of inverter A6D is logic 0. The outputs of NAND gates A6C and A4B are then fixed at logic 1, and NAND gate A5A has logic 1 at two inputs (pins 1 and 2). NAND gate ASB has logic 1 at pin 8 (OTEST) and the 1RPCM signal is gated through A5B by the

clock signal (OR4915). The output of the function logic switch at NAND gate A5A is the 1RPCM signal.

(b) When signal OTEST is logic 0 and signals TC1 and TC2 are logic 1, the output of NAND gate A5B provides a logic 1 at pin 3 of NAND gate A5A. Signal TC2 provides a logic 1 input to inverter A6C which then provides a logic 0 input to inverter A5C. Inverter A5C then provides the second fixed logic 1 at the input of A5A (pin 2). NAND gate A4B has a logic 1 at pin 6 from A6D and at pins 7 and 9 from TC1 and TC2. So signal OCLPCM passes through inverter A6B, and NAND gates A4B and A5A. The output of the function logic switch is the OCLPCM signal.

(c) When signals OTEST and TC1 are logic 0 and TC1 is logic 1, the outputs of NAND gates A5B and A4B are logic 1 because of the OTEST and TC1 signals, respectively. The output of NAND gate A5C is logic 1 because of signal OTEST, inverted in A6D. Thus NAND gate A5A has three logic 1 inputs and the output of the function logic switch is a fixed logic 0 (no signal).

(d) When the OTEST, TC1 and TC2 signals are all logic 0, NAND gate A5B provides a logic 1 input to NAND gate A5A at pin 3, and NAND gate A4B provides a logic 1 at pin 1. NAND gate A6A has a logic 1 at pin 1 so it gates the clock signal (OR49152) to the trigger input of flip-flop A3A. Flip-flop A3A divides the clock signal by two and sends a 2457.6 kHz signal to pin 11 of NAND gate A5C. This gate has logic 1 on pins 12 and 13 from signal TC2 inverted in A6C and signal OTEST inverted in A6D. So the 2457.6 kHz clock signal is the output of the function logic switch at NAND gate A5A.

(2) The output signal of the function logic switch is applied to the trigger input of monostable multivibrator A1. Monostable multivibrator A1 is the pulse width gate; it accurately sets the pcm signal pulse width at 407 nanosec (48-channel) or 203 nanosec (96-channel). It triggers on the positive-going edge of the trigger signal and the timing is determined by resistor R3 and capacitor C1. The output signal of A1 (waveform A, fig. 5-38.1) is applied through inverter A2B waveform B, fig. 5-38.1 to one input of NAND gates A2C (pin 10) and A2D (pin 12) in the bipolar cable driver. From A2B, the signal is also applied to the trigger input of flipflop A3B via NAND gate A2A (waveform C, fig. 5-38.1). Flip-flop A3B triggers on the positive going edge of the trigger signal and transfers the logic signal then present at input D to the TM 11-582069535 logic 1 output (pin 9) (waveform D, fig. 5-38.1). The, signal at the logic 0 output (pin 8) (waveform E, fig. 5-38.1) is always the

logical complement of the signal at pin 9. The signal status of pins 8 and 9 remains fixed until the next trigger pulse. The logic 0 output (pin 8) is connected to the D input (pin 12) of A3B and to pin 13 of NAND gate A2D (waveform E, fig. 5-38.1). The logic 1 output is connected to pin 9 of NAND gate A2C. When either A2C or A2D has logic 1 at both inputs, its output goes to logic 0 (ov). This condition can never occur for both NAND gates at the same time since they receive complementary inputs from A3B. When A2C has logic 1 at both inputs, A2D has a logic 0 at pin 13, so the output of A2C is Ov (waveform F, fig. 5-38.1) and the output of A2D is +5v (waveform G, fig. 538.1). The +5v output of A2D matches the +5v at the center tap of the primary of transformer T1, so no current flows between terminals 3 and 4. The ground at the output of A2C causes current to flow between terminals 1 and 2 from the +5v at the center tap. This induces a positive pulse in the secondary of T1 (waveform H, fig. 5-38.1). When conditions are reversed and A2C has a +5v output and A2D has ground output, a pulse of the opposite polarity is induced in the secondary of T1. Thus the standard logic pcm signal is converted into bipolar form. In figure 5-38.1 the logic 1 pulses of waveform A are labeled A through E and the corresponding bipolar pulses are identified by the same letter in waveform H.

(3) The bipolar pcm signal at the secondary of T1 is fed through the equalizer (cable simulation network). The overvoltage shunt circuit protects circuits of radio digital processor AA16 against input voltage surges from the cable. The pulse shaper circuit (L2-R14) improves the waveshape of the output signal. The orderwire and cable direct current signal (OW1, pin A) is connected through the pulse shaper and overvoltage circuits and combined with the pcm signal. The output signal, designated TOCX is routed to the TO CABLE jack, J5.

(4) The bipolar pcm signal is connected to the cable traffic circuit by means of an auxiliary secondary winding (pins 5 and 6) on transformer T1. The signal is then rectified and filtered in a voltage doubler rectifier filter circuit (C11, C12, CR7, CR8, R15 and R16). When traffic is active, the positive voltage output of the rectifier circuit forward biases transistor Q1. Current flow in the collector load resistor of Q1 (R17) then forward biases transistor Q2. Resistor R19 is the collector load resistor for Q2. The positive voltage developed across

R19 is applied through bias/current limiting resistors R20 and R21 to the bases of transistors Q3 and Q4. Transistor Q3 is turned on and the ONOR output signal is logic 0 (normal) because the +12vdc supply voltage is dropped across the collector load CR9 and R23. Transistor Q4 also turns on, lamp DS1 turns on and signal 1RPFALL is logic zero (normal). If there is no traffic activity, there is no voltage output from the rectifier and transistors Q1 through Q4 are all off. Signal ONOR is then logic 1 (alarm) and signal 1RPFALL is logic 1 (alarm). When Q4 is off, resistor R22 allows a small current to flow through lamp DS1 to keep the filament warm. This reduces the current surge in Q4 caused by lighting of DS1 when Q4 turns on

d. *Cable Digital Processor 1A12A4* (fig. 5-8 and 5-32) The radio-to-cable circuits portion of cable digital processor 1A12A4 is used only in the radio repeater mode of operation. Cable digital processor 1A12A4 receives the retimed pcm (1RPCM) signal from radio control-comparator 1A12A9 and converts the 1RPCM signal from standard logic levels to the levels required by the input circuits of Transmitter, Radio T-1054/GRC-144.

(1) The retimed radio-to-cable pcm signal (1RPCM) is applied through digital buffer 2 to level converter 2 and to alarm circuit 2. The level converter (R9, R10, R11) converts the signal voltages to the levels required by the modulator circuits of Transmitter, Radio T-1054/GRC-144. The output signal, radio repeat pcm (1RRPCM), is applied to the RADIO REPEATER OUTPUT connector.

(2) Alarm circuit 2 monitors the retimed pcm signal from the digital buffer. Operation of alarm circuit 2 is similar to operation of alarm circuit 1, described in paragraph 2-5c. If the pcm signal is detected, indicator

lamp DS2 in 1A12A4 is lighted green and the alarm signal output (radio repeater pcm failure, 1RRPFALL) is deactivated. If the retimed pcm signal is not detected, the alarm circuit causes the green indicator lamp to go out and activates the failure signal (1RRPFALL) which is applied to alarm monitor 1A12A5 or 1A12A15.

e. *Orderwire and Direct Current Path* (fig. 5-8 and 5-29). The orderwire portion of the from radio pcm and orderwire signal (FRPCM) is recovered in radio amplifier-detector 1A12A7. The orderwire output signal (RRØW) from 1A12A7 is sent to orderwire assembly 1A13 where it is distributed to the orderwire stations and routed back (cable ow in CCØWIN) to an amplifier 1A12A6. The amplified output of 1A12A6 (cable transmit ow, CCTØW) is applied to the primary of transformer 1A12A12A2T2. The direct current path from the cable-to-radio circuits is completed through the normally closed contacts of the fault locator relay (1A12A12A2BIK1). The fault locator relay is normally energized by a ground from the CABLE LOOP TEST switch (NORMAL position) or by a control signal (ON R) from radio digital processor 1A12A10. When the CABLE LOOP TEST switch is in NORMAL position, fault locator relay is energized; when the CABLE LOOP TEST switch is in TEST position the fault locator relay is deenergized. The position of the CABLE LOOP TEST switch determines the mode of operation of the cable-to-radio circuits of cable digital processor 1A12A4 (para 2-5c), the radio-to-cable circuits of alarm-monitor 1A12A5 or 1A12A15 (h below), and radio digital processor 1A12A10 or 1A12A16. The effect of the CABLE LOOP TEST switch on the operation of 1A12A10 or 1A12A16 is explained in c(3)(c) above; this information in relation to the relay is summarized in the following chart.

CABLE LOOP TEST switch position	pcm traffic	ONOR	IRPFALL	Relay	1A12A10 or 1A12A16 output signal
NORMAL	normal	logic zero	logic zero	energized	radio-to-cable pcm
Test	normal	logic zero	logic zero	not energized	cable loop-back pcm
NORMAL	failed	logic one	logic one	energized	no pcm
TEST	failed	logic one	logic one	not energized	cable loop-back pcm

With the fault locator relay deenergized, the resistor/capacitor/diode network on terminal board 1A12A12A2TB1 is switched into the direct current path and provides fault localizing information to Multiplexer TD-204/U at the other end of the cable system.

f. *Radio Amplifier-Detector 1A12A7* (fig. 5-8 and 5-35) Radio amplifier-detector 1A12A7 receives the

pcm/dc/orderwire (FRPCM) signal from Receiver, Radio R-1467/GRC-144 and the reshaped pcm signal (1RSPCM-2) from 1A12A8. The function of 1A12A7 is to recover the orderwire signal from the FRPCM signal (that is, eliminate the pcm component) and provide an amplified orderwire signal as output. The basic method used to accomplish this purpose is to

apply the two input signals (FRPCM and IRSPCM-2) to a subtractor. The output signal of the subtractor is the

difference between the input signals. This will be the orderwire signal.

**Change 2 2-20.3**

if the pcm components of the input signals are equal. The circuits of 1A12A7 (other than the subtractor and the audio output amplifier) are used to create this equality of pcm components at the subtractor inputs. The FRPCM (pcm plus orderwire) signal is passed through a low pass filter which eliminates the high frequency components of the pcm signal but passes some low frequency components. This signal is applied to one input of the subtractor. The pcm signal (1RSPCM-2) was separated from the FRPCM signal and reshaped in 1A12AS, so it is not the same as the pcm component of the FRPCM signal. To equalize for this, the amplitude, phase shift and attenuation characteristics of the pcm (1RSPCM-2) signal are modified so that they approximate the similar characteristics of the pcm component of the FRPCM signal. The 1RSPCM2 signal is also passed through a low pass filter. The characteristics of the pcm components of the input signals are then approximately equal. The output signal of the subtractor is applied to the audio amplifier and to a feedback circuit. The feedback circuit applies the output signal to the product detector circuit. If there is a residual pcm component in the output signal, it is combined with the 1RSIPCM-2 signal in the product detector. The output of the product detector, through the differential amplifier, controls the amplitude of the pcm (1RSPCM-2) signal input to the residual pcm component at the output of the subtractor to a minimum.

(1) The FRPCM signal from Receiver, Radio R-1467/GRC-144 is passed through a 50 kHz low-pass filter to remove high frequency components before processing. At the output side of the filter, the signal consists of orderwire plus residual pcm and noise components below 50 kHz. The filtered signal is applied to the noninverting input of the subtractor stage (differential amplifier A1).

(2) The 1RSPCM-1 signal is sliced by age slicer Q4. The amplitude of the agc slicer output signal is controlled so that it is the same amplitude as FRPCM signal (approximately 1 volt peak-to-peak). Agc slicer amplitude is controlled by a dc signal from differential amplifier Q2 and Q3. The dc signal is developed from the 1RSPCM-1 signal through a low-pass filter, buffer amplifier Q1 and the product detector and from the residual pcm from subtractor A1. The product of these signals produces a dc output from the rectifier and integration network which is applied to differential amplifier Q2 and Q3, which, in turn, controls agc slicer gain. The signal is then passed through a 50 kHz low-pass filter, to remove the very high frequency

components, and applied to emitter follower buffer amplifier Q5.

(3) The pcm signal is then applied to the radio simulation network where the low frequency components of the signal are phase shifted and attenuated in the same manner as were the low frequency components of the FRPCM signal during radio transmission. The radio simulation network consists of two sections: The first section provides for simulation of the low frequency phase shift and a portion of the attenuation characteristics of the radio; the second section provides the additional phase shift and attenuation required to properly simulate the radio characteristics. The output of the radio simulation network is applied to the second input of the subtractor (inverting input).

(4) The only difference between the two input signals applied to the subtractor is the orderwire signal which has been added to the FRPCM signal prior to radio transmission. The output of the subtractor stage therefore, is the orderwire signal plus a minimum residual pcm signal. The orderwire signal is amplified by the af amplifier stage (Q6, Q7, Q8). The audio amplifier has an adjustment for gain and a low-pass network to attenuate the residual pcm. The output of the amplifier (RRØW) is applied to orderwire assembly 1A13 for further processing. A level detector circuit at the output generates a dc voltage when the orderwire signal is active. The dc voltage is available at a test point for monitoring and testing purposes.

*g. AF Amplifier 1A12A6* (fig. 5-8 and 534). The radio-to-cable circuits of af amplifier 1A12A6 amplify the "cable ow in" signal (CCOWIN) for orderwire assembly 1A18. The radio-to-cable circuits of 1A12A6 are comprised of an input level control, an input amplifier, a lowpass filter with cutoff frequency of 2000 Hz and a power amplifier. The amplified output of 1A12A6, cable transmit ow (CCTOW), is applied to the primary side of transformer 1A12A12A2T2. A level detector circuit at the output generates a dc voltage when the orderwire signal is active. The dc voltage is available at a test point for monitoring and testing purposes.

*h. Alarm-Monitor, Synchronous Mode 1A12A5* (fig. 5-8 and 5-33). The radio-to-cable circuits of alarm monitor 1A1aA5 control the RADIO TO CABLE MODEM indicator on meter panel assembly 1A16A4 and the shelter mounted traffic out indicator. Two kinds of Signal are monitored by the radio-to-cable circuits: functional alarm sig-

nals from IA12A8 (IRRIFAIL), 1A1A9 (1RCFAIL), IA12A10 (1RPFAIL), and 1A12A4 (1RRPFAIL); and the radio traffic failure signal (1FRFAIL,) from 1A12A8. The functioning of these signals is similar to that described for cable-to-radio circuits (para 2-5f). That is, since the radio pcm signal is processed in sequence through the indicated circuits, a functional failure in any plug-in module causes that module and any modules following it in the processing sequence to activate the functional failure signal. Likewise, when the radio pcm signal (FRPCM) fails, all functional failure signals are activated. The radio-to-cable circuits use these signals to distinguish which kind of failure has occurred, functional or radio traffic failure.

(1) *Radio Traffic Normal.* When radio traffic is normal, signal 1FRFAIL (from 1A12AS) is logic zero and the output of inverter A8D is high. Relay driver transistor Q7 is turned on and output signal 1BPOW is at logic zero. The output signal (high) from A8D is inverted by negative OR gate A4D (input pin 12 of A4D is always high from switch S1A) and inverted again by A7D. Negative OR gate A1A, therefore, has a high input at pin 1, negative OR gate A4B has a high input at pin 6 and NAND gate A4A has a high input at pin 2.

(2) *Radio Traffic Failure.* When loss of the radio traffic signal occurs, signal LFRFAIL is logic one and the output of inverter A8D is low. Relay driver transistor A7 is turned off and output signal 1BPOW is at logic one. Signal 1BPOW is connected to orderwire assembly IA,13 and, when it is a logic one, activates a relay which causes the from radio (FRPCM) signal to be applied directly to orderwire assembly 1A13 instead of through digital data modem 1A12. This connection allows orderwire communications to be maintained when the radio pcm signal is lost. The output signal (low) from A8D is inverted first by A4D, and inverted again by A7D. Negative OR gate A1A, therefore, has a low input at pin 1; negative OR gate A4B has a low input at pin 6, and NAND gate A4A has a low input at pin 2.

(3) *No Functional Failure.* When there is no functional failure, the output signal of inverters A8A, A8B, A2C and A7 are all high and the corresponding inputs at negative OR gate A9 are high. The inputs to A9 from ASC and A8F are always high; A8C and A8E are not used. The signal at pin 3 of A9 is always high except when the CABLE LOOP TEST switch is in TEST position. When Radio Set AN/GRC144 is being used in the radio repeater mode, input signal ORRM is logic zero. This signal is inverted to logic one (high) by inverter A2D, and applied to AND gate A2C. Then if

1RRPFAIL is logic one (failure of radio repeat pcm signal), the output of A2C is low. When there is no functional failure, 1RRPFAIL is logic zero and A2C applies a high to A9. When Radio Set AN/ARC-144 is not in radio repeater mode, signal ORRM is logic one, and A2C then always applies a high to A9. With all input signals high, the output of A9 is low and A4A has a low at pin 1. The low output of A9 is inverted to a high by inverter A7E, so A4B has a high at pin 6 and A1A has a high at pin 13.

(4) *Functional Failure.* When a functional failure occurs, the output of at least one inverter (A8A, A8B, A2C, or A8E) switches to low and the output of A9 is then high. The output of A9 is also-high without a functional failure if the CABLE LOOP TEST switch is placed in TEST position. In either case, A4A has a high at pin 1. The high from A9 is inverted by A7E, so A4B has a low at pin 5 and A1A has a low at pin 18.

(5) *Radio Traffic Normal No Functional Failure.* When radio traffic is normal and there is no functional failure, the conditions of (1) and (3) above exist and operation is as follows:

(a) A4A has a high at pin 2 and a low at pin 1 and its output is high. Lamp driver Q1 is turned on and signal 1RFFL is logic zero. The high output of A4A is inverted to low by A3A, and lamp driver Q2 is turned off. Signal ORFFL is logic one and the RADIO TO CABLE MODEM indicator is lighted green.

(b) A4B has a high at both inputs and its output is low. Lamp driver Q3 is turned off and signal ORTFL is logic one. The low output from A4B is inverted by ASB and lamp driver Q4 is turned off. Signal IRTFL is logic zero and the traffic out indicator is lighted green.

(c) A1A has high inputs at pins 13 and 1. If there is no failure in the cable-to-radio circuits, the output of NAND gate A2B is high (para 2-5f(5)) so A1A has a high at pins 2 and 3. With all inputs high, the output of A1A is low and this is inverted to high by ASD. Transistor Q5 is turned on, Q6 is turned off and signal OMARY is high (no alarm).

(6) *Radio Traffic Normal-Functional Failure.* When radio traffic is normal and there is a functional failure, the conditions of (1) and (4) above exist and operation is as follows:

(a) Both inputs to A4A are high and its output is low. Lamp driver Q1 is turned off and signal IRFFL is logic one. The low output of A4A is inverted to low by A3A and lamp driver A2 is turned on. Signal ORFFL is logic zero. The RADIO TO CABLE MODEM indicator is lighted red.

(b) The inputs to A4B are high at pin 6 and low at pin 5. The output, therefore, is high. Lamp driver Q3 is turned on and signal ORTFL is logic zero. The high output from A4B is inverted by A3B and lamp driver Q4 is turned off. Signal 1RTFL is logic one. The traffic out indicator is lighted red.

(c) The inputs to A1A are low at pin 13, from A7E, when a radio-to-cable functional failure exists, or low at pin 2 and 3, from A2B, when a cable-to-radio functional failure exists (para 25f(6)). The output of A1A is high and this is inverted to low by A3D. Transistor Q5 is turned off, transistor Q6 is turned on, and signal OMARY is low (alarm condition).

(7) Radio Traffic Failure. When a radio traffic failure occurs (loss of the FRPCM signal), all functional failure signals are also affected and switch to logic one (high). The conditions of (2) and (4) above then exist and the relay driver circuit is activated as explained in (2) above. Other operation is as follows:

(a) The input signals to A4A are low at pin 2 and high at pin 1 and its output is high. Otherwise, operating conditions are as explained in (5Xa) above.

(b) Both inputs to A4B are low and its output is high. Otherwise, operating conditions are as explained in (6)(b) above.

(c) A1A has a low input at pin 1 and its output is high. Otherwise, operation is as explained in (6Xc) above.

(8) Switch S1. Alarm monitor 1A12A6 also contains switch S1 which is not used. Section SIC lights lamp DS1 when the switch is placed in the TEST position; but the lamp has no function. Section SIA applies +5V to A4D in either NORMAL or TEST position.

i. Alarm-Monitor LA12At Asynchronous Mode. (fig. 5.1 and 533.1). The radio-to-cable circuits of alarm monitor 2A control the RADIO TO CABLE MODEM indicator on meter panel assembly 1A16A4 and the shelter mounted traffic out indicator. Two kinds of signal are monitored by the radio-to-cable circuits: functional alarm signals from 1A12A8 (1RRIFAIL), 1A12A9 (1RCFAIL), U2A126 (1RPFFAIL), and 1A12A4 (1RRPFFAIL); and the radio traffic failure signal

(1FRFAIL) from 1A12A8. The functioning of these signals is similar to that described for cable-to-radio circuits (para 2-5f). That is, since the radio pcm signal is processed in sequence through the indicated circuits, a functional failure in any plug-in module causes that module and any modules following it in the processing sequence to activate the functional failure signal. Likewise, when the radio pcm signal (FRPCM) fails, all functional failure signals are activated. The radio-to-cable circuits use these signals to distinguish which kind of failure has occurred, functional or radio traffic failure.

(1) Radio Traffic Normal. When radio traffic is normal, signal 1FRFAIL (from 1A12A8) is logic zero and the output of inverter A6F is high. Relay driver transistor Q7 is turned on and output signal 1BPOW is at logic zero. NOR gate A8A has a high input at pin 1, NOR gate A3D has a high input at pin 12 and NAND gate A3C has a high input at pin 9.

(2) Radio Traffic Failure. When loss of the radio traffic signal occurs, signal IFRFAIL is logic one and the output of inverter A6F is low. Relay driver transistor A7 is turned off and output signal 1BPOW is a logic one. Signal 1BPOW is connected to orderwire assembly LA13 and, when it is a logic one, activates a relay which causes the from radio (FRPCM) signal to be applied directly to orderwire assembly 1A13 instead of through digital data modem 1A12. This connection allows orderwire communications to be maintained when the radio pcm signal is lost. NOR gate A8A has a low input at pin 1; NOR gate A3B has a low input at pin 12, and NAND gate A3C has a low input at pin 9.

(3) No Functional Failure. When there is no functional failure, the output signal of Inverters A5A, A5B, A3B and A5C are all high and the corresponding inputs at NOR gate A4 are high. The signal at pin 3 of A9 is always high except when the CABLE LOOP TEST switch is in TEST position. When Radio Set ANIGRC-144 is being used in the radio repeater mode, input signal ORRM is logic zero. This signal is inverted to logic one (high) by inverter A3A, and applied to NOR gate A3B. Then if IRRPFFAIL is logic one (failure of radio repeat pcm signal), the output of A3B is low. When there is no functional failure, 1RRPFFAIL is logic zero and A3B applies a high to A4. When Radio Set AN/GRC-144 is not in radio repeater mode, signal ORRM is logic one, and A3B then always applies a high to A4. With all input signals high, the output of A4 is low and A3C has a low at pin 8. The low output of A4 is inverted to a high by



inverter A5F, so A3D has a high at pin 13 and A8A has a high at pin 13.

(4) Functional Failure. When a functional failure occurs, the output of at least one inverter (A5A, AB, A5C, or A3B) switches to low and the output of A4 is then high. The output of A4 is also high without a functional failure if the CABLE LOOP TEST switch is placed in TEST position. In either case, A3C has a high at pin 8. The high from A4 is inverted by A5F, so A3D has a low at pin 13 and A8A has a low at pin 13.

(5) Radio Traffic Normal-No Functional Failure. When radio traffic is normal and there is no functional failure, the conditions of (1) and (3) above exist and operation is as follows:

(a) A3C has a high at pin 9 and a low at pin 8 and its output is high. Lamp driver Q1 is turned on and signal 1RFFL is logic zero. The high output of A3C is inverted to low by A5E, and lamp driver Q2 is turned off. Signal ORFFL is logic one and the RADIO TO CABLE MODEM indicator is lighted green.

(b) A3D has a high at both inputs and its output is low. Lamp driver Q3 is turned off and signal ORTFL is logic one. The low output from A3D is inverted by A5D and lamp driver Q4 is turned off. Signal IRTFL is logic zero and the traffic out indicator is lighted green.

(c) A8A has high inputs at pins 13 and 1. If there is no failure in the cable-to-radio circuits, the output of NAND gate A2D is high (para 2-5f(5)) so A8A has a high at pins 2 and 3. With all inputs high, the output of A8A is low and this is inverted to high by A9E. Transistor Q5 is turned on, Q6 is turned off and signal OMARY is high (no alarm) .

(6) Radio Traffic Normal Functional Failure. When radio traffic is normal and there is a functional

failure, the conditions of (1) and (4) above exist and operation is as follows:

(a) Both inputs to A3C are high and its output is low. Lamp driver Q1 is turned off and signal 1RFFL is logic one. The low output of A3C is inverted to low by A5E and lamp driver Q2 is turned on. Signal ORFFL is logic zero. The RADIO TO CABLE MODEM indicator is lighted red.

(b) The inputs to A3D are high at pin 12 and low at pin 13. The output, therefore, is high. Lamp driver Q3 is turned on and signal ORTFL is logic zero. The high output from A3D is inverted by A5D and lamp driver Q4 is turned off. Signal 1RTFL is logic one. The traffic out indicator is lighted red.

(c) The inputs to A8A are low at pin 13, from A5F, when a radio-to-cable functional failure exists, or low at pins 2 and 3, from A7D, when a cable to-radio functional failure exists (para 2-5f(6)). The output of A8A is high and this is inverted to low by A9E. Transistor Q5 is turned off, transistor Q6 is turned on, and signal OMARY is low (alarm condition).

(7) Radio Traffic Failure. When a radio traffic failure occurs (loss of the FRPCM signal), all functional failure signals are also affected and switch to logic one (high). The conditions of (2) and (4) above then exist and the relay driver circuit is activated as explained in (2) above. Other operation is as follows:

(a) The input signals to A3C are low at pin 9 and high at pin 8 and its output is high. Otherwise, operating conditions are as explained in (5)(a) above.

(b) Both inputs to A3D are low and its output is high. Otherwise, operating conditions are as explained in (6)(b) above.

(c) A8A has a low input at pin -J 1 and its output is high. Otherwise, operation is as explained in (6)(c) above.

2-6.1 Digital Data Combiner 1A12 Radio-To-Cable Circuits Functional Block Diagram Description

The functional relationships between radio-to-cable plug-in components and J chassis circuits of digital data combiner 1A12 are shown in figure 5-8.3. Each plug-in component is functionalized and the main signal paths (heavy lines) are shown in figure 5-8.3 as well as control and alarm functions.

a. Combiner, Alarm-Status 1A12A2 (fig. 5-8.3 and 5-38.4). Combiner, alarm-status -11252 receives radio-to-cable status input signals as listed on the following page. It processes these signals to generate output status signals that are routed to destinations indicated in the chart. The CLB signal is from LOOP TEST switch 1A12S3; CLB is logic 1 when S3 is not in DGM position and logic 0 when it is in DGM position. All other input signals listed are logic 1 for normal status and logic 0 for fault status. Normal logic states for -- output signals are listed in the chart below All input signals listed are radio-to-cable monitor signals except EQPT FAIL. This is a cable-to-radio signal (para 2.5. lb) and it is used here for an inhibit function.

(1) The FR FAIL signal is applied directly at U2A-1 and through inverter U6B at U6C-5, U7D-4, U3C-11, UIOC-9 and to cable-to-radio monitor circuits (para 2.5.1b). FR FAIL is normally logic 0 and U6B-4 is logic 1. This signal, twice inverted in U6C and U7C, applies logic 1 (open circuit) at relay K2 and K2 is deenergized (normal). The relay contacts are open circuit and logic 1 (normal) is sent to the OCU. If FR FAIL changes to logic 1, the logic signals reverse, K2 is energized and logic 0 (fault) signal is sent to the OCU. Signal 1 BPOWS at U7D-13 is normally logic A. This signal is used only in analog orderwire mode. It is connected through P1-H to AVOW switch 1A1252 at 52-1. The switch arm (52.2) is connected to OW SEL switch 1A12S1 at S1-4 and the arm (S1-C2) is connected through P1-5 to route the signal to orderwire assembly 1A13 at module 1A1343 (para 2-8e). The 1 BPOWS signal is connected-through this path only when S2 (AVOW) is in the NORMAL position and S1 t(OW SEL) is in the ANLG position. For any other combination of positions of S1 and S2, the output at P1-H is open circuit. If the FR FAIL signal goes to fault status (logic 1), 1 BPOWS is also logic 1 and, in analog orderwire mode, orderwire assembly 1A13 generates an alarm signal that lights the CNTRL ALARM red indicator at 1A15A8.

Input Signals			Output Signals			
MNEMONIC	PIN	Source Module	MNEMONIC	PIN	Destination	Logic Level (Normal)
FR FAIL	P1-9	A8				
CVDOW RPPL FAIL	P1-D	A6	ORFFL	P1-F	1A15A8	1
OWDMX FAIL	P1-4	A7	1RFFL	P1-6	1A15A8	0
SLICER FAIL	P1-C	A8	ORTFL	P1-18	External	1
DRPLL FAIL	P1-3	A5	1RTFL	P1-17	External	0
DT FAIL	P1-V	A4				
EQPT FAIL	P1-M	A4	TFC OUT	P1-12	Not Used	1
			1BPOWS	P1-H	1A13	0
			RS-NO	P1-10	OCU	1
DSCRM FAIL	P1-N	A3	1RTFL	P1-17	External	0
CLB	P1-Z	-	RS-NC	P1-11	OCU	1

(2) Input signals at U4A and U11D are logic 0 (normal) or logic 1 (fault). All FAIL signals including DSCRM FAIL at the input to U3B are logic 1 (normal) or logic 0 (fault) and the resulting output signal at U3B-6 for either logic state is indicated in the chart below in the MONITORED SIGNAL column. U3C monitors the summary signal from U3B-6 and U3A monitors the DT FAIL signal. U3C and U3A are each inhibited for one position of the LOOP TEST switch as indicated in the chart. When U3C is not inhibited by the CLB signal (U3C-10), the signal at U3C-8 shows the logic state of

the monitored signal at U3C-9. The fault state is listed twice. If FR FAIL (U3C-11) is normal, U3C-8 is logic 0 (fault) for monitored signal fault status. But if FR FAIL is logic 1 (fault), U3C is inhibited by logic 0 at pin 11 and U3C-8 is logic 1 regardless of the logic state of the monitored signal (U3C-9). Operation of U3A is similar as indicated in the chart below. For U3A, logic 0 at pin 13 inhibits fault status indication at U3A-12 when EQPT FAIL signal is logic 1 (fault). The output signals at U3C-8 and U3A-12 are summarized by U2C and U11C.

LOOP TEST SWITCH	Monitored Signal		U3C				U3A				U2C -10	U11C
	U3B-6	OR P1-V	9	10	11	8	1	2	13	12		
Not in DGM position	Normal	1	0	1	1	1	Inhibited by logic 0 at pin 1. U3A-12 is logic 1.				0	1
	Fault	0	1	1	1	0					1	0
	Fault	0	1	1	0	1					0	1
In DGM position	Normal	1	Inhibited by logic 0 at pin 10 U3C-8 is logic 1				1	0	1	1	0	1
	Fault	0					1	1	1	0	1	0
	Fault	0					1	1	0	1	0	1

(3) Input signals at U4B are normally logic 0 and the signal at UIOD-12 is logic 1. If either input at U4B fails, logic 0 is applied at UIOD-12. U4B monitors orderwire signals; the output signal at U11C reflects the status of data signals. These are the inputs to UOD and the output at U1OD-II is connected at U1OC-100. This signal reflects the status of monitored data and orderwire signals. The FR FAIL signal at U1OC-9 is an inhibit signal. If FR FAIL is normal, the signal at U1OC-9 is logic and the signal at U1OC-8 can show the status of the signal at U1OD-II. If FR FAIL is logic 1, U1OC-8 is

held at logic 1 by a logic 0 at U1OC-9. The chart below summarizes the logic action. When U1OC-8 is logic 1 (normally), signal 1RFFL is logic 0. This signal is routed through P1-6 to meter panel 1A1548. Logic 0 causes RADIO TO CABLE MODEM indicator 1A15A8DS2 (green) to light. At the same time, signal ORFFL is logic 1. This signal through P1-F holds indicator 1A15A80S4 (red) off. If the signal at U1OC-8 changes to logic 0, 1RFFL is logic 1 (green lamp off) and ORFFL is logic 0 (red lamp on). The output at U1OC-8 is also used in cable-to-radio monitor circuits (para 2-5 lb).

Data Signal (U11C)	Orderwire Signal (U4B-4)	U100		U1OC		
		13	12	10	9	8
Normal	Normal	1	1	0	1	1
Fault	Normal	0	1	1	1	0
Normal	Fault	1	0	1	1	0
FR FAIL fault status		U1OC inhibited by logic 0 at pin 9. U1OC-8 is held at logic 1.				

(4) Inputs at U2D are both normally logic 0 and U2D-II is logic 1. The signal at U2D-II can go to logic 0 only when EQPT FAIL signal is logic 1 (fault) while LOOP TEST switch 1A12S3 is not in DGM position. Similarly the signal at U2A-3 is logic 0 only when FR FAIL is logic 1 (fault) while S3 is not in DGM position. These two signals with the signal from U11C ((2) above) are inputs to U8B. Normally U8B has three logic 1 inputs and U8B-6 is logic 0. Signal ORTFL is then logic 1 and signal IRTFL is logic 0. These signals are routed through P1-17 and -18 to external traffic alarm locations. If any input at U8B changes to logic 0 (fault), U8B-6 changes to logic 1 and ORTFL and IRTFL reverse logic states. The signal from U8B-6, inverted in U11F, is routed to P1-12 (TFC OUT) and is used for test purposes only.

b. Digital Interface Buffer 1A12A4 (fig. 5-8.3 and 5-38.6). Digital buffer interface 1A12A4 receives the retimed, radio recovered descrambled data signal from module A3. In A4 this signal is routed to the DGM normally. When in radio loopback mode, it is returned to the remote site by radio. Operation of the circuits of A4 for these functions is explained in paragraph 2.5.1d.

c. Digital Traffic Retimer 1A12A5 (fig. 5-8.3 and 5.38-7). The function of digital traffic retimer 1A12A5 is to retime the SLICED DATA signal received from module A8 at P1-2 and -3. The retimed data output signal (RCOVD DATA, P1-M) and the data clock signal (RCOVD TMG, PI-12) are routed to module A4. The retimed data signal (REG DATA, PI-10) is also routed to module A8. The data clock signal is synchronized to the timing of the input data signal transitions in a phase lock loop. The phase lock loop and retimed data signals are monitored to generate a status signal. The status signal (DRPLL FAIL, P1-L) is routed to module A2. Input

signals from DATA RATE SEL (MB) switch 1A12S4 are used to set the operating data rate of module A5.

(1) One of four external crystals (Y1 through Y4) is used to set the operating frequency of oscillator U18. The selected crystal is connected into the oscillator circuit when the corresponding control diode (CR1/Y1, CR2/Y2, CR3/Y3 or CR4/Y4) is forward biased. Circuit operation for selection of crystal Y1 is typical. When the signal at U2A-2 is logic 1 (crystal Y1 not selected), +12 vdc through R1, R6 and L1 is applied to the anode of CR1. U2 is an open collector type IC, and the logic 1 at U2A-2 is a high impedance. With a high impedance at the junction of R2 and R7, the +12 vdc is also applied through R2, R7, L2 and L3 to the cathode of CR1. CR1 is reverse biased and crystal Y1 is isolated from the oscillator circuit. When the signal at U2A-2 switches to logic 0 ((5) below), the junction of R2 and R7 is grounded. Now diode CR1 is forward biased with the cathode connected to ground through L3, L2 and R7 but with the anode still connected to +12 vdc. CR1 then provides a low impedance path between C8 and L7 and crystal Y1 is connected into the oscillator circuit through C7 and C8. Variable inductor L7 is a trimmer used to fine tune the oscillator frequency. Inductors L1, L2, and L3 isolate the dc control circuit of CR1 from the oscillator circuit. Crystals Y2, Y3, and Y4 are isolated by their control diodes when crystal Y1 is selected. These crystals are selected in a similar manner when U2B, U2C, or U2D is switched to logic 0 by the crystal select logic circuits.

(2) The frequency of oscillator U18, operating with selected crystal, is phase controlled by varactor diode CR5. The capacitance of CR5 is controlled by a dc signal generated by the phase lock loop and applied at the anode. The

control voltage from the output of the phase lock at U4-10 is applied to CR5 through an isolating and filtering network (CR8, CR9, C26, R25, R28, L12). Zener diodes CR8 and CR9 limit the range of this voltage to protect varactor diode CR5. A bias voltage, applied at the cathode of CR5, sets its operating (pull-in) range. This voltage is derived from +12 vdc through R27, CR7 and filter capacitor C27. It is applied to CR5 through an isolating and filtering network (CR6, C25, R24, R26, and L11).

(3) The operating frequency of oscillator U18 is determined by the crystal selected. The output signal of U18 must be divided by some factor to provide the clock signal at the operating data rate. This is required because the crystal frequency is higher than the data rate and because crystals Y1, Y2, and Y4 are used for more than one data rate. These functions are discussed in (4) through (6) below. The clock signal must be synchronized to the timing of the data signal. This function is discussed in (8) and (9) below.

(4) Data rate select logic circuits U2, U6, U7, UO1 and U11 under control of signals from DATA RATE SEL (MB) switch IA12S4 provide the two required rate select functions. Gates U2, U7, and U11 provide the crystal select function. Gates U6 and U10 provide for division of the oscillator signal by the factor required to produce the selected data rate clock. Dual sinewave outputs at U18-2 and -3 are coupled through C4/R15 and C5/R16 to squarewave generator U19. The inputs at U19-4 and -5 balanced to ground by R12/R13. Dual complementary squarewave outputs at U19-13 and -4 are applied to the divider circuits and to clock gate U14.

(5) Crystal Y1 is used for three data rates, Y2 for four data rates, Y3 for one data rate and Y4 for two data rates. The input signals from DATA RATE SEL (MB) switch IA12S4 at the pins listed in the crystal select chart below are connected to the rate select logic gates. Each of these input signals is logic 1 (high), except the input corresponding to the selected rate. This signal is logic 0 (low). The input lines have pull-up resistors (U8) which

CRYSTAL SELECT CHART							
DATA RATE SEL (MB/S) switch inputs	Selected rate MB/S	Selected crystal	Divide ratio	Crystal select (Logic 0 selects)			
				Y1 U2A-2	Y2 U2B-4	Y3 U2C-6	Y4 U2D-8
P1-B	1.024	Y1 16.384 MHz	16	0	1	0	1
P1-C	2.048		8	0	1	1	1
P1-A	4.096		4	0	1	1	1
P1-6	1.152	Y2 18.432 MHz	16	1	0	1	1
P1-D	1.536		12	1	0	1	1
P1-5	2.304		8	1	0	1	1
P1-E	4.608		4	1	0	1	1
P1-J	4.9152	Y3 19.6608 MHz	4	1	1	0	1
P1-9	9.36	Y4 18.72 MHz	2	1	1	1	0
P1-F	18.72		1	1	1	1	0

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apply the voltage for the logic 1 state to the rate select logic gates. The chart shows the crystal selected for each rate and the corresponding division factor. The last four columns of the chart show the output logic states of the final crystal select gates. Operation of the crystal select logic for rate 1.024 is typical. When 1A12S4 is set for this rate, the signal at P1-B and at U7A-1 is logic 0. The signals from 1A12S4 at all other inputs are logic 1. Logic 1 from U7A-6 is inverted by U2A and the logic 0 at U2A-2 selects crystal Y1 as discussed in (1) above. Operation of the crystal select logic for any other rate or crystal is similar.

(6) The rate select signals at gates U6 and U10 determine the division factor that will be used and thus the data rate (clock) signal. The division factor for each rate is given in the chart below along with the logic states of the signals at the precount inputs at US. These inputs in D, C, B, A order are the binary code for the precount given in decimal form in the last column. When data rate 1.024 is selected, the signals at U6-11 and -13 are logic 0 and at U6-1, -2, -3, -4, -5 and -10 are logic 1. The signal at U10-1 is logic 1. U10-2 and U6-6, -8 and -12 then apply precount inputs at U5 as shown

in the chart for rate 1.024. The precount is 8. This means that U5 starts each count cycle (for rate 1.024) at a count of 8 (binary 1000) and it reaches full count (binary 1111) 7 counts later. Each time the count reaches binary 1111, U5 produces a positive pulse (RC) at pin 15. The duration of this pulse is one cycle of the CLK input at U5-2 from U19. The signal at UiOD-8 is then logic 0. On the eighth clock pulse, the logic 0 from UiOD-8 resets U5 at pin 9. This injects the precount again for the start of the next count cycle. Thus, for rate 1.024, a precount of 8 is stored in U5, and an output pulse at U5-15 is produced for every 8 cycles of the CLK signal at U5-2. The signal from U5-15 is gated through U11C in synchronism with the oscillator signal from U-19 by the signal at U10C-6. Divider U15 divides the signal from U5 by 2. Thus the oscillator signal has been divided by 8 in U5 and by 2 in U15. So it has been divided by 16 as indicated in the chart for rate 1.024. Operation of the division factor select circuits and US/U15 is similar for any other data rate. The data rate (clock) signal is gated through U14 which is a dual, 2-pole electronic switch. For all data rates from 1.024 to 9.36, the signal from U15-5 at U14-10 is connected

DIVISION FACTOR CHART

Selected Rate (MB/S)	Division Factor	Precount Gates					Precount (decimal)
		D (fixed)	C U6A-12	B U6C-8	A U10A-2	U6B-6	
1.024	16	1	0	0	0	1	8
2.048	8	1	1	0	0	0	12
4.096	4	1	1	1	0	1	14
1.152	16	1	0	0	0	1	8
1.536	12	1	0	1	0	1	10
2.304	8	1	1	0	0	0	12
4.608	4	1	1	1	0	1	14
4.9152	4	1	1	1	0	1	14
9.36	2	1	1	1	1	1	15
18.72	1	1	1	1	0	1	14

through to U14-8; and the signal from U15-6 at U14-5 is connected through to U14-6. For rate 18.72, the clock signal is taken directly from U19 (it is not divided) and applied at U14-1 and -2. For all rates, the outputs at U14-8 and -6 are complementary clock signals at the selected rate. Switching operation of U14 is controlled by the signals at pins 3, 4, 9, and 13. For all rates except 18.72, the signals at U14-4 and -9 are logic 1; they switch to logic 0 for rate 18.72. For all rates except 18.72 the signals at U14-3 and -13 are logic 0; they switch to logic 1 for rate 18.72.

(7) The balanced SLICED DATA signal from module A8 at P1-2 and -3 is converted to TTL level in line receiver U3. Resistors R18 and R19 are line terminations. The data signal from U3-13 is retimed in U12A by the clock signal from U14-6. The retimed data signal at U12A-6 is routed through buffers U17A and U13D to module A4 (REGEN DATA, PI-M) and to module A8 (REG DATA, PI-10). The clock signal from U14-8 is routed through buffer U17B to module A4 (RCOVD TMG, P1-12).

(8) U12A and B, U13A, B, and C and U16A comprise a phase detector. The input signals at U13B are the data signal from U3-13 and the retimed data signal (inverted) from U12A-6. Buffer U13A provides a slight delay for the signal at U13B-4 to compensate for the delay incurred by the signal at U13B-5 in passing through U12A. If the clock signal from U14-6 is exactly in phase with transitions of the data signal from U3-13, the signals at U13B-4 and -5 will always be opposites (logic 0 and logic 1) and U13B-6 will be logic 1. If there is a phase difference, the signals at U13B-4 and -5 will sometimes be the same. U13B-6 will be logic 0 at those times. This is the phase detector error signal and its duration is proportional to the phase difference between data and clock signals. The retimed data signals from U12A-5 and U12B-9 are applied to U13C and the output signal at U13C-8 is ended with the clock signal in U16A. The output at U16A-6 is a constant width negative pulse

occurring at clock rate. This is the REF signal. When the ERR signal goes positive, it charges C35 through CR10 and when the REF signal goes negative it discharges C35 through CR11. The net charge in C35 at any time is proportional to the phase difference between the ERR and REF signal pulse widths. This difference is proportional to the phase difference between the data and clock signals.

(9) A reference voltage (+2 Vdc) is applied to pin 5 of voltage comparator U4. The voltage is developed from +5 Vdc through R37, R38 and R39 and is filtered by C36. Variable resistor R39 is adjusted to set the level. The voltage across C35 is applied to inverting input U4-4 through isolating resistor R34. The output voltage at U4-10 varies in the range +4 Vdc for the normal range of phase difference in the data and clock signals. This signal is applied to varactor diode CR5 through a low pass filter as described in (2) above.

(10) The output at U4-10 is also applied to voltage comparators U9A and B which are used as an out-of-range detector. Resistor network R41, R44 and R45 applies reference voltages of +8 Vdc at U9A-4 and -8 vdc at U9B-II. For the normal range of phase difference, the outputs at U9A-15 and U9B-8 are high. This signal is applied to monostable U20B which is normally reset with logic 0 at U20B-12. If the phase difference exceeds the normal limits, the outputs at U9A and B switch to low. This transition sets U208B and U20B-12 changes to logic 0. The signal from U20B-12 is applied to electronic switch U1. When the signal at U1-5 and -10 is logic 1, U1 is off and has no effect on U4. When U1-5 and -10 switch to logic 0, U1-13 and -14 are connected together and also U1-I and -2. The short at U1-1 and -2 discharges the feedback network of U4; the short at U1-13 and -14 applies +5 vdc through R31 and R34 to U4-4. The output voltage at U4-10 is then approximately 0 Vdc and oscillator U18 is driven to center frequency. The phase detector starts searching again

for sync between data and clock signals. After 150 msec, U20B resets, U1 turns off and operation of U4 returns to normal.

(11) The retimed data signal from U12B-8 is applied to activity detector U20A. As long as the data signal is active, U20(A is set and logic 1 from U20A-13, inverted in U10E, makes the DRPLL FAIL signal logic 0 (normal). Logic 0 from U20A-4, inverted to logic 1 in U16B, holds indicator CR12 off (normal). If the data signal fails, U20A times out and resets. If an out-of-range condition is detected by U20B ((10) above), a logic 0 at U20A-2 resets U20A. In either case, the logic signals reverse: DRPLL FAIL is logic 1 (fault) and indicator CR12 turns on.

d. Digital Orderwire Retimer (1A12A6 (fig. 5-8.3 and 5-38.8). The principal function of digital orderwire retimer IA12A8 is to retime the CDVOW signal. To accomplish this, a CVDOW clock signal is generated in a phase lock loop by extracting timing from the CVDOW signal ((2), (3), and (4) below). The RETIMED CVDOW and CLOCK SIGNALS are routed to module A7. The retimed.CVDOW signal and the phase lock loop are monitored to generate a status signal. The status signal is routed to module A2. These activities occur only in digital orderwire mode.

(1) The timing is extracted from the CVDOW signal and used in a phase lock loop to synchronize the frequency of oscillator U1. Oscillator U1 generates a 64 kHz signal at U1-13. This signal is inverted to U3C and divided by 2 in U6A to provide the 32 kHz clock C1. The 64 kHz signal is applied through buffer U2D to U6B. U2D provides a time delay equal to that of U3C, so inputs to U6A and 8 are exactly 180 degrees out-of-phase. The signal at U6B-9 is 32 kHz clock C2; it lags 90 degrees behind clock C1. The SLICED CVDOW signal (from module A8) is inverted in L2C and applied

to USA and U2A. The CVDOW signal is retimed in U5A and 8 Clock C1. The output at U5B-9 is connected to UIIA-3. The signal at UIIA-2 is normally logic 1 ((7) below) and the RETIMED CVDOW signal at UIIA-1 is routed through PI-12 to module A7.

(2) IC's U2 and U3 comprise the transitional phase detector. The input signals at U2A are the CVDOW signal and the same signal inverted (U2A-2) from U5B-6. The signal at U5A-6 is clocked through USA by clock C1. If clock C1 is exactly in phase with transitions of the CVDOW signal, the signals at U2A-1 and -2 will always be opposites (logic 1 and logic 0) and U2A-3 will be logic 1. If there is a phase difference between clock C1 and CVDOW transitions, the signals at U2A-1 and -2 will sometimes be the same. U2A-3 will be logic 0 at those times. This is the phase detector error signal and its duration is proportional to the phase difference between CVDOW and clock C1. The retimed CVDOW signals from USA-5 and U5B-9 are applied to U2B and the output is ANDed with clock C2 in U3B. This is the REF signal with constant width equal to one cycle at 32 kHz. When the ERR signal (U3A-12) goes positive, it charges capacitor C8 through CR1, and when the REF signal (U3B-6) goes negative it discharges C8 through CR2. The net charge in C8 at any time is proportional to the difference in width between the ERR and REF pulses. This difference is proportional to the phase difference between clock C1 and the timing of the CVDOW signal.

(3) A reference voltage (2.5 Vdc) is applied to pin 5 of voltage comparator U4. The voltage is developed from +5 vdc through R7, R8 and R9 and is filtered by C9. Variable resistor R9 is adjusted to set the level. The voltage across C8 is applied to inverting input V4-4 through isolating resistor R10. The output voltage at U4-10 is approximately Change 6



zero when the CVDOW signal and the 32 kHz clock are the phase; it is applied to oscillator U1 through R37 at pin 6. This control voltage causes the frequency of U1 to track with CVDOW timing. If the ERR pulse is wider than the FEF pulse, the net charge in C8 and the voltage at U4-4 increases. The output at U4-10 increases. The output at L4-10 then decreases and causes the oscillator frequency to increase. The opposite reactions occur when the ERR pulse width decreases. U4 also acts as a low pass filter to smooth out changes in the oscillator control signal. The signal at U4-10 normally varies between  $\pm 7$  Vdc.

(4) The output signal from U10-4 is also applied to the inverting input of voltage comparator U7B which is used as an analog inverter. U7B and U7A together act as an out-of-limits detector. When the phase difference between CVDOW and the 32 kHz clock is within limits, the output at U4-10 is within the range +7 Vdc. When this voltage is in the minus range, it is passed by diode CR5. When it is in the positive range, it is inverted by U7B and passed by diode CR4. In either case, normally, a negative voltage of 7 volts or less is applied through R18 to U7A-1. The normal output voltage at U7A-12 is -12 Vdc. This voltage and a supply of -12 Vdc at R30 combine through the resistor network R28 through R33 and CR6 to produce a signal between 0 and -7 Vdc at U7A-2. As long as the control voltage from U4-10 is within the +7 Vdc limits, the signal at U7A-12 is -12 Vdc. If this voltage exceeds these limits, the output at U7A-12 switches to +12 Vdc. The voltage at U7A-2 then switches to -1 Vdc. The signal at U7A-12 is connected through R32 and inverter U9A to the clear input (pin 11) of status monitor U8 ((7) below).

(5) The output at U7A-12 is applied through R13 to transistor Q1, the out-of-range reset control. Normally the signal applied to Q1 is -12 Vdc; Q1 is off

and has no effect on U4. When an out-of-range condition is detected, the +12 Vdc signal from U7A-12 turns on Q1. With Q1 on, a low impedance bypass path through Q1 shorts the feedback network (R11, C11, C12) of U4. This sets U4 to mid-range and the phase detector starts hunting again for sync between CVDOW and the 32 kHz clock. As the varying output of U4 is processed by U7A and U7B, the input level at U7A must fall within +1 Vdc ((5) above) before the output at U7A-12 returns to the normal -12 Vdc. When this occurs, Q1 turns off and normal phase detector loop operation resumes.

(6) The retimed CVDOW signal from U5B-9 ((2) above) is applied to status monitor U8 and to U11A. U8 is in the set state as long as the CVDOW signal is active. Logic 0 from U8-12 at UIIA-2 has no effect and U11A passes the CVDOW signal. In digital orderwire mode, OW SEL switch IA12SI (P-10) applies logic 0 at U11B, so logic 1 from U8-5 holds the output of U11B at Logic 0. Signal CVDOW RPLL FAIL is then logic 0 (normal) and status indicator CR10 is off. If the CVDOW signals fails, U8 times out and resets, so logic 1 from U8-12 clamps UIIA-1 at logic 0. U8-5 applies logic 0 at U11B, which has logic 0 input also from PI-10. The U11B output and signal CVDOW RPLL FAIL are then logic 1 (fault), and indicator CR10 turns on. If an out-of-range condition is detected ((5) above), U8 is reset and the same fault indications occur as those described for failure of the CVDOW signal. In analog orderwire mode, the signal at U18B from PI-10 is logic 1. The output of U11B is then clamped in the logic 0 state (normal) and status indicator CR10 is off.

e. Digital Orderwire Demultiplexer IA1247 (fig. 5-8.3 and 5.9). Digital orderwire demultiplexer IA127 receives the retimed CVDOW signal and its 32 kHz clock signal from module A6. In module

A7, the CVDOW signal is demultiplexed to obtain its two components, 16 Kb/s CVOW and 2 Kb/s DOW. The DVOW and DOW signals are routed to the OCU. These output signals are monitored to generate status signal OWDMMX FAIL WHICH is routed to module A2. Module A7 is used only in digital orderwire mode. A control signal from OW SEL switch IA12SI inhibits the status signal and prevents an alarm status indication in analog orderwire mode when there is no CVDOW signal.

(1) In the 32 kb/s CVDOW signal, alternate bits are DVOW and DOW signal bits. The sequence of alternate bits comprising the DVOW signal is random and unpredictable, but the sequence of alternate bits comprising the DOW signal has known characteristics. These characteristics of the DOW signal provide the working basis for the demultiplexing process.

(a) The DVOW bit rate is 16 kb/s so alternate bits in the 32 kb/s CVDOW signal are DVOW bits.

(b) The DOW signal bit rate is 2 kb/s but one DOW bit is redundantly represented by eight consecutive alternate bits in the 32 kb/s CVDOW signal.

(c) The redundant bit pattern for DOW logic 0 is 01010101, and for logic 1, the pattern is 10101010. Thus the DOW bits in CVDOW are alternating I's and O's, except at DOW signal transitions. At transitions from logic 0 to logic 1, there are two consecutive I's (the last bit of the DOW logic 0 and the first bit of the logic 1). At transitions from logic 1 to logic 0, there are two consecutive O's in the DOW signal (remember they are alternate bits in CVDOW) mark DOW signal transitions because that is the only time this condition can occur.

(d) The DVOW demultiplexing process is basically simple because alternate bits in the 32 kb/s

CVDOW signal are DVOW bits. The CVDOW signal is applied to a demultiplexing flip-flop. It is clocked through the flip-flop by a 16 kHz signal derived from the 32 kHz CVDOW clock. Since the clocking rate (16 kb/s), is one-half the CVDOW bit rate (32 kb/s), one or the other of the two alternate sequences of bits in CVDOW is passed through the demultiplexing flip-flop. If the 16 kHz clock is phased to the wrong sequence of bits in CVDOW (DOW instead of DVOW), a simple 180 degree phase inversion of the 16 kHz clock will phase it to the correct bit sequence.

(e) The DOW demultiplexing process is more complex. The CVDOW signal is clocked through the DOW demultiplexing flip-flop by a 2 kHz clock derived from the 32 kHz CVDOW clock. Since the clocking rate (2 kHz) is one-sixteenth the CVDOW bit rate (32 kb/s), only every 16th bit in CVDOW is passed by the DOW demultiplexing flip-flop. To assure the correct DOW signal, the 2 kHz clock must be synced to DOW signal transitions ((b) and (c) above). Then, for DOW logic 0, the demultiplexing flip-flop will pass a logic 0 (the first bit in the redundant DOW logic 0 sequence). For logic 1, it passed a logic 1 (first bit in the redundant DOW logic 1 sequence).

(f) Both demultiplexing processes ((s) and (e) above) depend on first establishing the correct phase for the 16 kHz.

(2) The CVDOW signal (P1-B, from module A6) is inverted in U4 and applied to 5-stage shift register U2/U1. The 32 kHz signal (P1-H, from A6) is inverted in U4 and applied to the shift register, to a divide-by-2 flip-flop at U1-9, and to CLK input (pin 14) of up/down counter U3. The output at U5-1 (16 kHz) is applied to pin 1 of Exclusive-OR gate U5. The signal at U5-5 is normally logic 1. If the signal at U5-4 (and U1-3 and

U5-2) is logic 0, U5-6 is logic 1 and the 32 kHz signal continuously clocks this signal, maintaining U1-3 and U5-2 at logic 0. If U5-4 is logic 1, U5-6 is logic 0 and U1-3 and U5-2 are maintained at logic 1. The signal at U5-1 is passed through to U5-3 unchanged when U5-2 is logic 1 and it is inverted when U5-2 is logic 0. This is in the inverting phase control for the 16 kHz clock ((1) (d) above). The phase control signal from U1-3 will be logic 1 or logic 0, depending on the signal at U5-5 ((5) below). The 16 kHz signal is applied through P1-2 and P1-D to U6-2.

(3) The CD)OW signal is continuously clocked through the shift register, shifting CVDOW bits in sequence through the five stages. The logic states of the outputs of the five shift register stages for each clock cycle are the states of the last five bits shifted in. Alternate bits in the shift register (stages 1, 3, 5) are compared in two Exclusive OR gates (U5). When stages 1 and 3 have opposite (logic 0 and logic 1) inputs, U5-5 is logic 1 and U4-8 is logic 0. When stages 3 and 5 have opposite inputs, U5-11 is logic 1. When U5-8 and U5-11 are both logic 1, U6-8 and U3-5 are logic 0.

(4) The signal at U6-8 is connected through P1-6 and P1-I to the count control input of up/down counter U3 at pin 5. The signal at U3-4 (EN) must be logic 0 to enable operation of the counter. On positive half cycles of the 32 kHz signal at U3-14, if the signal at U3-4 is logic 0, the counter counts. If the signal at U3-5 is logic 0, it counts up one count; if U3-5 is logic 1, it counts down. The signal at U3-12 (MIN/MAX) is logic 1 for count 0 or 15 and logic 0 for counts 1 through 14. The signal at U3-7 is logic 1 at count 15 only, otherwise it is logic 0. When the count in U3 reaches 15, U3 is inhibited for up-counting ((6) below) but it can count down. Thus, unless the count is 15, U6-11 applies logic 1 at U6-1. Then, during each positive half cycle of the

16 kHz clock, logic 0 at U6-3 and U3-4 enables U3. U3 is in count enable state only during half cycles of the 16 kHz clock and the CLK (U3-14) and UP/DN (U3-5) signals are at a 32 kHz rate. This means that U3 counts only alternate pulses from U6-8. The pulses counted therefore correspond either to DVOW or DOW in the CVDOW signal. While U3 is operating with any count from 1 to 14, U3-12 and U3-7 are both logic 0. U6-12 and U6-13 are then both logic 0 and U6-11 and U6-1 are logic 1. The 16 kHz clock is passed by U6-3 to U3-4. As counter U3 is enabled for each positive half cycle of the 16 kHz signal, U3 counts pulses from U6-8. The signal at U6-4 (from U3-12 through P1-5 and P1-C) is logic 0, so U6-6 applies logic 1 at U5-5. Flip-flop U1-3 then applies either logic 1 or logic 0 at U5-2 and selects a phase of the 16 kHz signal ((2) above).

(5) If the 16 kHz clock phase is such that DVOW bits are being sampled at U6-8, counter U3 will count up and down at random. However, the DVOW signal does not have the constant one-zero sequence that U5-8 and U5-11 are designed to detect so the trend will be to count down. While the count in U3 is varying anywhere from 1 to 14, U3-12 and U3-7 are both logic 0 and logic 1 is maintained at U5-5 as explained in (2) and (4) above. The 16 kHz clock phase remains the same. When the count reaches 0, U3-12 goes to logic 0 but U3-7 is still logic 0. So U6-11 remains logic 1 and the counter can still count ((4) above). But logic 1 at U6-4 switches U6-6 to logic 0 for one half cycle of the 16 kHz signal through U4-4. During this half cycle, one cycle of 32 kHz occurs at U1-9. Since U5-5 has changed and therefore U5-6 has changed, the signals at U1-3 and U5-2 switch from logic 0 to logic 1 or the reverse. Either way the phase of the 16 kHz clock at U5-3 is reversed. Since we started by assuming a 16 kHz clock phase, such that DVOW bits were being sampled, the 180

degree phase-shifted 16 kHz clock must be sampling DOW bits. Since DOW bits alternate between 1 and 0, U6-8 will apply more logic 0's at U3-5 than logic 1's and U3 will quickly count up to 15. While the count is anywhere from 1 to 14, conditions are explained in paragraph (4) above. The logic states of the counter signals and control gates are given in the chart below for the three kinds of counter states.

(6) When the count reaches 15, U3-12 and U3-7 are both logic 1. U6-12 and U6-13 are then logic 1

and U6-11 and U6-1 are logic 0. The logic 0 at U6-1 clamps U6-3 at logic 1 and counter U3 is disabled for up counting.

(7) The 32 Kb/s CVDOW signal is applied at pin 2 of DVOW demultiplexer U7. The 16 KHz signal, inverted U4-2, clocks the CVDOW signal through to U7-5. The 16 kHz clocking rate assures that only every other bit in DVOW appears at U7-5. When the correct 16 kHz clock phase has been selected, these will be DVOW bits.

Count	U3			U6						U4
	Pin 12	Pin 7	Pin 4	Pin 12	Pin 13	Pin 11	Pin 1	Pin 3	Pin 6	Pin 4
0	1	0	0	1	0	1	1	clocking	0	1 (clock)
1 to 14	0	0	0	0	0	1	1	clocking	1	1 (clock)
15	1	1	1	1	1	0	0	1	1	0

(8) The 16 kHz signal from U5-3 is divided by 8 in ring counter U10 to provide the 2 kHz signal to demultiplex the DOW signal. However, the 2 kHz signal must be phased to transitions in the DOW signal. Inverter U4-8 provides the phase information and U12 provides the phase control of U10. Assuming the 16 kHz signal has been set to the correct phase ((5) above), U5-9 and U5-10 are sampling DOW bits. At DOW transitions, U5-9 and U5-10 are both logic 1 or both logic 0 ((1) (c) above). At that time, logic 0 at U5-

8, inverted in U4, is applied as logic 1 at U12-10. This action is clocked by one cycle of the 52 kHz signal at U2, but the 32 kHz signal is applied at U12-11. Thus the DOW transition signal (U4-8) always goes to logic 1 (U12-10) in coincidence with rising edges (logic 1) of the 16 kHz and 32 kHz signal at U12-9 and U12-11. So U12-8 applies a reset pulse to U10 every time a DOW transition is detected. This action synchronizes the 2 kHz signal to DOW transitions.

(9) The DVDOW signal is applied to pin 12 of DOW demultiplexer U7 and the 2 kHz signal is applied at pin 11. The redundant DOW bits in the CVDOW signal start with logic 0 for DOW logic 0 and with logic 1 for DOW logic 1 ((1)(c) above). U7 transfers the logic state of the signal at pin 12 to pin 9 only at the rising edge of the clock signal at pin 11. Since the 2 kHz signal is synchronized to DOW transitions ((8) above) this means that only the first bit in the redundant DOW signal is passed through U7. Thus, the correct DOW bit values are demultiplexed.

(10) The DVOW data and, timing signals are converted to balanced signals in line driver U9. Resistors R1 through R5, C3 and CR1 balance the signals to ground. The DOW data and timing signals are similarly processed in U8. The output signals are routed to the OCU. The signal at PI-17 is from OW SEL switch IA12SI. In digital mode, this signal is logic 0 and the signal at U13-2 enables U8, U9 and U12. Thus for digital mode, module A7 is operational. In analog orderwire mode, the signal at PI-17 is logic 1. Logic 0 from U13-2 then inhibits all data and timing signal outputs and prevents an alarm indication.

(11) The DVOW data and timing signals are applied to monitor U11. As long as both signals are active, U11-5 applies logic 1 at U12-3. Similarly as long as the CVDOW and the 2 kHz (DOW) timing signals are active, U11-13 applies logic 1 at U12-5. U12-6 then applies logic 0 at U12-13. The resulting logic 1 at U12-12 is inverted in U13 and the OWDMX FAIL signal is logic 0 (normal). This signal, inverted at U13-12 holds status indicator CR off. If any data or timing signal fails these conditions are reversed.

f. Digital Regenerator 1A12A8 (fig. 5-8.3 and 5-38.10). Digital regenerator IA12A8 receives the composite data/OW signal from the radio (P1-17) and separates the data and orderwire signals. The data

signal is routed to module A5; the orderwire signal is routed to module A6. The retimed, regenerated data signal is returned from A5 to A8 and used in the separation of the orderwire signal from the data signal. Status signals SLICER FAIL and FR FAIL are routed to module A2.

(1) The composite data/OW signal is applied to X4 amplifier U9. Resistor R39 is a line termination and R40 is used to adjust the input level to U9 to obtain a level of 4 volts peak-to-peak at the output. The amplified composite data/OW signal must be processed to separate the data and orderwire signals. The output at U9-11 is connected to U6 and U10 for data separation ((2) below) and to low pass filter (LPF), U4B or orderwire separation ((5) below). Output signals are taken from U6 or from radio signal activity monitoring ((8) below).

(2) U6 and associated circuitry comprise a peak-to-peak tracking threshold circuit. One transistor in U6 has +12 V applied at the collector (U6-1) through R46. The other transistor has -12 V applied at the collector (U6-7) through R48. The composite data/orderwire signal from U9-11 is applied at U6-2 and U6-6. The peak-to-peak values of this signal vary with changes in the data and the orderwire signal components. Thus its average value also varies. To slice the signal precisely at data signal transitions, it is necessary to determine the average (transition) level. As the signal varies between positive and negative values, the transistors in U6 are alternately turned on. When the signal is positive, base U6-2 is forward biased and capacitor C48 is charged from ground through C48, U6-3, U6-1, and R46. When the signal is negative, base U6-6 is forward biased and C47 charged from -12 V through R48, U6-7, U6-5 and C47 to ground. The voltages developed across the capacitors are of opposite polarities and they track the varying negative (C47) and

positive (C48) peak levels of the composite data/orderwire signal. The voltage at the junction of R49 and R50 is the algebraic sum of the voltages across capacitors C47/C48. The input at U9-6 is adjusted (R40) for a maximum peak-to-peak level of 4 volts at U9-11. The corresponding average value at the junction of R49 and R50 is 2.6 volts (max.). This signal is applied as a reference voltage at the inverting input (pin 5) of comparator/slicer U10 to set the slicing level. The from radio signal (U9-11) is applied at U10-4. As the signal at U10-4 varies above and below the average (reference) signal at U10-5, U10 slices the signal at data transitions and provides the balanced data signal at U10-13 and -14. Center slicing between peaks of the from radio signal regenerates the data signal because its amplitude is relatively large compared to the amplitude of the orderwire signal. The output signals at U10-13 and -14 are balanced to ground through resistors R58, R59, R61, and R62 and routed to module A5 at P1-K and -L.

(3) Simple filtering is not sufficient to accomplish separation of the orderwire from the composite data/OW signal. This is principally because the low frequency components of the data signal occupy the same part of the frequency spectrum as the orderwire signal. The system used to effect the separation takes advantage of the fact that the data and orderwire signals are independent variables and that the data signal is easily regenerated (2) above). The basic function of the orderwire extraction process is accomplished in subtractor U4A. One input to U4A is the composite data/OW signal with the high frequency components filtered out. The other input is derived from the retimed, regenerated data only signal (from A5) with the high frequency components filtered out by an identical filter. If the two input signals to subtractor U4A are matched in low frequency data components, their

difference (subtraction) will yield a "clean" orderwire signal. However, using just the filtered data only signal as the second input to the subtractor is not sufficient to assure a "clean" orderwire signal, because the from radio signal may vary in amplitude. To compensate for this variable, an automatic gain servo loop is used to generate the second input to the subtractor. In the servo loop, the LF data signal is analog multiplied times the orderwire plus LF data signal. In the resultant signal, the (LF data)<sup>2</sup> component contains a positive average value that can be used as a control signal to set the input level of the second signal at the subtractor as required. With a level-controlled input, the subtractor output signal tracks in the proper direction to maintain maximum LF data component cancellation.

(4) The composite data/OW signal from U9-II is applied to a low pass filter (LPF) comprised of U4B (the active element) and R36, R37, R38, C33 and C34. The cutoff frequency is 22 kHz (3 dB down). The output at U4B-100 (LF data plus orderwire) is applied through C38 and R55 to subtractor U4A at pin 1. The input at U4A-2 is the filtered data only signal. Derivation of this signal is explained in (5) below. The output at U4A-12 is the difference between these two input signals (input at pin 1 minus input at pin 2).

(5) The retimed, regenerated data only signal (from A5) is applied at U8B-3 and U8A-1. The signal from U8A-2 is passed through LPF U18B (identical to LPF U4B, (4) above) and amplified in X3 amplifier U1A. The signal at U1A-12, approximately fixed in level, is applied to analog multiplier U5. A second input to U5 (at pin 1) is supplied by the output of U4A ((4) above). The signal is applied through coupling network C39/R66. This is the orderwire signal with a residual level of the LF data signal. These signals are analog multiplied in U5. The output at U5-4 is

passed through a low pass filter (R28, C26, C27, CR4 with cutoff frequency approximately 1 Hz) and applied to X180 amplifier U7A. The output of U7A is a dc signal proportional to the residual data component in the signal from U4A-12. The output at U7A-12 is applied through a coupling network (R19, R21, C19) to LPF U7B (identical to LPF U4B, (4) above). The regenerated data signal (7U88-4) is also coupled at this point. The AGC voltage from U7A regulates the level of the input signal to LPF U7B. The filtered and AGC level-controlled data only signal output of LPF U7B is finally the required second input to subtractor U4A. The feedback signal from the subtractor output (U4A-12) into the servo loop at U5-1 provides for maximum cancellation of the data component. The output signal at U4A-12 is then the required "clean" orderwire signal. The signal at U8E-12 is normally high (logic 1) and U8E is isolated from the servo loop ((8) below).

(6) In digital orderwire mode, the output signal at U4A-12 is the CVDOW signal; in analog orderwire mode it is the AVOW signal. The CVDOW signal is applied through R54 to CVDOW slicer U3A at pin 3 and through a low pass filter (cutoff frequency 10 Hz) at U3A-4. In U3A the CVDOW signal is center sliced and the regenerated CVDOW output signal is routed (PI-I) to module A6. In orderwire mode, the unfiltered AVOW signal output at U4A-12 is routed (P1-3) to module A6.

(7) Status monitor monostable U12B monitors activity of the SLICED DATA signal (U10-13) and U12A monitors activity of the SLICED CVDOW signal (U3A-15). As long as monitored signals are active, U12A and B are held in the set state with logic 1 at U12B-5 and U12A-13. OW SEL switch 1A12S1 applies a control signal (PI-10) through inverter U8 to CVDOW monitor U12A. In digital orderwire mode, signal AVOW/DVOW is logic 0 and the signal at U8-10

is logic 1 U8 then has no effect and U12A operates normally. In analog orderwire mode, signal AVOW/DVOW is logic 1 and U8-10 applies a constant logic 0 at U12A-2. With no input signal activity, U12A times out and resets, but the constant logic 1 at U11C-9 holds the output U11C-10 at logic 0. This prevents a CVDOW fail indication in analog orderwire mode, since then there is no CVDOW signal. Nor gate U11A can still process the monitor signal from U12B normally. For digital orderwire mode, with normal activity of monitored signals, U12A and B are set. U11C then has logic 0 at pin 9 and logic 1 at pin 8. U11C-10 applies logic 0 at U11A-2 and U128-12 applies logic 0 at U11A-3. U11A-1 is then logic 1 and U11B-4 and status signal SLICER FAIL are both logic 0 (normal). This signal inverted in U8D holds indicator CR7 off. This condition is shown in the first line of the chart on the following page for DGTL position. The chart shows the logic states of the monitor circuits for normal and fail conditions and for both positions of the OW SEL switch.

(8) Differential amplifier U2 and voltage comparator U3 monitor the from radio signal activity and generate status signal FR FAIL (P1-2). The peak tracking signals from U6 are applied to differential amplifier U2. The output signal at U2-6 is the voltage difference between positive and negative peaks. As explained in (2) above, this voltage is a maximum 2.6 V. It varies with the from radio signal but is always present as long as the from radio signal is active. A reference voltage derived from +5 vdc through R7, R8 and R9 is applied to voltage comparator U3 at pin 11. It is set to a level of +1 Vdc by adjustment of R8. As long as the voltage at U3-12 is more positive than the voltage at U3-11, the output signal at U3-8 is ground (logic 0). Signal FR FAIL is then logic 0 (normal) and the output at U8E-12 is logic 1 ((5) above). If from radio signal activity fails, the output signal at U3-8 changes to high impedance and +5 Vdc through pull-up

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resistor R10 makes FR FAIL signal logic 1 (fault). At the same time, U8E-12 changes to logic 0 and cuts off the

input at U4A-1 (through U7B). Since the from radio signal failed, there is no input at U4A-2 and no output.

OW SEL (Sl)	U11C		U11A		U11B	U8D	CR7	Condition
	pin 8	pin 9	pin 2	pin 3	pin 4	pin 8		
DGTL	1	0	0	0	0	1	off	normal
position	0	0	1	0	1	0	on	CVDOW fail
	1	0	0	1	1	0	on	data fail
ANLG	0	1	0	0	0	1	off	normal
position	0	1	0	1	1	0	on	data fail

**2-7. Orderwire Assembly 1A13 Block Diagram Descriptions**

Operational or maintenance activities between the distant radio station, Radio Set AN/GRC-144, and terminal equipment (through orderwire) are provided by a single orderwire channel operated on a party-line basis. Orderwire assembly 1A13 provides duplex telephone communication between the orderwire stations by interconnecting signals from four different sources. These four sources are Handset H-156/U, Telephone Set TA-312/PT, the radio equipment (transmitter orderwire output and recovered orderwire or orderwire, pcm bypass inputs), and the through orderwire (TO CABLE output and FROM CABLE input). Orderwire assembly 1A13 also provides alarm

monitoring circuits, and input to a speaker monitor, in-band signaling at 1.6 kHz, a 1.1 kHz test tone, and orderwire fault detection circuits (para 2-8, 2-9). Orderwire assembly 1A13 is comprised of five daughter board assemblies (IA13A1-IA13A6) and chassis mounted components. The daughter board assemblies contain both discrete components (transistors, resistors, etc.) and integrated circuits (IC's).

**2-8. Orderwire Assembly 1A13 Signal Distribution Block Diagram Description (fig. 5-9)**

a. Duplex (transmit and receive) orderwire signal paths connecting the distant radio sta



tion, Radio Set AN/GRC-144, and terminal equipment are shown. Input orderwire signals, recovered orderwire, orderwire (pcm bypass), the remote telephone (Telephone Set TA-312/PT), and Handset H-156/U are shown entering the orderwire circuits on the left-hand side of the diagram. Output orderwire signals, to Handset H-156/U, through orderwire transmit to cable, to remote telephone, and to transmitter, are shown leaving the orderwire circuits on the righthand side of the diagram. The through orderwire receive (FROM CABLE) input signal is received by cable from the terminal equipment and the through orderwire transmit (TO CABLE) output signal is sent by cable to the terminal equipment. The recovered orderwire or orderwire (pcm bypass) input signal is received by the antenna and Receiver, R-1467(P)/GIRC144(V) from the distant radio station and the transmitter orderwire output signal is sent by Transmitter, T-1054 (P)/GC:-144(V), and antenna to the distant radio station. The internal orderwire circuit connections are such that a signal originating at one of the four inputs is distributed to the other three outputs but not to the associated output. For example, the through orderwire receive (FROM CABLE) input signal is distributed to the transmitter orderwire, Handset H-156/U, and the remote telephone outputs but not to the through orderwire transmit (TO CABLE) output.

b. To illustrate signal distribution through the orderwire assembly, assume that a signal is applied from remote telephone output. The signal passes through hybrid transformer IA13A7TB1T1 and peak limiter B (integrated circuit A3) on 1A13A5 and is distributed as follows: (1) To the loudspeaker through IC amplifier A2 on 1A13A4, the speaker volume control on the meter panel and IC amplifier A2 on IA13A4, the speaker volume control on the meter panel and IC amplifier A2 on IA13A2.

(2) To Handset H-156/U receive through IC amplifier A2 and filter FL1 on 1A13A4.

(3) To Transmitter, T-1054(P)/GRC-144(V) through IC amplifiers A5 and A4, filter FL1 and transformer T1 on 1A13A5.

(4) To through orderwire transmit (TO CABLE) through IC amplifier A5 on IA13A5, and IC amplifier A1, filter FL1, and transformer T1 on IA13A3.

c. Assume that a signal is applied from Handset H-166/U output. The signal is applied to peak limiter A (integrated circuit A2) and to sidetone amplifier Q2 on 1A13A5. The output of sidetone amplifier Q2 is applied to the handset's receive element to provide sidetone.

The signal output of peak limiter A is distributed as follows:

(1) To the remote telephone through IC amplifier A2 and filter FL2 on 1A13A3, and hybrid transformer IA13A7TB1T1.

(2) To the through orderwire transmit (TO CABLE) through IC amplifier A5 on IA13A5, and IC amplifier A1, filter FL1, and transformer T1 on 1A13A3.

(3) To Transmitter, T-1054(P)/GC-144(VY) through IC amplifier A5 and A4, filter FL1, and transformer T1 on IA13A5.

d. Assume that the through orderwire receive signal is applied to the orderwire circuits. The signal is distributed as follows:

(1) To the loudspeaker through transformer T1 and IC amplifiers A1 and A2 on IA13A4, the speaker volume control on meter panel assembly IA15A8, and IC amplifier A2 on IA13A2.

(2) To Handset H-166/U through transformer T1, IC amplifiers A1 and A2, and filter FL1 on IA13A4.

(3) To Transmitter, Radio T-1054/GRC-144 through transformer IA13A4T1, and IC amplifier A4, filter FL1, and transformer T1 on 1A13A5.

(4) To the remote telephone through transformer T1 and IC amplifier A1 on 1A13A4, IC amplifier A2 and filter FL12 on IA13A3, the hybrid transformer IA13A7TB1T1.

e. For normal operating conditions, relay K1 on IA13A3 is energized, allowing the recovered orderwire signal (the orderwire signal from the distant radio station) to enter the orderwire circuits. However, if the recovered orderwire sensing signal is lost (pcm alarm condition), relay K1 becomes deenergized and the orderwire (pcm bypass) signal enters the circuits to maintain orderwire communications. In either case, the recovered orderwire signal or the orderwire (pcm bypass) signal passes through contacts of relay K1 on 1A13A3 and is distributed as follows:

(1) To the loudspeaker through IC amplifiers A1 and A2 on 1A13A4, the speaker volume control on the meter panel, and IC amplifier A2 on IA13A2.

(2) To Handset H-156/U through IC amplifiers A1 and A2, and filter FL1 on IA13A4.

(3) To the remote telephone through IC amplifier A1 on 1A13A4, IC amplifier A2 and filter FL2 on IA13A3, and hybrid transformer IA13A7TB1T1.

(4) To the through orderwire transmit (TO CABLE) through IC amplifier A1, filter FL1, and transformer T1 on 1A13A3.

f. The 1.6 kHz monitor (integrated circuits A3 and A4) on 1A13A4 detects the in-band signaling tone (1.6 kHz) when it is present on any of the inputs and causes relay K1 on 1A13A4 to become energized. With K1 energized, the signal is directed to the loudspeaker passing through IC amplifiers (A1 and/or A2) and contacts of relay K1 on 1A13A4 and IC amplifier A2 on 1A13A2. Note that with K1 energized the speaker volume control is bypassed. Energizing K1 also changes the RING indicator color from green to amber.

g. Signaling tone is generated locally by pressing the RING pushbutton located on meter panel assembly

1A15A8. When the RING pushbutton is depressed, ground is applied to the 1.6 kHz oscillator (Q1) on 1A13A5 causing oscillations and making 1.6 kHz tone available at the output of the oscillator. The 1.6 kHz oscillator tone is distributed through IC amplifier A1 on 1A13A5 as follows:

(1) To the loudspeaker through closed contacts of the RING switch, peak limiter B (integrated circuit A3) on 1A13A5, IC amplifier A2 and closed contacts of relay K1 on 1A13A4, and IC amplifier A2 on 1A-13A2.

(2) To the loudspeaker through emitter follower Q5 and IC amplifier A2 on 1A13A2.

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(3) To Handset H-1156/U through closed contacts of the RING switch, peak limiter B (integrated circuit IA3) on 1A13A5, and IC amplifier A2 and filter FL1 on 1A13A4.

(4) To the remote telephone through emitter follower Q4 on 1A13A2 and hybrid transformer 1A13A7TB1T1.

(5) To Transmitter, Radio T-1054/GRC144 through closed contacts of the RING switch, and peak limiter B, IC amplifiers A5, A4, filter FL1, and transformer T1 on 1A13A6.

(6) To through orderwire transmit (TO CABLE) through closed contacts of the RING switch, peak limiter B and IC amplifier A5 on 1A113A5, IC amplifier AI, filter FL1, and transformer T1 on 1A13AS.

h. Test tone is generated by depressing the TEST TONE pushbutton switch located on the orderwire assembly front panel. When the TEST TONE pushbutton is depressed, ground is applied to the 1.1 kHz oscillator Q7 on 1A18A2 causing oscillation and making 1.1 kHz test tone available at the output of the oscillator. The 1.1 kHz test tone is amplified by IC amplifier AI on 1A13A2, passes through contacts of the depressed TEST TONE switch, and is distributed as follows:

(1) To Handset H-156/U through sidetone amplifier Q2 on 1A13BA5.

(2) To the remote telephone through peak limiter A (integrated circuit A2) on 1A13A5, IC amplifier A2 and filter FL2 on 1A13A3, and hybrid transformer 1A13A71TB1T1.

(3) To Transmitter, Radio T-1054-GRC144 through peak limiter A, IC amplifiers A5 and A4, filter FL1, and transformer T1 on 1A13A6.

(4) To the through orderwire transmit (TO CABLE) through peak limiter A and IC amplifier A5 on 1A13A5, and IC amplifier AI, filter FL1, and transformer T1 on 1A13A3.

i. OR gate circuits A and B on 1A13A2 monitor summary alarm signal inputs from the R11467/RC-144 (rcvr elm), the T-1054/GRC-144 (rcvr aim), and digital data modem IA12 (pcm aim). A fault in the monitored equipment results in a grounded alarm input to the OR gate circuits. OR gate A, CR 6-CR 9, controls multivibrator circuit Q13 and OR gate BX, OR-CR5 controls transistor switch Q6. When one of the alarm input signal becomes grounded, the transistor switch is activated causing the CNTRL ALARM indication on

meter panel assembly 1A16A8 to change from a green to a red indication. The grounded alarm input signal also activates multivibrator circuit Q1-Q3. When activated, the multivibrator alternately triggers the 1.1 kHz oscillator Q7 on 1A13A2 and the 1.6 kHz oscillator Q1 on 1A13A5 into operation. The 1.1 kHz oscillator is connected to the 1.6 kHz tone output of the 1.6 kHz oscillator through contacts of the TEST TONE and RING switches. The alternating 1.1/1.6 kHz tone is distributed to the loudspeaker on meter panel assembly 1A16A8 and to the remote telephone to provide an audible indication that a fault has occurred. The 1.1/1.6 kHz tone is distributed to the loudspeaker by emitter follower Q5 and IC amplifier A2 on 1A13A2. The 1.1/1.6 kHz tone is sent to the remote telephone through emitter follower Q4 on 1A13A2 and hybrid transformer 1A13A7TB1T1. Momentarily depressing the RESET switch on the transmitter panel or an external AUDIBLE ALARM DISABLE switch (shelter mounted) silences the loudspeaker alarm by disabling multivibrator. The CNTRL ALARM indicator on the meter panel assembly 1A15A8 remains lighted red indicating a fault still exists. The CNTRL ALARM indicator will turn green only after the fault is removed.

## 2-9. Orderwire Assembly IA13 Fault Detection Circuits Block Diagram Description (fig. 5-10))

a. The test circuits consist of MODULE TEST selector switch 1A13A1S1, 4.02 kHz oscillator IA13AIQ1 and IC amplifier 1A13AIAI, transformer 1A13AIT1, 4.02 kHz monitor IA13A1'Q2 and IC amplifier 1A13AIA2, and light switch assembly 1A13A1S2 which contains the MODULE TEST monitor indicator. Figure 510 is arranged for left to right signal flow with the test input circuits on the left and the test output circuits on the right.

b. With the MODULE TEST selector switch set to position 1, the module fault detector circuits are tested. The output of the 4.02 kHz oscillator is connected to the 4.02 kHz monitor through contacts S1,E-1 and SIE5 of the selector switch and contacts of the MODULE TEST indicator press-to-test switch. The 4.02 kHz monitor converts the 4.02 kHz signal into a dc output voltage which biases the lamp driver in light switch assembly 1A13A1S2 off. With the lamp driver biased off, the MODULE TEST indicator is extinguished indicating that the fault detection circuits are operating normally. Depressing the MODULE TEST indicator (press-to-test),

grounds the 4.02 kHz monitor input thus removing its output voltage. This causes the lamp driver to be biased on and the MODULE TEST indicator conducts and glows red.

c. To test IC amplifier 1 (IA1SA A5), the MODULE TEST selector switch is set to position 2, connecting the 4.02 kHz oscillator output signal through selector switch contact S1C-2 to one input IC amplifier 1. This signal is designated +4.02 kHz. The 4.02 kHz oscillator output signal is also connected through transformer T<sub>i</sub> and selector switch contact SID-2 to the output input of amplifier 1. Transformer T1 reverses the phase of the signal which is designated -4.02 kHz. The output signal level of amplifier 1' is applied to 4.02 kHz monitor Q2 through contact S18-2 of the selector switch and the

MODULE TEST press-to-test switch. If the output signal level of amplifier 1 is normal, the lamp driver is biased off. Thus, the MODULE TEST indicator is extinguished indicating amplifier 1 is operating normally. However, if the output signal level of amplifier 1 is low, the 4.02 kHz monitor cannot develop a dc voltage sufficient to bias the lamp driver off. With the lamp driver biased on, the MODULE TEST indicator lights red indicating that amplifier 1 is defective.

d. Amplifiers 2 through 6, the peak limiters, and the speaker amplifier are tested in the same manner as described above for amplifier 1. The selector switch positions and input and output contacts associated with each test are listed in the following chart.

Module test selector switch (S1) position	Input selector switch contacts			Circuits tested	Output selector switch contacts
	+4.02 kHz	-4.02 kHz	Ground		
1	S1E-5			Fault detection circuits (1A13A1Q1, 1A13A1A1, 1A13A1S2, 1A13A1Q2, 1A13A1A2)	
2	S1C-2	S1D-2		Amplifier 1 (1A13A5A5)	S1B-2
3	S1C-3	S1D-3		Amplifier 2 (1A13A6A2)	S1B-3
4	S1C-4	S1D-4		Amplifier 3 (1A13A3A1)	S1B-4
5	S1C-5	S1D-5		Amplifier 4 (1A13A4A1)	S1B-5
6	S1C-6	S1D-6		Amplifier 5 (1A13A5A4)	S1B-6
7	S1C-7	S1D-7		Amplifier 6 (1A13A4A2)	S1B-7
8	S1C-8	E1D-8		Peak limiters (1A13A5A2 and A9)	S1B-8
9	S1C-9			Speaker Amplifier (1A13A2A2)	S1B-9
10			S1E-2, -10	1.6 kHz oscillator (1A13A5Q1)	S1A-10
11			S1E-3, -11	1.1 kHz oscillator (1A13A2Q7)	S1A-11
12			S1E-4, -12	Alarm monitor circuit (1A13A2Q1 - Q8)	S1A-12

e. To test 1.6 kHz oscillator 1A13A5Q1, the MODULE TEST selector switch is set to position 10 which connects ground to the oscillator input through 91E-2 and S1E-10. With its input grounded the oscillator starts to oscillate and provides 1.6 kHz tone output through IC amplifier 1A13A5A1. The tone signal is connected to the 1.1/1.6 kHz input of 4.02 kHz monitor IA13AIQ2 through emitter follower Q5 and IC amplifier A2 on 1A13A2, and contact S1A-10 of the selector switch. If the 1.6 kHz oscillator and emitter follower Q5 are operating normally (IC amplifier 1A13A2A2 was tested for normal operation in position 9 of the selector switch), the MODULE TEST indicator should be extinguished. If the 1.6 kHz oscillator and/or emitter follower Q5 are not operating normally, the MODULE TEST indicator will light red.

f. The 1.1 kHz oscillator IA13A2Q7 is tested in a manner similar to that described above for the 1.6 kHz oscillator except that the MODULE TEST selector switch

is set to position 11. Ground is applied to the oscillator input through S1E-6 and S1E-11 causing the oscillator to provide a 1.1 kHz tone output through IC amplifier 1A13A2A1. The 1.1 kHz tone signal is connected to the 1.1/1.6 kHz input of the 4.02 kHz monitor by the TEST TONE switch, emitter follower Q6 and IC amplifier A2 on board No. 2 IA13A2, and selector switch contact S1A-11.

g. To test the central alarm monitor circuit on meter panel assembly 1A15A8 and the monitor circuit on IA13A.2, the MODULE TEST selector switch S1 is set to position 12. Sections S1E and S1E-12 apply ground to simulate power amplifier alarm input OR gates A and B on

1A13A2. OR gate A triggers multivibrator circuit Q1, Q2 and Q3 into operation. The multivibrator alternately connects ground to the 1.1 kHz oscillator inputs. The 1.6 kHz oscillator is located on 1A13A6. The alternating output of each oscillator is coupled through the TEST TONE and RING switches and applied to emitter followers Q4 and Q5 and speaker amplifier A2 on 1A13A2. The output of A2 is applied to the monitor circuit amplifier A2 through switch section SIA-r12. Monitor circuit amplifier A2 will provide an output to extinguish the MODULE TEST indicator. Alarm OR gate B turns off transistor switch Q6 on 1A13A2, thereby removing the operating voltage from CNTRL IALARM indicator on meter panel assembly 1A15A8. Removing the voltage changes the lamp indication from green to red for alarm condition. Emitter follower Q4 applies the 1.1/1.6 kHz tone to meter panel assembly 1A15A8 for an audible alarm.

2-10. Transmitter, Radio T-1054(P)/ GRC-144(V)  
Modulator Circuits Functional Block Diagram  
Description (fig. 5-11)

The modulator circuits consist of input circuits, radio transmitter modulator 1A8, and electronic frequency control 1A7. The input circuits combine the pcm and orderwire signals at the appropriate signal levels. The composite signal is applied to radio transmitter modulator 1A8 and modulates a 160 MHz oscillator in 1A8. The frequency modulated 150 MHz output is applied to transmitter frequency mixer stage 1A9. A sample of the frequency modulated output is fed back from radio transmitter modulator 1A8 to electronic frequency control 1A7 which produces an automatic frequency control (afc) signal to stabilize the center frequency of the 150 MHz oscillator in 1A8.

a. Input Circuits. The input circuits consist of attenuator assembly 1A3, af-rf amplifier 1A4, and 4.5 MHz low-pass filter 1A6.

(1) The pcm input from digital data modem 1A12 is applied to pcm attenuator and phase shift network (R1-R5, C1, C2) in attenuator assembly 1A3. The attenuator and phase shift network provides a pcm signal phase shift of 21 degrees at 300 Hz and attenuates the signal to the proper level for application to af-rf amplifier 1A4. To maintain separation between pcm and orderwire signals, a 21-degree phase shift of the transmitter signals is required (the receiver signals phase shift is 16 degrees and the overall TM 11-5820-

695-35 signal phase shift requirement of Radio Set AN/GRC-144 is 37 degrees at 300 Hz). Af-rf amplifier 1A4 provides a maximum gain of 25 db. The amplifier comprised of stages Q1, Q2, Q3 is basically a shunt feedback amplifier. The TRAFFIC LEVEL ADJ control at the input to the amplifier allows the gain to be adjusted from its maximum value to zero.

(2) The orderwire input from orderwire assembly 1A13 is applied to the 48 channel attenuator and metering circuit through the input attenuator circuit and the 48/96 channel selector switch. The OW LEVEL ADJUST control in the input attenuator circuit and the 4.8 channel attenuator circuit are used to maintain the orderwire signal level within 15 to 20 percent of the pcm signal level. The orderwire signal level is detected in the 48 channel metering circuit for application to the meter selector switch. The 48/96 channel selector switch is placed in the 48 CH position for all modes of operation. (The 96 CH selector switch position and associated attenuator and metering circuits are provided for future applications of Radio Set AN/GRC-144.) The pcm output signal from af-rf amplifier 1A4 and the orderwire signal are connected together at the output of af-rf amplifier 1A4 and form a combined signal (pcm and orderwire) input to 4.5 MHz low-pass filter 1A6. The 4.5 MHz lowpass filter passes the combined signal to radio transmitter modulator 1A8 and, together with other filters in the radio set, provides the required shaping.

b. Radio Transmitter Modulator 1A8. Radio transmitter modulator 1A8 receives the combined pcm and orderwire signal and produces a frequency modulated 150 MHz output which is applied to transmitter frequency mixer stage 1A9. A sample of the frequency modulated output is fed back from 1A8 to electronic frequency control 1A7 which produces an afc signal to stabilize the center frequency of the 150 MHz oscillator in 1A8.

(1) The traffic input signal (combined pcm and orderwire signal) is applied to operational amplifier A1 (integrated circuit). Front panel variable resistor R2 is used to adjust the input level to the amplifier A1 (transmitter fm deviation). The amplifier traffic signal is then applied to 150 MHz vco Q1. The 150 MHz vco uses varactor diodes to control the output frequency. A positive going traffic signal deviates the vco toward a lower frequency and a negative going traffic signal deviates the vco toward a higher

frequency. The vco's center frequency can be adjusted with front panel variable capacitor C15. The 1.50 MHz frequency modulated output of the vco is applied to amplifier stages Q3, Q4, Q8, and Q9 through emitter follower Q2 which isolates the vco from the amplifier stages. The amplified frequency modulated 1150 MHz signal is applied through matching pad R%3-R65 to frequency mixer 11A9.

(2) The 150-MHz output signal is also applied to mixer circuit T3, CR7, CR8 where it is mixed with a 220 MHz signal. The 220 MHz signal is developed by the 110 MHz crystal oscillator circuit Q5 and frequency doubler circuit T2, CR5, CR6. The output of the mixer is applied to low-pass filter L10, C38, and C39. The 70 MHz difference signal produced by the mixing process is passed by the filter and amplified by stages Q6 and Q7 for application to electronic frequency control 1A7.

*c. Electronic Frequency Control 1A7.* Electronic frequency control 1A7 receives the sampled frequency modulated 70 MHz signal from radio transmitter modulator 1A8 and produces an afc signal to stabilize the center frequency of the 1150 MHz vco in 1A8. The 70 MHz sampled signal is applied to gate-A, CR4CR6, through emitter follower Q3 in electronic frequency control 1A7. A 70 MHz reference signal from reference oscillator circuit Q1 is applied to gate-B, CR1-CR3, through emitter follower Q2. The frequency of the reference oscillator can be adjusted using variable inductor L2. With switch S1 in the OPR position, free-running multivibrator Q4 and Q5 alternately switches between gate A and gate B. Thus, the 70 MHz sample signal from 1A8 and the 70 MHz signal from the reference oscillator are alternately applied to emitter follower Q7. The emitter follower provides isolation between the gate inputs and limiter stages Q8 and Q9. The limiter stages prevent any amplitude variations from reaching the discriminator. The limiter stages are tuned by adjusting the 1ST LIM LEVEL and the 2ND LIM LEVEL controls. Emitter follower Q10 isolates the second limiter stage from discriminator driver Q11. The discriminator, T1, C51-C56, CR10 and CR11 is a conventional type, employing the phase shift principle. Both the primary and secondary of T1 are tuned for a linear S-curve centered about 70 MHz. The output of the discriminator is a square wave with an amplitude proportional to the frequency difference of the signals (70 MHz modulated signal from the modulator and 70 MHz reference signal). The difference (error) signal is applied to phase detector circuit T2, CR12-CR15 by

square wave amplifier Q12Q15. The square wave amplifier is a highly stable feedback amplifier which is ac coupled both at the output and the input. The phase detector circuit receives the error signal and an input from the multivibrator to determine the polarity for plus or minus correction. When the sampled input from the modulator is lower than 70 MHz, the phase detector provides a negative correction voltage output to drive the vco frequency higher. When the sampled input from the modulator is higher than 70 MHz, the phase detector provides a positive correction voltage output to drive the vco frequency lower. The center frequency of the phase detector can be adjusted with phase detector balance variable resistor R78. Emitter follower Q6 isolates the multivibrator from the phase detector. The correction signal (afc) is applied to differential amplifier A2-A and A2-B in modulator 1A8. The differential amplifier increases the sensitivity of the afc output circuit. The afc signal applied to the 150 MHz vco provides  $\pm$ 20 kHz center frequency stability. The EFC DISABLE switch on modulator 1A8 is used to disable the afc input signal. When depressed, the EFC DISABLE switch shorts out the afc input to modulator 1A8. When aligning the vco, the EFC DISABLE switch is depressed and front panel variable capacitor C15 is adjusted.

*d. Meter Circuits*

(1) The orderwire metering circuit in attenuator assembly 1A3 provides an output to the meter selector switch on meter panel assembly 1A15A8. The orderwire signal level may be monitored by setting the meter selector switch to the OW TEST position.

(2) Various signals from radio transmitter modulator 1A8 and electronic frequency control 1A7 are applied to the meter selector switch on meter panel assembly 1A15A8. The traffic input to 1A8 is applied through emitter follower A2) (part of integrated circuit A2) to the 48 channel traffic attenuator in attenuator 1A3 and then to the meter selector switch by alarm monitor 1A5. Note that the 48/96 channel attenuator switch on 1A3 must be set to the 48 CH position (para 2-10a(2)). Variable resistor 1A15A8R7 mounted on the back of meter panel assembly 1A15A8 is used to calibrate the T,RAFFIC meter indication. The 150-MHz output and 70 MHz sample output signals from 1A8 are applied through meter circuits CR10 and CR9, respectively, to the meter selector switch. The center frequency (afc signal) is applied from output electronic frequency control 1A7 to the meter selec

tor switch. Also, the afc level at the output of the limiter stages in electronic frequency control 1A7 is applied to the meter selector switch through meter circuit 1A7CR9. Any one of the above signals may be monitored by setting the meter selector switch to the desired position.

#### 2-10.1 Transmitter, Radio T-1054 (P) A/GRC-144(V) Modulator 1A8 Functional Block Diagram Description (fig. 5-11.1)

The modulator circuits in Transmitter, Radio T-1054(P)A/IRC-144(V) are basic all the same as those in Transmitter, Radio T-1054(P)/GRC-144(V) (para 2-10). The same functions are performed and the circuits are the same except as noted below.

a. Input Circuits. In digital orderwire mode, the combined data/digital orderwire signal is applied to attenuator assembly 1A3, and the PH NTWK switch is in NORMAL position. The signal is coupled through the attenuator to AF-RF amplifier 1A4. Since there is no analog orderwire signal, the input from orderwire assembly 1A13 is grounded by OW SEL switch in the DVOW position. In analog orderwire mode, the PH NTWK switch is in the IN position and the data (only) signal is coupled through the phase shift network to AF-RF amplifier 1A4. The OW SEL switch is in AVW position and the analog orderwire signal from orderwire assembly 1A13 is coupled through an attenuator according to the position of DATA RATE switch. For higher data rates, a different attenuator assembly is used for 1A3 and LPF 1A6 is replaced by a cable, as shown in figure 5-11.1.

b. Radio Transmitter Modulator 1A8. Radio transmitter modulator 1A8 receives the combined data and orderwire signal and produces a frequency modulated 150 MHz output which is applied to transmitter frequency mixer stage 1A9. A sample of the frequency modulated output is fed back from 1A8 to electronic frequency control 1A7 which produces an afc signal to stabilize the TM 11-5820-695-35 center

frequency of the 150 MHz oscillator in 1A8. The traffic input signal (combined data and orderwire signal) is applied to baseband amplifier Q101-Q103 through BANDSET switches S102 and S101. These switches are set according to the operating frequency, as explained in paragraph 2-35.1. Front panel variable resistor R149 is used to adjust the input level to the baseband amplifier (transmitter fm deviation). The amplified traffic signal is then applied to 150 MHz vco Q1. The 150 MHz vco uses varactor diodes to control the output frequency. A positive going traffic signal deviates the vco toward a lower frequency and a negative going traffic signal deviates the vco toward a higher frequency. The vco's center frequency can be adjusted with front panel variable capacitor C114. The 150 MHz frequency modulated output of the vco is applied to limiter amplifier stages Q104 to Q106 and Q108 through buffer amplifier Q109 which isolates the vco from the amplifier stages. The amplified frequency modulated 150 MHz signal is applied through matching pad R154-R156 to frequency mixer 1A9.

c. Electronic Frequency Control 1A7. Refer to paragraph 2-10c.

d. Meter Circuits.

(1) The orderwire metering circuit in attenuator assembly 1A3 provides an output to the meter selector switch on meter panel assembly 1A15A8. The orderwire signal level may be monitored by setting the meter selector switch to the OW TEST position.

(2) Various signals from radio transmitter modulator 1A8 and electronic frequency control 1A7 are applied to the meter selector switch on meter panel assembly 1A15A8. The traffic input to 1A8 is applied through emitter follower Q110 to attenuator assembly 1A3 and then through alarm monitor 1A5 to meter panel assembly 1A15A8.

## 2-11. Transmitter, Radio T-1054(P) /GRC-144(V) Local Oscillator and Mixer Circuits Functional Block Diagram Description (fig. 2-3)

The local oscillator circuits consist of electrical frequency synthesizer 1A14, transmitter amplifier-frequency multiplier 1A11, coaxial circulator 1HY1, and transmitter frequency multiplier group 1A10. The local oscillator circuits produce a 4.55 to 4.85 GHz output which is applied to transmitter frequency mixer stage 1A9 along with the frequency modulated 150 MHz output from radio transmitter modulator 1A8. The mixer circuits consist of crystal mixer 1A9A1 and coaxial circulator 1A9HY1 in frequency mixer 1A9. The mixer circuits heterodyne the local oscillator frequency with the 150-MHz signal to produce a 4.4 to 5.0 GHz output which is applied to the antenna system through rf bandpass filter 1FL3, rf low-pass filter 1FL4, and directional coupler 1DC1.

*a. Local Oscillator Circuits.* The local oscillator circuits produce an output frequency of 4.55 to 4.85 GHz by multiplying the electrical frequency synthesizer's output frequency by 16. Electrical frequency synthesizer 1A14 generates a highly stable radio frequency in the range of 284.375 to 303.125 MHz, adjustable in 6.250 kHz steps. Electrical frequency synthesizer 1A14 circuits are described in detail in paragraph 212. The 284.375 to 303.125 MHz, 20 milliwatt output of electrical frequency synthesizer 1A14 is applied to transmitter amplifier-frequency multiplier 1A11.

(1) Transmitter amplifier-frequency multiplier 1A11 is comprised of frequency doubler stage 1 CR1 and CR2, 600 MHz amplifier stages Q1 Q4, and frequency doubler stage 2 CR3. The 284.375 to 303.125 MHz input is doubled to 568.750 to 606.250 MHz by frequency doubler stage 1 and applied to the 600 MHz amplifier stages. The 600 MHz amplifier stages amplify the 568.750 to 606.250 MHz signal to a level (approximately 18 watts) to drive frequency doubler stage 2. Frequency doubler stage 2 doubles the signal, 1137.5 to 1212.5 MHz. The 1137.5 to 1212.5 MHz signal (approximately 8 watts power output) is applied to transmitter frequency multiplier 1A10 through coaxial circulator 1HY1. The circulator isolates frequency doubler stage 2 in 1A11 from the transmitter 2na stage

frequency multiplier in 1A10. Coaxial circulator 1HY1 also provides a detected sample of the 1137.5 to 1212.5 MHz signal (1st multiplier) to the meter selector switch on meter panel assembly 1A15A8. Variable resistor 1A15A8R4 on the back of meter panel assembly 1A15A8 is used to calibrate the 1st multiplier (AMPLMULT) meter indication.

(2) Transmitter frequency multiplier group 1A10 is comprised of transmitter 2nd stage frequency multiplier 1A10A1, coaxial circulator 1A10HY1, and transmitter 3rd stage frequency multiplier 1A10A2. The transmitter 2nd stage frequency multiplier 1A10A1 employs a tuned circuit, a varactor diode doubler and a tuned cavity to multiply the frequency up to 2275-2425 MHz at 4 watts (nominal). Coaxial circulator 1A10HY1 isolates transmitter 2nd stage frequency multiplier 1A10A1 from transmitter 3rd stage frequency multiplier 1A10A2 and also provides a detected sample of the 2276 to 2426 MHz signal (2nd multiplier) to the meter selector switch on meter panel assembly 1A15AS. Variable resistor 1A15A8RS on the back of meter panel assembly 1A15A8 is used to calibrate the 2ND MULT meter indication. Transmitter 3rd stage frequency multiplier 1A10A2 employs a low pass filter, varactor diode doubler, and a tuned cavity to multiply the frequency up to 4.55-4.85 GHz at 1.7 watts (nominal). The 4.55-4.85 GHz signal is applied to transmitter frequency mixer stage 1A9 where it is mixed with the frequency modulated 1150 MHz signal from radio transmitter modulator 1A8.

*b. Transmitter Frequency Mixer Stage 1A9.* Transmitter frequency mixer stage 1A9 translates the frequency modulated 150 MHz signal up to the 4.4 to 5.0 GHz band. This is accomplished by heterodyning the local oscillator frequency of 4.55 to 4.85 GHz with the 150 MHz signal in a tuned varactor cavity. Frequency conversion is accomplished by the nonlinear capacitance-voltage relationship of the varactor diode in the tuned cavity.

(1) The frequency mixer circuits consist of crystal mixer 1A9A1 and coaxial circulator 1A9HY1. The 4.665 to 4.85 GHz local oscillator signal enters port number 1 of the circulator and leaves at port number 2, entering tuned varactor cavity Z1 in crystal mixer 1A9A1. The 150 MHz signal is applied at the opposite end of the tuned varactor cavity by the 150 MHz tuned circuit.



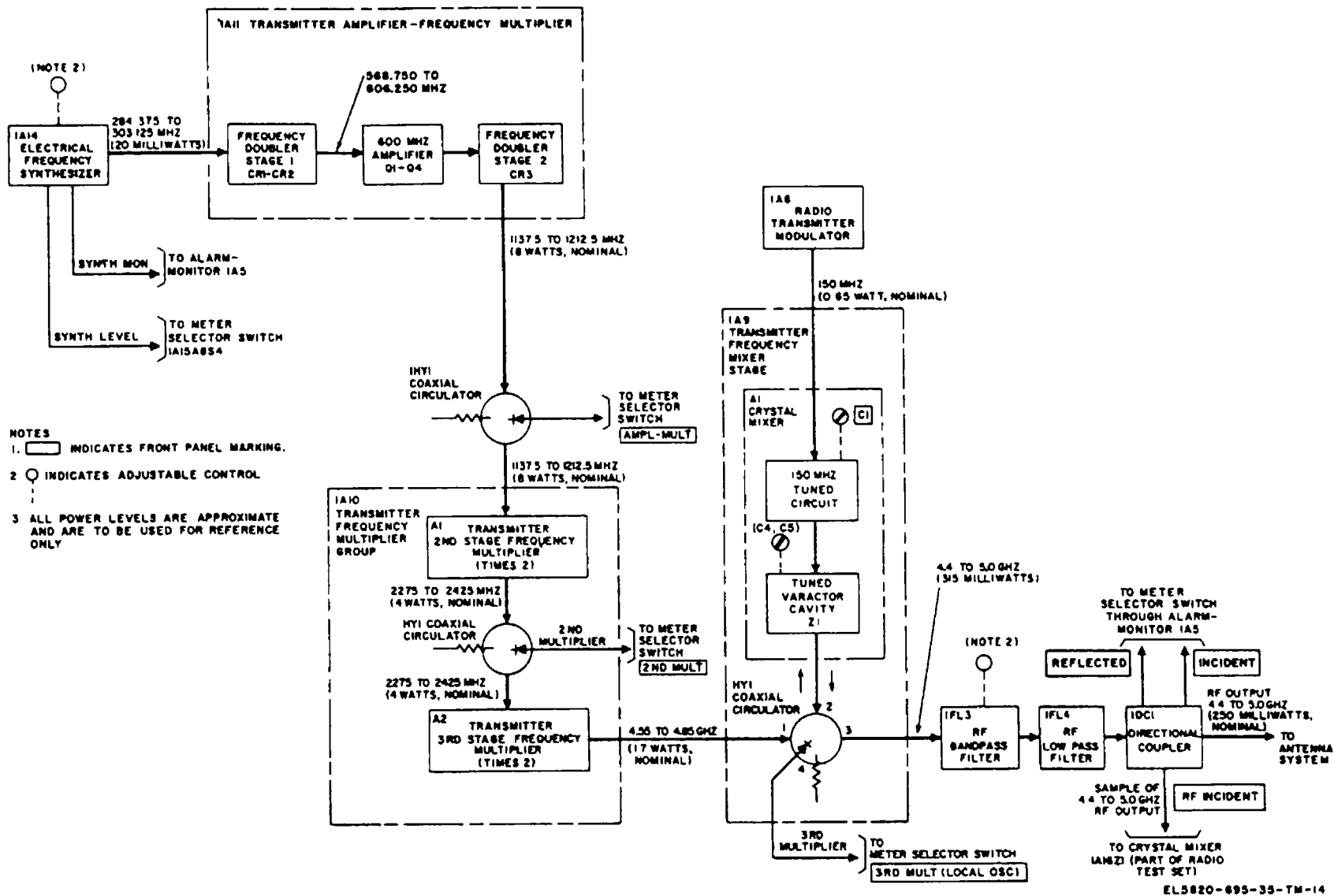


Figure 2-3. Transmitter, Radio T-1054(P)/GRC-144(V) Local Oscillator and Mixer Circuits, Functional Block Diagram

Change 6 2-30.1/(2-30.2 blank)

This circuit tunes out the varactor capacity at the 150 MHz frequency. Variable capacitor C1 is accessible from the front panel and is used when aligning the tuned circuit. The tuned circuit also prevents rf from leaking back to radio transmitter modulator 1A8. The 4.55 to 4.85 GHz local oscillator fundamental frequency is suppressed in the tuned varactor cavity by two tuned stubs C4 and CS5, producing sidebands containing frequency modulated 150 MHz signal. The sidebands are reflected out of the tuned varactor cavity, enter the circulator at port number 2, and leave at port number 3. The 4.4 to 5.0 GHz (approximately 315 milliwatts) output from port number 3 is applied to radio frequency bandpass filter 1FL3 which is tuned to the desired sideband and passes the selected sideband to radio frequency low pass filter 1FL4. The unwanted sideband is reflected by 1FL3 to port number 3 and applied to port number 4 of the circulator where it is absorbed in a dummy load. The circulator also provides a detected sample of the 4.65 to 4.85 signal (3rd multiplier) to the meter selector switch on meter panel assembly 1A16A8. Variable resistor 1A15ASR2 on the back of meter panel assembly 1A115A8 is used to calibrate the 3RD MULT meter indication.

(2) Radio frequency bandpass filter 1FL5 has a maximum 3 db bandpass of 38 MHz and is tuned to the desired frequency in the 4.4-.0 GHz band by setting the filter's tuning knob to the appropriate frequency. The bandpass filter passes the desired frequency through radio frequency low pass filter 1FL4 and directional coupler 1DC1 to the antenna system. The rf power output from directional coupler IDC1 to the antenna system is 2,50 milliwatts (nominal). The directional coupler provides three additional outputs (monitor ports). Two of the outputs are dc levels which indicate the transmitter's forward rf power and reflected power. These outputs are applied through alarm monitor 1A5 to the meter selector switch on meter panel assembly 1A15A8. Potentiometers 1A15A8R5 and 1A15A8R6 on the back of 1A15A8 are used to calibrate the REFL RF POWER and RF POWER meter indications, respectively. The third output from the directional coupler provides a sample of the 4.45.0 GHz output signal which is 21 db down from the mainline rf power output signal. This sampled signal is applied to crystal mixer 1A16Z1 of the radio test set.

## 2-12. Electrical Frequency Synthesizer 1A14/2A14 Functional Operation

### a. General.

(1) Two identical electrical frequency synthesizers are used in Radio Set AN/GRC-144. One is in Transmitter, Radio T-1054/GRC-144 and is designated 1A14. The other is in Receiver, Radio R-1467/GRC-144 and is designated 2A14. The transmitter and receiver local oscillator operating frequencies are derived from the associated electrical frequency synthesizer. The electrical frequency synthesizer generates one output signal selectable within the frequency range of 284.375 MHz to 303.125 MHz which is subsequently converted (external to the electrical frequency synthesizer) to an operating frequency within the range of 4400.0 MHz through and including 5000.0 MHz.

(2) The electrical frequency synthesizer output frequency is selected by setting thumbwheel switches. This frequency is increased by frequency multipliers and mixers in the T-1054/ GRC-144 (or R-1467/GRC-144) to the required final operating frequency. Thumbwheel switch settings on the electrical frequency synthesizer are direct reading and are calibrated to indicate (in MHz) the operating frequency of the T1054/GRC-144 (or R-1467/GRC-144), not the electrical frequency synthesizer output frequency.

(3) The electrical frequency synthesizer is an application of the phase-locked loop principle. The electrical frequency synthesizer uses a voltage controlled oscillator (vco) to generate the output signal. The accuracy of the frequency of the vco is maintained by a crystal oscillator standard (operating at 8 MHz). The output signal of the vco is returned, through a feedback network which lowers the frequency, and it is compared in phase with the crystal oscillator standard frequency. A difference in frequency between the vco signal and the crystal oscillator standard frequency is detected as a phase error. A phase error detector generates a signal which in turn adjusts the frequency of the vco as required. This feedback loop is designated a phase locked loop since it locks the vco frequency in step with the crystal oscillator control frequency.

(4) The subparagraphs that follow describe the correlation between the thumbwheel switch settings and the electrical frequency synthesizer's rf output frequencies, the correlation between the transmit operating frequency and the electrical frequency synthesizer rf output frequency, the correlation between the receive operating frequency and the electrical frequency

synthesizer rf output frequency, and the overall block diagram description of the electrical frequency synthesizer.

*b. Correlation Between Thumbwheel Switch Settings and Electrical Frequency Synthesizer RF Output Frequencies.* The thumbwheel switches on the front panel of electrical frequency synthesizer select and indicate a specific operating frequency in the 4400.0 MHz to 5000.0 MHz range. Any frequency in this range can be selected. The electrical frequency synthesizer rf output frequencies from 284.375 MHz to 303.11875 MHz correspond to Radio Set AN/ GRC-144 operating frequencies from 4400.0 MHz to 4699.9 MHz. This rf output frequency range (284.375 MHz to 303.11876 MHz) is repeated for operating frequencies from 4700.0 MHz to 4999.9 MHz. An electrical frequency synthesizer rf output frequency of 303.125 MHz corresponds to a thumbwheel switch setting of 5000.0 MHz. Thus, the thumbwheel switches provide for the selection of 6001 different operating frequencies in 0.1 MHz steps. The 5000.0 MHz frequency down to and including the 4400.0 MHz frequency is a range of 600.1 MHz. The four thumbwheel switches provide a direct reading of five digits in MHz. The first thumbwheel switch (on the left) sets the first two digits of the Radio Set AN/GRC-144 operating frequency. The last three digits of the operating frequency are set respectively by the remaining three thumbwheel switches. The chart below lists the electrical frequency synthesizer rf output frequency (frequency A) resulting from the thumbwheel switch settings for the first three digits of the Radio Set AN/GRC-144 operating frequency. It also lists the additive frequency increments resulting from setting the thumbwheel switches for the remaining two digits (fourth and fifth) of the operating frequency. The fourth digit additive frequency is listed as frequency B. The fifth digit additive frequency is listed as frequency C. Therefore, when the last two (of five) digits are set at a number other than zero, the frequency electrical synthesizer rf output frequency (F.) is the sum of frequency A and the two additive frequencies B and C (F.= Frequency A + Frequency B + Frequency C). For example, assume that the thumbwheel switches are set to an operating frequency of 4765.9 MHz. From the chart below, the corresponding electrical frequency synthesizer rf output frequency (F.) is calculated as follows:

Frequency A (first three digits showing 476) = 288.125000 MHz  
 Frequency B (fourth digit showing 6) = 0.312500 MHz  
 Frequency C (fifth digit showing .9) = 0.056250 MHz  
 F. = 288.493750 MHz

(1) Thumbwheel switch setting (first three digits).

First and second digit	Third digit	Frequency A (MHz)
44 or 47	0	284.375000
	1	285.000000
	2	285.625000
	3	286.250000
	4	286.875000
	5	287.500000
	6	288.125000
	7	288.750000
	8	289.375000
9	290.000000	
First and second digit	Third digit	Frequency A (MHz)
45 or 48	0	290.625000
	1	291.250000
	2	291.875000
	3	292.500000
	4	293.125000
	5	293.750000
	6	294.375000
	7	295.000000
	8	295.625000
9	296.250000	
First and second digit	Third digit	Frequency A (MHz)
46 or 49	0	296.875000
	1	297.500000
	2	298.125000
	3	298.750000
	4	299.375000
	5	300.000000
	6	300.625000
	7	301.250000
	8	301.875000
9	302.500000	
50	0	303.125000

(2) Thumbwheel switch setting (fourth digit).

Fourth digit	Frequency B (MHz)
0	0.000000
1	0.062500
2	0.125000
3	0.187500
4	0.250000
5	0.312500
6	0.375000
7	0.437500
8	0.500000
9	0.562500

**(3) Thumbwheel switch setting (fifth digit).**

Fifth digit	Frequency C (MHz)
0	0.000000
1	0.006250
2	0.012500
3	0.018750
4	0.025000
5	0.031250
6	0.037500
7	0.043750
8	0.050000
9	0.056250

c. *Correlation Between Transmit Operating Frequency and Electrical Frequency Synthesizer 1A14 RF Output Frequency.* The correlation between the transmit operating frequency and the electrical synthesizer 1A14 rf output frequency is described below.

(1) When the thumbwheel switches on 1A14 are set to 4400.0 MHz (transmit operating frequency), the rf output frequency of 1A14 is 284.375 MHz. The 284.375 MHz signal is multiplied by 16 to a 4550 MHz local oscillator signal by the times 16 frequency multiplier chain in Transmitter, Radio T-1054/GRC-144. The 4650 MHz local oscillator signal is then mixed with a 150 MHz frequency modulated signal containing the intelligence to be transmitted. Frequency selective circuits in the T-1054/GRC-144 select the lower sideband (4550 MHz minus 150 MHz) produced by the mixing process to obtain the selected 4400 MHz (4.4 GHz) transmit operating frequency.

(2) When the thumbwheel switches on 1A14 are set to 4700.0 MHz (transmit operating frequency), the rf output of 1A14 is 284.375 MHz. The 284.375 MHz signal is multiplied by 16 to a 4550 MHz local oscillator signal and mixed with 150 MHz as described above. However, to obtain the 4700 MHz (4.7 GHz) transmit operating frequency, frequency selective circuits in the T-1054/GRC-144 select the upper sideband (4550 MHz plus 160 MHz).

d. *Correlation Between Receive Operating Frequency and Electrical Frequency Synthesizer 2A14 RF Output Frequency.* The thumbwheel switches on electrical frequency synthesizer 2A14 are set to the desired receive operating frequency within the range of 4400.0 MHz to 5000.0 MHz. The corresponding electrical frequency synthesizer rf output frequencies are the same as described in b above. The incoming receive operating frequency is used as a mixing signal

to obtain a 70 MHz if signal containing received intelligence. The correlation between the receive operating frequency and electrical frequency synthesizer 2A14 rf output frequency is described below.

(1) When the thumbwheel switches on 2A14 are set to 4400.0 MHz (receive operating frequency), the rf output frequency of 2A14 is 284.375 MHz. The 284.375 MHz signal is multiplied by 16 to 4550 MHz by the times 16 multiplier chain in Receiver, Radio R-1467/GRC144. The 4560 MHz signal is then mixed with a 220 MHz signal. Frequency selective circuits in the R-1467/GRC-144 select the lower sideband (4550 MHz minus 220 MHz) produced by the mixing process to obtain a 4330 MHz local oscillator signal. The 4330 MHz signal is then mixed with the 4400 MHz incoming signal (receive operating frequency). Frequency selective circuits in the R-1467/GRC-144 select the lower sideband (440 MHz minus 4330 producing the required 70 MHz if. Signal which contains the received intelligence.

(2) When the thumbwheel switches on 2A21 are set to 4700.0 MHz (receive operating frequency), the rf output of electrical frequency synthesizer 2A14 is 284.375 MHz. The 284.375 MHz signal is multiplied by 16 to 4550 MHz by the times 16 multiplier chain in the R-1467/ GRC-144 and mixed with 220 MHz as described above. However, in order to obtain the correct receiver local oscillator frequency (4770 MHz), frequency selective circuits select the upper sideband (4650 MHz plus 220 MHz). The 4770 MHz local oscillator frequency is then mixed with the 4700 MHz incoming signal (receive operating frequency). Frequency selective circuits in the R-1467/GRC-144 then select the lower sideband (4770 MHz minus 4700 MHz) producing the required 70 MHz if signal which contains the received intelligence.

e. *Overall Block Diagram Description of Electrical Frequency Synthesizer 1A14/2A14 (fig. 512).* The main signal flow (heavy lines on diagram) between plug-in components (A1 through A7) is shown. The dc power distribution from power supply AS to components A1 through A7 is also shown. Each component is represented by a block on the diagram. Main chassis circuits (e.g., thumbwheel switches) are also shown as blocks on the diagram. The following subparagraphs describe the main signal flow through electrical frequency synthesizer 1A14. The description also applies to electrical frequency synthesizer 2A14, except the reference designations are prefixed with 1A14 instead of 2A14 and the word transmitter is used instead of receiver.

(1) Radio frequency oscillator 1A14A1 utilizes a voltage controlled oscillator (vco) to produce an rf output signal in the 284.3750 MHz to 303.1250 MHz frequency range. The specific frequency of the rf output signal is determined by the vco bias signal. Two rf output signal levels (high and low), at the same frequency, are provided by radio frequency oscillator 1A14A1. The 20 milliwatt (nominal) rf output (high) signal is applied through electrical frequency synthesizer 1A14 main chassis (synth output) to the transmitter frequency multiplier circuits. A detected rf output signal level (meter), derived from the rf output (high) signal is applied through the main chassis (synth level) to the meter panel assembly 1A15A8 meter selector switch. The 1 milliwatt (nominal) rf output (low) signal is applied to electronic frequency converter 1A14A2 (part of phase-lock loop circuits). The vco bias voltage input to 1A14A1 is derived from a comparison of the rf output (low) signal from 1A14A1 with a reference signal. A lamp test signal from the main chassis TEST switch is applied to test the failure lamp in 1A14A1. The failure lamp lights when the rf output signal is not present.

(2) Electronic frequency converter 1A14A2 converts the rf output (low) signal from 1A14A1 to an intermediate frequency (if) output signal that is compatible with the digital integrated circuits in variable 1 and 2 frequency dividers, 1A14A4 and 1A14A5. This is accomplished by first dividing the rf output (low) signal (284.375 MHz to 303.125 MHz) by two and then mixing the resulting frequency (142.1875 MHz to 151.5625 MHz) with a 128 MHz reference frequency. The 128 MHz reference signal is produced in 1A14A2 by multiplying the 8 MHz signal from standard radio frequency oscillator 1A14A7 by 16. The intermediate frequency (14.1875 MHz to 23.5625 MHz) is produced by mixer circuits within 1A14A2 and is applied to variable 1 frequency divider 1A14A4.

(3) Variable 1 frequency divider 1A14A4 operates in conjunction with variable 2 frequency divider 1A14A5 to divide the if output signal from 1A14A2. Variable 1 frequency divider 1A14A4 has the capability of dividing the if output signal by 200. The divided if output signal (count) from 1A14A4 is applied to variable 2 frequency divider 1A14A5. Variable 2 frequency divider 1A14A5 has the capability of dividing the input signal by 80. Thus, the variable frequency dividers have the capability of dividing the if output signal from 1A14A2 by 16,000 (200 x 80). However, the maximum division capability is not utilized. The division ratio is established by the thumbwheel switches on the electrical

frequency synthesizer 1A14 front panel. The thumbwheel switches can be set between 4400.0 MHz and 5000.0 MHz to provide a divisor from 9080 to 15080. When the thumbwheel switches are set between 4400.0 MHz and 4699.9 MHz, the intermediate output signal from electronic frequency converter 1A14A2 is divided by between 9080 and 15078, respectively. Each 0.1 MHz step in the switch changes the divisor by two; e.g., switch setting 4400 establishes division by 9080 and switch setting 4400.1 establishes division, by 9082. When switches are set between 4700.0 MHz and 4999.9 MHz, the division is again between 9080 and 16078, respectively. When the switches are set to 5000 MHz, the divisor is set at 15080. Variable 1 frequency divider 1A14A4 divides the if output frequency from 1A14A2 in accordance with the 1 MHz and 0.1 MHz thumbwheel switch settings. Variable 2 frequency divider 1A14A5 divides the count output from variable 1 frequency divider 1A14A4 in accordance with the 1000 MHz, 100 MHz, and 10 MHz switch settings. The variable frequency dividers divide the if output signal from 1A14A2 to produce the divide-by-N (N) signal. When phase-lock is established (rf output from 1A14A1 is exactly at the frequency indicated by the thumbwheel settings), the frequency of the divide-by-N pulses is exactly 1.5625 kHz. If the thumbwheel switch settings are changed to a new frequency, the countdown on the variable frequency divider circuits changes causing the frequency of the divide by-N pulses to change. For this condition (phase loop unlocked), the frequency of the divide-by-N pulses is not exactly 1.5625 kHz. The divide-by-N output pulses from variable 2 frequency divider 1A14A5 are applied to fixed frequency divider 1A14A6 and audio frequency phase error detector 1A14A3.

(4) Fixed frequency divider 1A14A6 produces a 1.5625 kHz reference signal from the 8 MHz input signal from standard radio frequency oscillator 1A14A7 and compares the 1.5625 kHz reference signal with the divide-by-N pulses received from 1A14A5. A two-bit correction signal and a phase lock signal are generated within 1A14A6 as a result of this comparison. The two-bit correction signal is used in determining the vco bias voltage which is produced by audio frequency phase error detector 1A14A3. The phase lock signal is applied (synth alarm) to alarm monitor 1A5 circuits and is used to control an alarm indicator on meter panel assembly 1A15A8. If the 1.5625 kHz reference signal and the divide-by-N pulses are in phase, the two-bit

correction signal remains fixed and the phase lock signal indicates a phase lock condition (normal indication on meter panel assembly 1A15A8). If the 1.5625 kHz reference signal and the divide-by-N pulses are not in phase, the two bit correct signal ( $2^0$  and  $2^1$ ) cycles through four states (00, 01, 10, and 11), causing the vco bias voltage produced in 1A14A3 to cycle through four voltage levels. Also, for this condition, the phase-lock signal indicates an out-of phase condition causing an alarm indication on meter panel assembly 1A15A8.

(5) Audio frequency phase error detector 1A14A3 receives the 1.5625 kHz reference and two-bit correction signals from 1A14A6 and the divide-by-N pulses from 1A14A5. The 1.5625 kHz reference signal is used to start a sawtooth waveform generated within 1A14A3. The sawtooth waveform is superimposed on dc level(s) determined by the two-bit correction signal. For a phase lock condition, the dc level remains fixed. For an out-of-phase condition, the two-bit correction signal cycles through its four states causing the vco bias voltage to cycle through four voltage step levels. The sawtooth waveform, superimposed on each step level, is of sufficient amplitude to overlap adjacent step levels. Thus, the step levels provide coarse tuning of the vco bias voltage and the sawtooth waveform provides fine tuning of the vco bias voltage within each step voltage change. The divide-by-N pulses are used to gate and store the sawtooth waveform level. The stored voltage is the vco bias voltage which is applied to the vco in 1A14A1, thereby controlling the rf output frequency. When the divide-by-N pulses and the 1.5625 kHz reference frequencies are equal (phase-lock condition), the gate opens at the same point on the sawtooth ramp for each vco bias voltage sample; thus, the vco bias voltage will remain constant causing the rf output frequency to remain constant. If the divide-by-N pulses and the 1.5625 kHz reference signal are not exactly the same frequency (a changing phase), the sampling point on the sawtooth waveform varies and the vco bias voltage changes. If the phase (time) between the pulses is decreasing (corresponding to an increase in the vco rf output frequency), the sawtooth is sampled at a lower point on the sawtooth ramp and the vco bias voltage is reduced which will decrease the vco rf output frequency to produce the phase lock condition. Conversely, if the phase difference increases (corresponding to a decrease in rf output frequency) the sawtooth is sampled at a higher point on the sawtooth ramp and the vco bias voltage is increased which will increase the vco

rf output frequency to produce the phase lock condition. Once phase-lock is accomplished, the correction cycle is halted and the vco bias voltage remains fixed.

### **2-13. Electrical Frequency Synthesizer 1A14/2A14 Detailed Block Diagram Description (fig. 5-13)**

The functional relationships between the plug-in components 1A14A1 through 1A14A8 and chassis components are shown. Plug-in components 1A14A1 through 1A14A6 are functionalized and the signal paths through each component and between each component are shown. Components 1A14A7 and 1A14A8 are shown as single blocks on the diagram because they are sealed units (nonrepairable). Paragraphs 1-13a through 2-13e provide a detailed block diagram description of electrical frequency synthesizer 1A14 used in the T-1054/GRC-144. The components are described in signal flow sequence starting with rf output signal from 1A114A1 and proceeding through the phase-lock loop components (1A14A2, 1A14A4, 1A14A5, 1A14A6, 1A14A3). The descriptions also apply to electrical frequency synthesizer 2A14 used in the R-1467/GRC-144, except the reference designations are prefixed with 1A14 instead of 2A14 and the word transmitter is used instead of receiver.

a. *Radio Frequency Oscillator 1A14A1 Block Diagram Description* (fig. 5-13). Radio frequency oscillator 1A14A1 consists of three printed circuit boards (A2, A3, and A4) and one encapsulated vco subassembly Y1. When 28 vdc is applied to board A3, regulator VR1 and lamp circuits on board A3 are energized. The regulator applies 21 vdc to vco subassembly Y1 and to boards A2 and A4. The vco subassembly Y1 produces an rf signal between 284.3750 MHz and 303.1250 MHz which is applied to boards A2 and A4. The specific rf signal depends upon the vco bias signal level (4.5 vdc to 16.0 vdc) applied to vco subassembly Y1.

(1) *Board A4*. The rf output signal between 284.3750 MHz and 303.1250 MHz from vco subassembly Y1 is amplified by buffer amplifier Q4 and Q5 to a 20 milliwatt output level. The amplified rf output (high) signal, is applied through the main chassis OUTPUT connector (synth output) to the T-1067/RC14 local oscillator circuits. A sample of the amplified signal from the buffer amplifier Q4 and Q5 is detected

by meter detector diode CR3 to produce a dc current proportional to the rf signal level. The meter current (detected rf level) is 25 microamperes when the rf output (high) signal level is 20 milliwatts. The detected rf level is applied through main chassis low pass filter 1A14RL4 and applied to synthesizer position of meter panel assembly 1A15A8 meter selector switch as a synth level signal used to monitor output of electrical frequency synthesizer 1A14.

(2) *Board A2.* The rf output signal (between 284.3750 MHz and 303.1250 MHz) from vco subassembly Y1 is amplified by digital amplifier Q1 and Q2 to a 1 milliwatt output level. The amplified rf output (low) signal, is applied to electronic frequency converter 1A14A2. The amplified output signal from the digital amplifier Q1 and Q2 is detected by lamp detector diode CR1 and applied to diode CR2 on board AS. The detected signal is then applied to lamp driver Q3 on board A3. When the rf output level from the digital amplifier is 1 milliwatt (normal condition), the detected signal biases the lamp driver Q3 off causing the failure lamp DS1 to be extinguished. When the rf output level from the digital amplifier Q1 and Q2 drops below 1 milliwatt (alarm condition), the lamp driver Q3 is biased on causing the failure lamp to light red. The lamp is tested by pressing the TEST button on the electrical frequency synthesizer 1A14 front panel.

*b. Electronic Frequency Converter 1A14A2 Block Diagram Description (fig. 5-13).* The electronic frequency converter 1A14A2 consists of two printed circuit boards A1 and A2 that translate the rf output (low) signal from radio frequency oscillator 1A14A1 to an intermediate frequency which is applied to variable 1 frequency divider 1A14A4. The rf output (low) signal is between 284.3750 MHz and is applied to a divide-by-two circuit consisting of Q1, Q2 and Q3 on board A1. The divided signal (142.1875 MHz to 151.15625 MHz) is amplified by rf amplifiers Q4 and Q5 and applied to the local oscillator input port of mixer Z1. The 8 MHz signal from standard radio frequency oscillator 1A114A7 is applied to board A2 where it is multiplied by 16 through multiplier stages Q1, Q2, and Q3 producing a 128 MHz output signal. The resultant 128 MHz signal is applied through emitter follower Q4 to the signal input port of mixer Z1 on board A1. The mixer Z1 output is the difference frequency (14.1875 MHz to 23.5625 MHz) of the two input signals to the mixer Z1. The 14.1875 MHz to 23.5625 MHz if output signal is amplified through video amplifiers Q6 and Q7 and applied to variable 1

frequency divider 1A14A4. The amplified 14.1875 MHz if output signal is also applied to bias diode CR6 on board A1 which rectifies the signal to provide a turn-off bias voltage for lamp driver Q8. With lamp driver Q8 turned off, the failure lamp DS1 is extinguished (normal condition). When the if output signal is not present or drops to a low level, the turn-off bias is reduced and lamp driver Q8 turns on causing the failure lamp DS1 to light red (alarm condition). The failure lamp DS1 is tested by pressing the TEST button on the electrical frequency synthesizer 1A14 front panel. Pressing the TEST button applies 5 vdc to lamp driver Q8 producing a bias which over rides the turn-off bias and causes failure lamp DS1 to light. Voltage regulator diode CR,5 on board A1 produces 6.2 vdc which is applied to rf amplifier (Q4 and Q5), the divide-by-two circuit Q1 through Q3 and lamp driver circuit Q8.

*c. Variable Frequency Dividers 1A14A4 and 1A14A5 Block Diagram Description (fig. 5-13).*

(1) *General.* The variable frequency divider modules divide the if output frequency from 1A14A2 in accordance with the thumbwheel switch settings (4400.0 MHz to 5000.0 MHz) to produce the divide-by-N output pulses. As stated previously, the variable divider circuits have the capability of dividing the if output frequency by 16,000, but the divisor is limited to a number from 9080 to 15080 by the thumbwheel switch settings ((2) below). The thumbwheel switches provide ground connections to the switch gate inputs of the variable frequency divider modules in accordance with their settings (para 2-56a). The ground connections preset the number in the associated registers. The 1000 MHz and 10 MHz thumbwheel switches preset the divide-by-eight ripple through counter registers in 1A14A5 with a number from 4 to 7. The 10 MHz thumbwheel switch presets the 10 MHz divide-by-ten registers in 1A14A5 with a number from 0 to 9. The 1 MHz thumbwheel switch presets the 1 MHz divide-by-ten registers in 1A14A4 with a number from 0 to 9. The 0.1 MHz thumbwheel switch presets the 0.1 MHz divide-by-ten registers in 1A14A4 with a number from 0 to 9. Variable 1 frequency divider 1A14A4 also contains a circuit which divides the if output frequency by two before it is applied to the 0.1 MHz divide-by-ten registers. The registers in both modules count down the divided-by-two if output frequency until the count in the registers reaches unique numbers

(decimal 74 and 64) in 1A14A5 and 1A14A4 respectively. The unique number of 7464 establishes the upper frequency limit for the divisor required for dividing the if output from 1A-14A2 ((2) below). When the number 7464 is decoded, the control circuits reset the registers to an initial condition and the registers are preloaded with the count set by the thumbwheel switch settings. After the preloading sequence, the if signal causes the registers to count down to zero. The next pulse produces the divide-by-N pulse output from 1A14A6. The pulse width of the divide-by-N output is equal to 40 periods of the if output signal whose sinewave frequency is between 14.1075 MHz and 23.525 MHz depending upon the rf output frequency of 1A14A2. The registers in 1A14A5 contain the most significant bits and will reach their unique number (decimal 74) before the registers in 1A14A4 have reached their number (decimal 64).

(2) *Thumbwheel switch settings/divisor ratios.*  
 Variable frequency dividers 1A14A4 and 1A14A5 divide the 14.1875 to 23.5625 MHz if output frequency from 1A14A2 by a number from 9080 to 1.5080 depending upon the thumbwheel switch settings. The 14.1875 MHz to 23.5625 MHz if output frequency is divided down to 1.5625 kHz to accomplish phase-lock. For example, for a thumbwheel setting of 5000.0 MHz, the required if output frequency is 23.5625 MHz. At this frequency, the variable frequency dividers divide the if output frequency from 1A14A2 by 15080 (23.5625 MHz ÷ 16080 = 1.5625 kHz). The divisor is obtained by adding the counts to reach the unique number, initialize, inhibit and preload sequence count and the thumbwheel settings (1 + 536 + 3 + 7000 = 7540). Multiplying the count by two (2 x 7540 = 15080) supplies the divisor. The count is multiplied by two because the frequency of the if output is divided by two in 1A14A4 before it is applied to the registers. The following subparagraphs describe how a thumbwheel switch setting of 5000.0 MHz produces a divisor of 15080 in the variable frequency divider circuits.

(a) For a thumbwheel switch setting of 5000.6 MHz, the 0.1 MHz, 1.0 MHz, and 10 MHz divider-by-ten registers in variable frequency dividers 1A14A4 and 1A14A5 are preloaded with zeros. The divide-by-eight ripple through registers are preloaded with zeros. The divide-by-eight ripple through registers are preloaded with the number 7 ((c) below). The countdown cycle starts at 0000 (1 count), then counts down from 7999 to the unique number of 7464 (536 counts), after this count an initialize, inhibit, preload sequence takes place (3 counts) and the thumbwheel switch settings are loaded into the registers. The registers then count down from

7000 (corresponds to 5000.0 MHz) through 0000 (7000 counts) until the unique number appears again in the registers. The cycle then repeats as described above.

(b) Note that any divisor (D) can be calculated by adding 540 to the number (N) preloaded into the registers and multiplying by 2 (D = 2 (N) + 540). For example, for a thumbwheel switch setting of 4400.0 MHz, the number preloaded into the registers is 4000. The divisor is calculated as follows: 2(4000 + 540) = 2(4640) = 9080.

(c) The following tables list the thumbwheel switch settings with corresponding closed switch contacts (fig. 5-13) and the resulting decimal numbers which are loaded into the associated registers.

1. *S1-I and S1-II.*

1000 MHz and 100 MHz switch settings	Closed switch contacts	Decimal number preloaded into ripple through register (÷ 8)
44 -----	NONE	4
45 -----	C	5
46 -----	B	6
47 -----	None	4
48 -----	C	5
49 -----	B	6
50 -----	B NAD C	7

2. *S1-III.*

10 Mhz switch settings	Closed switch contacts	Decimal number preloaded into ripple through register (÷ 10)
0 -----	A,B,C,D,E	0
1 -----	B,C,D,E	1
2 -----	C,D,E	2
3 -----	D,E	3
4 -----	E	4
5 -----	NONE	5
6 -----	A	6
7 -----	A,B	7
8 -----	A,B,C	8
9 -----	A,B,C,D	9

3. *S1-IV or S1-V.*

1 MHz or 0.1 MHz switch setting	Closed switch contacts	Decimal number preloaded into 1 MHz register (÷ 10) or 0.1 MHz register (÷ 10)
0 -----	NONE	0
1 -----	1	1



MHz switch 1 MHz or 0.1 setting	Closed switch contacts	Decimal number preloaded into 1 MHz register ( $\sim 10$ ) or 0.1 MHz register ( $\sim 10$ )
2 -----	2	2
3 -----	1,2	3
4 -----	4	4
5 -----	1,4	5
6 -----	2,4	6
7 -----	1,2,4	7
8 -----	8	8
9 -----	1,8	9

(3) *Variable 1 frequency divider 1A14A4 block diagram description* (fig. 5-13). With the thumbwheels set for 5000 MHz, the if output signal of 23.5655 MHz from 1A14A2 is applied to board A1 on variable 1 frequency divider 1A14A4 where it is clamped by diode CR1 and applied to the divide-by-2 circuit Z1 through driver Q1. The divided pulses are inverted through input inverter Z2 and are the clock pulses for operating both the first stage of the 0.1 MHz divide-by-10 register and the control flip-flops Z5 and Z7. The countdown cycle begins when all stages of the two registers 0.1 MHz and 1 MHz contain zeros and control flip-flops Z5 and Z7 are reset. The next pulse from the input inverter Z2 triggers the 0.1 MHz register which triggers the 1 MHz registers which in turn produces a count output. This count output is applied through count inverter Z14 to variable 2 frequency divider 1A14A5 where it triggers the 10 MHz register; this triggers the divide-by-8 ripple-through counter registers which triggers the output register and produces the divide-by-N (N) pulse. After 20 pulses from the input inverter Z2 (equal to 40 periods of the if output signal), an overflow from the 0.1 MHz divide-by-10 register into the 1 MHz divide-by-10 register causes an output reset pulse to be applied to variable 2 frequency divider 1A14A5 which resets output register Z10 in 1A14A5. The divide by-N (N) output is then applied to the fixed frequency divider 1A14A6 through output inverter Z1 on 1A14A5.

(a) The clock pulses from input inverter Z2 are applied to the registers causing the count down sequence (0000 to 7464). At the unique count (decimal 74, 1 + 536 count), the registers in variable 2 frequency divider 1A14A5 are decoded and produce a reset enable level which is applied to control circuits in variable 1 frequency divider 1A14A4. The reset enable level from reset enable gate Z1 on board A1 of 1A14A5 is applied to control gate Z3 through the reset inverter Z14 on board A2 of 1A14A4. When the reset enable level is received and the count in the 0.1 and 1 MHz divide-by-10 registers reach the unique count (decimal 64, 1 + 5386 count) required by control gate Z3, flip-flop Z5

becomes set. When flip-flop Z5 is set, the initialize pulse (537 + 1 count) is applied to all the registers in 1A14A4 and 1A14A5 which sets the registers to a count which enables the registers to be modified by the thumbwheel switch setting. The initialize pulse also prevents an additional count from being accumulated by the 1.0 MHz register.

(b) The next clock pulse following the initialized condition is not counted by the registers but sets flip-flop Z7. When flip-flop Z7 is set, the initialize condition is terminated and an inhibit level is produced (537 + 2 count) and applied to all registers. The next clock pulse resets flip-flop Z5 but is inhibited to the registers. When flip-flop Z5 is reset, a preload pulse (537 + 3 count) is generated and applied to the register switch gates Z4, Z9 and Z16 on board Z2 causing the switch gates Z4, Z9 and Z16 to open (540 count). With the switch gates Z4, Z9 and Z16 opened, the thumbwheel switch settings modify the count in the registers.

(c) The next clock pulse is applied to the registers and resets flip-flop Z7, this terminates the inhibit condition. The registers will then count down from the preloaded count to all zeros, during the next count down cycle.

(d) Bias diode CR6 on board A1 of 1A14A2 rectifies the count output signal to provide a turn-off bias for the lamp driver Q8. With the lamp driver Q8 turned off, failure lamp DS1 is extinguished. When the count output signal is not present or drops to a low level, the turn-off bias is reduced and lamp driver Q8 turns on causing the failure lamp DS1 to light red (alarm condition). Pressing the TEST button on the frequency synthesizer front panel applies 5 vdc to the lamp transistor driver causing the failure lamp to light red.

(4) *Variable 2 frequency divider 1A14A5 block diagram description* (fig. 5-13). Variable 2 frequency divider contains one printed circuit board A1 that divides the output from variable 1 frequency divider 1A14A4 in accordance with the settings of the 1000-, 100-, and 10 MHz thumbwheel switch sections (5000.0 MHz for this description). The count pulse from variable 1 frequency divider 1A14A4 are applied to the 10 MHz divide-by-10 register Z3 through Z6. The output pulses from the 10 MHz divide-by-10 register trigger the divide-by-eight ripple through counter registers Z7, Z8 and Z9.

(a) The count down-cycle continues until all of the registers Z2 through Z9 contain zeros. The next count pulse triggers the divide-by-eight ripple-through counter registers Z7, Z8, and Z9 which sets the output register Z10 and produces a divide-by-N ( $\div N$ ) pulse. At this time one of the 10 MHz registers conditions the output register Z10 to be reset. After 40 cycles of the if output frequency signal have been counted in variable 1 frequency divider 1A14A4 an output reset signal is sent to reset output register Z10 which terminates the divide-by-N pulse. At the unique count (decimal 74, 1 + 536 count), the registers in 1A14A5 are in the required condition to satisfy the conditions for the reset enable gate Z1 and a reset enable level is applied to variable 1 frequency divider 1A14A4. When the registers in variable 1 frequency divider No. 1 1A14A4 are at their unique count (decimal 64, 1 + 536 count), control flip-flops Z5 and Z7 on 1A14A4 are triggered to produce the inhibit, initialize, and preload signals (537 + 3 count). The inhibit level is applied to the 10 MHz counter register prevent it from accumulating a false count. The initialize pulse is applied to the registers in variable 2 frequency divider and they are set to a count which enables the registers to be modified by the thumbwheel switch settings. The preload pulse is applied to all the register switch gates Z12 through Z14 causing the switch gates to open. With the switch gates Z12 through Z14 opened, the thumbwheel switch settings modify the count in the registers. The preloaded registers then count down during the next count-down cycle.

(b) The divide-by-N signal is monitored by lamp driver Q1 and if it is not within the required amplitude and frequency limits, the lamp bias changes and failure lamp DS1 lights red. Pressing the TEST button on the frequency synthesizer 1A14 front panel applies 5 volts dc directly to the lamp transistor driver circuit causing the failure lamp DS1 to light red. For normal operating conditions the failure lamp DS1 is extinguished.

*d. Fixed Frequency Divider 1A14A6 Block Diagram Description (fig. 5-13).*

(1) Fixed frequency divider 1A14A6 contains two printed circuit boards A1 and A2 that perform three functions: (1) the 8.0 MHz signal from the standard radio frequency oscillator 1A14A7 is divided by 5120 to produce the 1.5625 kHz reference signal, (2) the 1.5625 kHz reference signal and the divide-by-N ( $\div N$ ) signal from variable 2 frequency divider 1A14A5 are compared, and (3) if the signals are not in phase, fixed

frequency divider 1A14A6 generates a phase-lock alarm signal and produces the two-bit correction codes for the audio frequency phase error detector 1A14A3.

(2) The 8.0 MHz sinusoidal signal from standard radio frequency oscillator 1A14A7 is applied to board A2. The 8.0 MHz signal is changed by clamp diode CR1 and inverted through inverter Z15 and applied to divider stages Z1 through Z10 and Z11 through Z13. These stages divide the 8 MHz signal by 5120 to provide the 1.5625 kHz reference signal. The 1.5625 kHz reference signal is applied to audio frequency phase error detector 1A14A3 through output register Z14 and inverter Z24. The 1.5625 kHz reference signal is also applied to fixed frequency divider board A1 through output register Z14. The 1.5625 kHz output from divider Z13 is monitored by failure lamp DS1 through bias diode CR3 and lamp driver Q1. For normal conditions, lamp driver Q1 is turned on and a transistor in the lamp assembly is turned off causing failure lamp DS1 to be extinguished. When the 1.5625 kHz output from divider Z.1S is not present, lamp driver Q1 turns off and the transistor in the lamp assembly turns on causing failure lamp DS1 to light red. Pressing the TEST button on electrical frequency synthesizer 1A114 front panel applies 5 vdc to the lamp transistor driver causing the failure lamp to light red.

(3) The divide-by-N signal from variable 2 frequency divider 1A14A5 is also applied to board A1 of 1A14A6 where it is compared with the 1.5625 kHz reference signal in the phase-lock detector circuits Z16 through Z18. If the signals are in phase, the phase-lock detector circuits are balanced. For this condition (phase-loop locked), the output of the phase-lock detector circuits is unchanged and no signals are applied to inverter Z24. The output of inverter Z24 is applied through alarm bias diode CR1 to the failure lamp DS1 assembly and to alarm driver Q2. With no signals applied to inverter Z24, failure lamp M1 is extinguished (normal condition) and alarm driver Q2 is turned off. The output from alarm driver Q2 is applied through main chassis low pass filter 1A14FL3 (synth lock) to the SYNTH LOCK indicator on meter panel assembly 1A15A8. With alarm driver Q2 turned off, the SYNTH LOCK indicator lights green (normal indication). If the divide-by-N pulses and the 1.6625 kHz signals are not in phase, the phase-lock detector circuits become unbalanced and squarewave pulses are applied

to inverter Z24. For this condition (phase loop unlocked), failure lamp DS1 on 1A14A6 lights red (alarm condition) and alarm driver Q2 turns on. With alarm driver Q2 turned on, the SYNTH LOCK indicator on meter panel assembly 1A15A8 also lights red (alarm condition).

(4) The output of the phase-lock detector circuits is also applied to counter circuit Z19 through Z23. With the phase-lock detector circuits balanced (phase-lock condition), the counter remains in a fixed condition. Therefore, the output of the counter is fixed causing the output of the two-bit gates Z18 to be fixed. For this condition, the two-bit correction signal ( $2^0$  and  $2^1$ ) applied to af phase error detector 1A14A3 remains fixed. When the phase-lock detector circuits become unbalanced (phase loop unlocked), the counter begins counting and the two-bit correction signal is applied to phase error detector 1A14A3 cycles through its four conditions (00, 01, 10, and 11).

*e. Audio Frequency Phase Error Detector 1A14AS Block Diagram Description (fig. 5-13).*

(1) Audio frequency phase error detector 1A14A3 consists of one printed circuit board A1 that converts the phase difference between the 1.5625 kHz reference signal from fixed frequency divider 1A14A6 and the divide-by-N signal from variable 2 frequency divider 1A14A5 into a bias voltage which controls the frequency of the vco in oscillator 1A14A1. The 1.5625 kHz pulses from fixed frequency divider 1A14A6 are applied to sawtooth generator Q3 and Q4 to restart the sawtooth waveform. The divide-by-N signal controls sample and hold circuit Q7 which samples the sawtooth signal and controls the hold signal transistors buffer amplifiers Q10 and Q11. When the 1.5625 kHz reference signal and the divide-by-N pulses are identical in frequency (zero time phase variation), the sampling point will occur at the same point on the sawtooth ramp resulting in a constant hold voltage. When the two signals are not identical in frequency (a changing time phase), each sample will occur at a different point on the sawtooth ramp resulting in a varying hold voltage (sawtooth in characteristic). The frequency of the varying hold voltage is equal to the difference frequency between the 1.5625 kHz reference signal and the divide-by-N pulses. The sampled voltage level is amplified by dc amplifier Q12, and Q13, filtered, and applied to the vco subassembly Y1 in 1A14A1 as a vco bias varying voltage to correct the output frequency. Thus, the reference and divide-by-N pulses are brought to the

same frequency (no time phase variation between them).

(2) The pull-in frequency range of the phase lock process is restricted to a portion of the total vco frequency range (rf output frequency range). In order to accomplish phase-locking of the vco over its entire range, it is necessary to "step change" the vco frequency in four discrete increments each increment being less than the phase-lock loop pull-in range. This is implemented by coarse tuning the vco bias voltage in four discrete dc voltage steps produced by the two-bit correction code ( $2^1$  and  $2^0$ ) and digital-to-analog converter Q8 and Q9. In a out-of-lock condition, the correction code cycles through its four states, 00, 01, 10, and 11 causing the vco bias voltage to cycle through its four step voltage levels. The sawtooth waveform is superimposed on each step level and is of sufficient amplitude to overlap adjacent step levels. Thus, the sawtooth provides the fine tuning vco bias voltage within each step voltage change. The composite signal is used to phase-lock the vco subassembly Y1. When the combined step voltage and sawtooth covers the portion of the bias voltage range that includes the desired rf output frequency, the loop starts to phase-lock. When phase-lock is achieved, the correction code cycling halts in one of its four coded states producing a corresponding fixed coarse tuning vco bias voltage. The constant stored voltage used to bias the vco to the exact frequency required is the combined coarse tuning dc voltage level and the fine tuning fixed error correction voltage produced by constant point sampling of the sawtooth ramp. For any given required vco frequency setting, the phase-lock loop automatically selects the correction code state and the sawtooth constant sampling point to maintain a phase-lock condition. Within any two coarse tuning increments, the sawtooth constant sampled point is positioned along the sawtooth ramp producing the required vco fine tuning frequency increments. The loop automatically positions the constant sampling point by adjusting the fixed phase difference between the identical frequency 1.5625 kHz reference pulses and the divide-by-N sampling pulses. The higher the required vco frequency, the greater the phase difference, the higher the sawtooth ramp constant voltage sampling point.

(3) The sawtooth waveform output from the saw-generator Q3 and Q4 is buffered by Q5 and Q6 and rectified by ac detector Q1. The resulting dc voltage biases the transistor in failure

lamp DS1 assembly off, causing failure lamp DS1 to be extinguished. When the sawtooth signal is not present or its amplitude drops to a low level, the ac detector biases the transistor in failure lamp DS1 assembly on, causing failure lamp DS1 to light red (alarm condition). Pressing the TEST button on electrical frequency synthesizer 1A14 front panel applies 5 vdc to the failure lamp transistor causing the lamp to light red.

(4) Voltage regulator Q02 provides 20 vdc to operate transistor circuits Q3 through Q6 and Q8 through Q13.

#### **2-14. Alarm-Monitor 1A5 Block Diagram Description (fig. 5-14)**

a. Alarm monitor 1A5 receives monitor signals (traffic monitor, forward rf power monitor, reflected rf power monitor, and synthesizer monitor signals) and controls the associated alarm indicators on transmitter meter panel assembly 1A15A8. Depending upon the signal level received, the associated indicator lights either green (normal indication) or red (alarm indication). The alarm monitor also contains a summary alarm circuit which is enabled when any one of the alarm conditions occur. The traffic monitor signal indicates the signal level input to radio transmitter modulator 1A8. The forward rf power monitor and reflected rf power monitor signals indicate the power levels at the output of the T-1054/GRC-144. The synthesizer monitor signal is received directly from electrical frequency synthesizer 1A14 and indicates if the signals from variable 2 frequency divider 1A14A5 and standard radio frequency oscillator 1A14A7 are phase locked. An identical alarm monitor 2A12 is used in the R-1467/GRC-144; however, the jumper connections on the associated plate assembly connectors are different for each assembly. Alarm monitor 2A1,2 is described in paragraph 2-24.

b. The following description is based on the circuits shown in figure 5-14.

(1) The TRAF, RF POWER, REFL RF POWER, and SYNTH LOCK indicators on the meter panel assembly 1A16A8 are controlled by Schmitt trigger circuits in alarm monitor 1A5. The Schmitt trigger circuits cause the associated indicators to light green (normal indication) or red (alarm condition). The input signals to the alarm monitor control the operation of the associated Schmitt trigger circuits.

(2) The traffic monitor signal is supplied by radio transmitter modulator 1A8 through attenuator assembly 1A3. The traffic monitor signal is applied directly to operational amplifier (integrated circuit) AR1. The operational amplifier output is detected and applied to the traffic meter through a potentiometer and to Schmitt trigger circuit Q5, Q6 through dc emitter follower Q1. If the traffic monitor signal exceeds a predetermined level, the dc voltage developed by the detector CR1 and CR2 will cause Q5 to turn on, causing Q6 to turn off and Q7 to turn on. With Q7 turned on, a low impedance path to ground is provided for the normal traffic indicator lamp, and the TRAF indicator lights green. Since Q6 is turned off, a high impedance path to ground is provided for the alarm traffic indicator lamp causing the indicator lamp (red) to remain off. When the traffic monitor signal falls below the predetermined voltage, the dc voltage applied to the base of Q5 is not sufficient to keep Q5 conducting. With Q5 turned off, Q6 turns on and Q7 turns off. For this condition, a high impedance path to ground is applied to the normal traffic indicator lamp and a low impedance path to ground is applied to the alarm traffic indicator lamp. Consequently, the TRAF indication changes from green to red. Also with Q7 turned off, the Q7 output dc voltage is high, enabling the OR gate which causes Q23 to turn on. With Q23 turned on, a transmitter summary alarm indication is provided.

(3) The synthesizer monitor signal is derived from electrical frequency synthesizer 1A14. The signal (dc level) is applied directly to Schmitt trigger Q14, Q15. Circuit operation is identical to that described above for the traffic monitor circuit. If the synthesizer monitor signal exceeds the predetermined dc level, the SYNTH LOCK indicator lights green (normal indication). If the synthesizer monitor signal is below the predetermined level, the SYNTH LOCK indicator lights red (alarm condition) and, in addition, the summary alarm circuit is enabled.

(4) The forward rf power monitor signal is a detected dc voltage supplied by directional coupler 1DC1. The dc signal is applied to operational amplifier (integrated circuit) AR3 and the meter selector switch on meter panel assembly 1A15A8 through an attenuator. The output of AR3 is applied directly to Schmitt trigger Q11, Q12. The operation of the Schmitt trigger is identical to that described above for the traffic monitor circuit. If the rf power monitor signal exceeds the predetermined dc level, the RF

POWER indicator lights green (normal indication). If the rf monitor signal is below the predetermined level, the RF POWER indicator lights red (alarm indication) and the summary alarm circuit is enabled.

(5) The reflected rf power monitor signal is a detected dc voltage supplied by directional coupler 1DC1. The dc signal is applied to operational amplifier (integrated circuit) AR2 through a variable attenuator circuit. An output from the attenuator circuit is also applied to the meter selector switch on meter panel assembly 1A15A8. The output of AR2 is applied to Schmitt trigger Q8, Q9. The operation of Schmitt trigger Q8, Q9 is similar to that previously described for the other monitor circuits except the alarm and normal outputs are revised. The outputs of Schmitt trigger QS, Q9 are reversed because it is the presence rather than the absence of a dc voltage at the Schmitt trigger input that results in an alarm condition.

(6) The summary alarm circuit is comprised of the diode OR gate CR12-CR15 and transistor Q23. Each of the normal outputs is connected to the OR gate. For normal operation, transistor Q23 is off (nonconducting). When any one of the alarm conditions occur, the OR gate switches Q23 on (conducting state) causing a transmitter summary alarm condition.

## 2-15. Radio Test Set (p/OIA16) Block Diagram Description (fig. 24)

The radio test set provides a test output signal from Transmitter, Radio T-1054/GRC144 which is applied to Receiver, Radio R-1467/GRC-144. The test output signal is obtained by mixing a sample of the rf output from directional coupler 1DC1 in the T-1054/GRC-144 with the output from 100 MHz radio frequency oscillator 1A2. The resulting test output signal is separated by 100 MHz from the rf output signal is used to align, test, or troubleshoot Radio Set AN/GRC-144. The radio test set is comprised of 100 MHz radio frequency oscillator 1A2, crystal mixer 1A16Z1, variable attenuator 1A16AT1, and the radio test set panel (part of plate assembly 1A16). The OUTPUT LEVEL control for the variable attenuator, a meter switch, and a meter are provided on the radio test set panel. The meter switch permits monitoring of the 100 MHz radio frequency oscillator's output level and the crystal mixer diode currents of mixer diodes 1A16Z1CR1 and 1A16Z1CR2.



a. When testing, aligning, or troubleshooting the R-1467/GRC-144, two 100 MHz signals are applied to crystal mixer diodes 1A16Z1CR1, and 1A16Z1CR2. The 100 MHz signals are generated when the 100 MHz rf oscillator's ON-OFF switch is placed in the ON position. With the switch in the ON position, the indicator on 1A2 is lighted, the RADIO TEST SET indicator on meter panel assembly 1A15A8 is lighted red and supply voltage is applied to the oscillator circuit. The LEV ADJ control is used to adjust the oscillator's output level. The output level is monitored by setting the meter switch to the OSC LEV position. The meter face is marked to indicate the proper oscillator output level. The crystal mixer diode currents (CR1 or CR2) can also be monitored by setting the meter switch to the appropriate position.

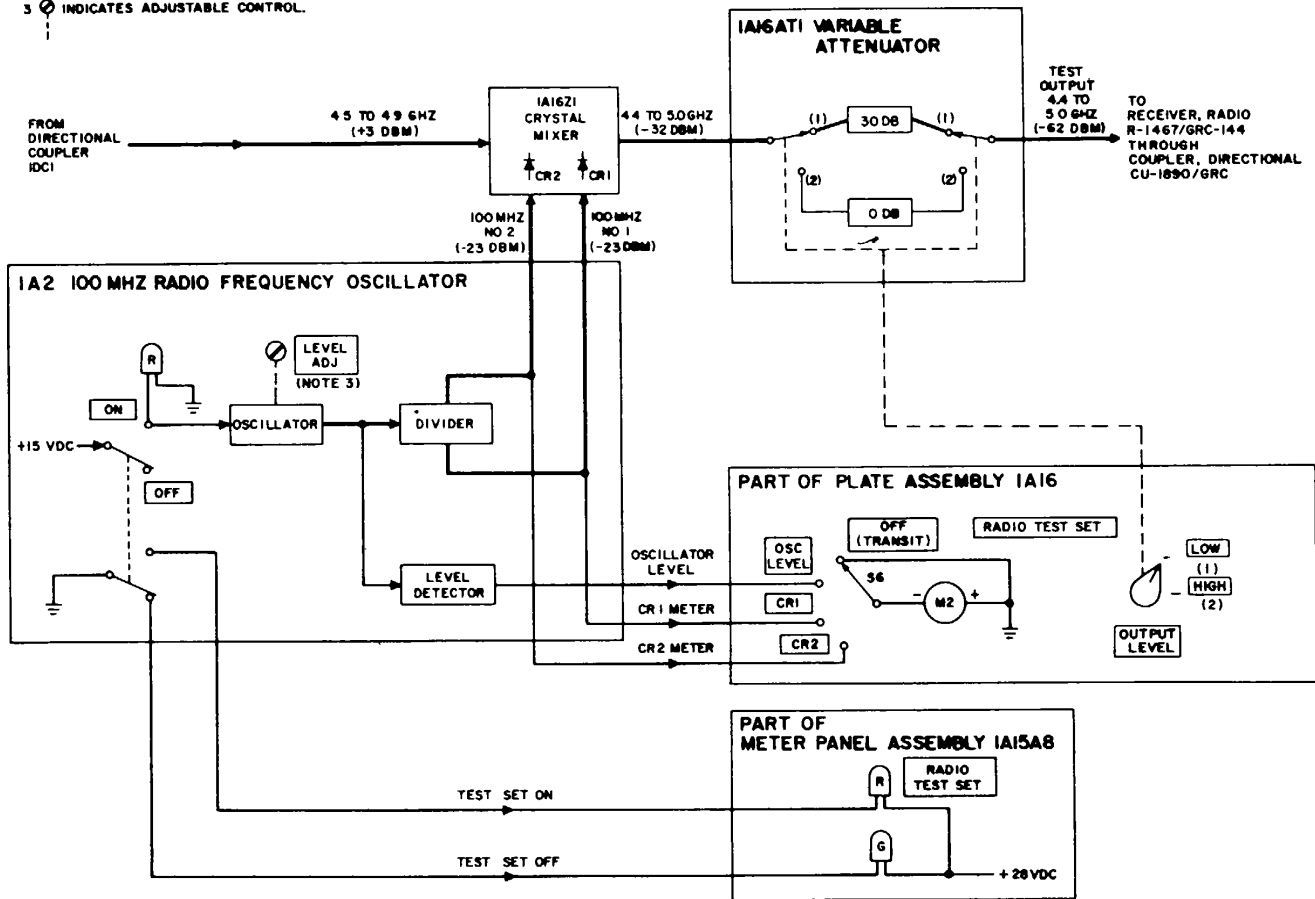
b. Crystal mixer 1A16Z1 receives a sample of the rf output signal from directional coupler 1DO1. The signal is in the 4.6 to 4.9 GHz frequency range at a level approximately 21 db down from the rf output. This signal is mixed with the 100 MHz output signal from 1A2 producing frequencies 100 MHz above and below the 4.5 to 4.9 GHz input. The signal level output of the crystal mixer is approximately -32 dbm (9 db below each 100 MHz input level to the crystal mixer). Variable attenuator 1A16AT1 provides two attenuation levels (0 and 30 db). With the OUTPUT LEVEL control set to the HIGH position, variable attenuator 1A16AT1 provides 0 db attenuation. With the OUTPUT LEVEL control set to the LOW position, variable attenuator 1A16AT1 provides 30 db  $(\pm 1 \text{ db})$  attenuation. The receive threshold level is approximately -91 dbm. The -91 dbm test input level to Receiver, Radio R-1467/GRC-144 is obtained as follows: (1) The output of crystal mixer 1A16Z1 is approximately 42 dbm (level was set by adjusting the LEVEL ADJ control on 1A2).

(2) Variable attenuator 1A16AT1 provides 30 db attenuation when the OUTPUT LEVEL control is set to the LOW position. Thus, the output of 1A16AT1 is -62 dbm.

(3) Coupler, Directional CU-1890/GRC provides a fixed decoupling loss of 20 db. A variable attenuator in the CU-1890/GRC provides an additional loss of 0 to 20 db. The variable attenuator is calibrated at the direct support level to provide the remaining loss required for a -91 dbm input to the R-1467/GRC-144. The variable attenuator in the CU-1890/GRC compensates for inequalities in the rf cabling and

NOTES:

- 1 ALL POWER LEVELS ARE APPROXIMATE AND ARE TO BE USED FOR REFERENCE ONLY
- 2  INDICATES FRONT PANEL MARKING
- 3  INDICATES ADJUSTABLE CONTROL.



EL5820-695-35-TM

Figure 2-4. Radio test set (p/o 1A16), block diagram.

other rf components between crystal mixer IA16-Z1 and the input to Receiver, Radio I R-1467(P)/GRC-144(V).

c. Variable attenuator 1A16AT1 provides 0 dB attenuation when the OUTPUT level control is set to the HIGH position. Consequently, the input to Receiver, Radio R-1467(P)/GRC-144(V) is 30 dB above threshold or approximately -61 dBm.

d. To ensure that the output pcm pulses from the demodulator circuits in Receiver, Radio R-1467(P)/GRC-144(V) are the same polarity as the input pcm pulses to the modulator circuits in Transmitter, Radio T-1054(P)/GRC-144(V), the T-1054(P)/GRC-144(V) must be tuned 100 MHz higher or lower than the R-1467(P)/GRC-144(V) operating frequency as follows:

(1) If the R-1467(P)/GRC-144(V) is tuned to any frequency between 4400.0 and 4699.9 MHz, the T-1054(P)/GRC-144(V) must be set in the same band between 4400.0 and 4699.9 MHz. For example, if the receiver carrier frequency is 4685.2 MHz, the transmitter carrier frequency must be set to 4585.2 MHz (but not 4785.2 MHz) in order to operate in the radio test set.

(2) If the R-1467(P)/GRC-144(V) is tuned to any frequency between 4700.0 and 5000.0 MHz, the T-1054(P)/GRC-144(V) must be set in the same band between 4700.0 and 5000.0 MHz. For example, if the receiver carrier frequency is 4785.7 MHz, the transmitter carrier frequency must be set to 4885.7 MHz (but not 4685.7 MHz) in order to operate the radio set.

e. When the radio test set is not in use, 100 MHz radio frequency oscillator 1A2 must be turned off. With the ON-OFF switch on 1A2 in the OFF position, the indicator on 1A2 is extinguished, the RADIO TEST SET indicator on the meter panel assembly 1A15A8 is lighted green, and the supply voltage is removed from the oscillator circuits in 1A2. For this condition, the test signal to the R-1467(P)/GRC-144(V) is removed.

## **2-16. Transmitter, Radio T-1054(P)/ GRC-144(V) Primary Power Distribution (fig. 2-5)**

The 115 Vac primary power is applied to the Transmitter, Radio T-1054(P)/GRC-144(V) through AC POWER INPUT connector 1A15A6J18. The 115 Vac input passes through line filters 1A15A6FL1 and FL2 to the POWER ON/OFF switch S3 on meter panel assembly 1A15A8. When the POWER ON/OFF switch is set to the ON position, 115 Vac passes through the 5 AMPS SLOBLO power fuse 1A15A8F1 and is distributed by terminal board 1A15TB3 to transformer 1A15A10T1, electrical frequency synthesizer 1A14 and blower motor 1A15B1. The 115 Vac lines are also distributed from 1A15TB3 to connector pins 1A15J20-A and C (320 FAULT LOCATOR-POWER SUPPLY INTERCONNECT). Connector pins 1A15J20-A, B, and C are provided for future application of Radio Set AN/GRC-144(V). Refer to the Transmitter, Radio T-1054(P)/GRC-144(V) interconnecting diagram (fig. 5-15) for point-to-point primary power connections. For the AN/GRC-144(V)3 and 4 configurations, 115 Vac passes to fan 1A15B1 through thermostatic switch 1A15A17S1.

## **2-17. Transmitter, Radio T-1054(P)/GRC-144(V) DC Power Distribution (fig. 5-16)**

The 115 Vac input to transformer 1A15A10T1 is stepped-down to an output voltages of 8.5, 11, 13.5, 15, 16, 16.5, 27.5, and 30 Vac. The ac output voltages are applied to voltage regulators in power supply 1A1. Four 5/6v voltage regulators, four 12v voltage regulators, and three 15/28v voltage regulators are utilized. A typical voltage regulator circuit is described in paragraph 2-18. The voltage regulators provide regulated dc voltage outputs and associated dc returns. The dc voltages and return lines are distributed to the plug-in assemblies and other cabinet components. Cabinet terminal board 1A15TB3 and plate assembly terminal board 1A15TB1 are used to distributed certain voltages. Refer to the Transmitter, Radio T-1054(P)/-GRC-144(V)

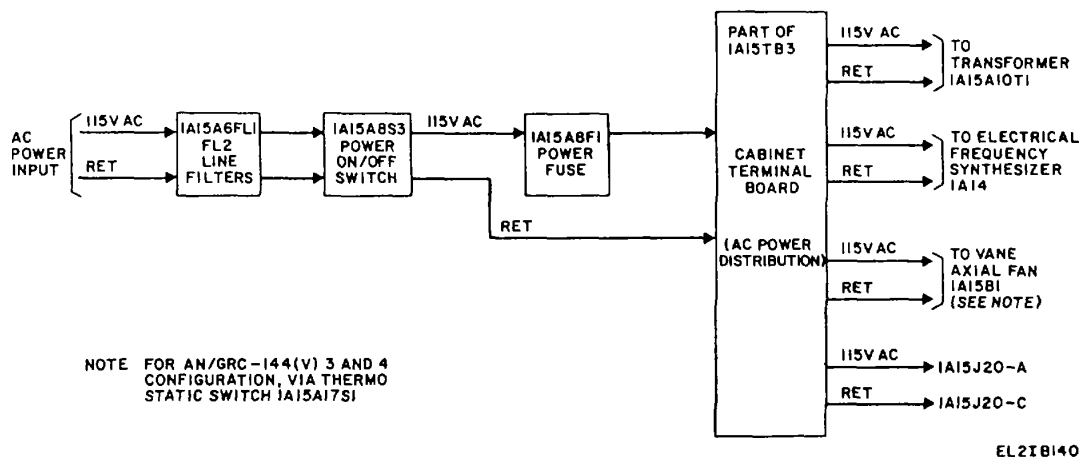


Figure 2-5. Transmitter, Radio T-1054(P)/GRC-144(V) and T-1054(P)/GRC-144(V), primary power distribution block diagram.

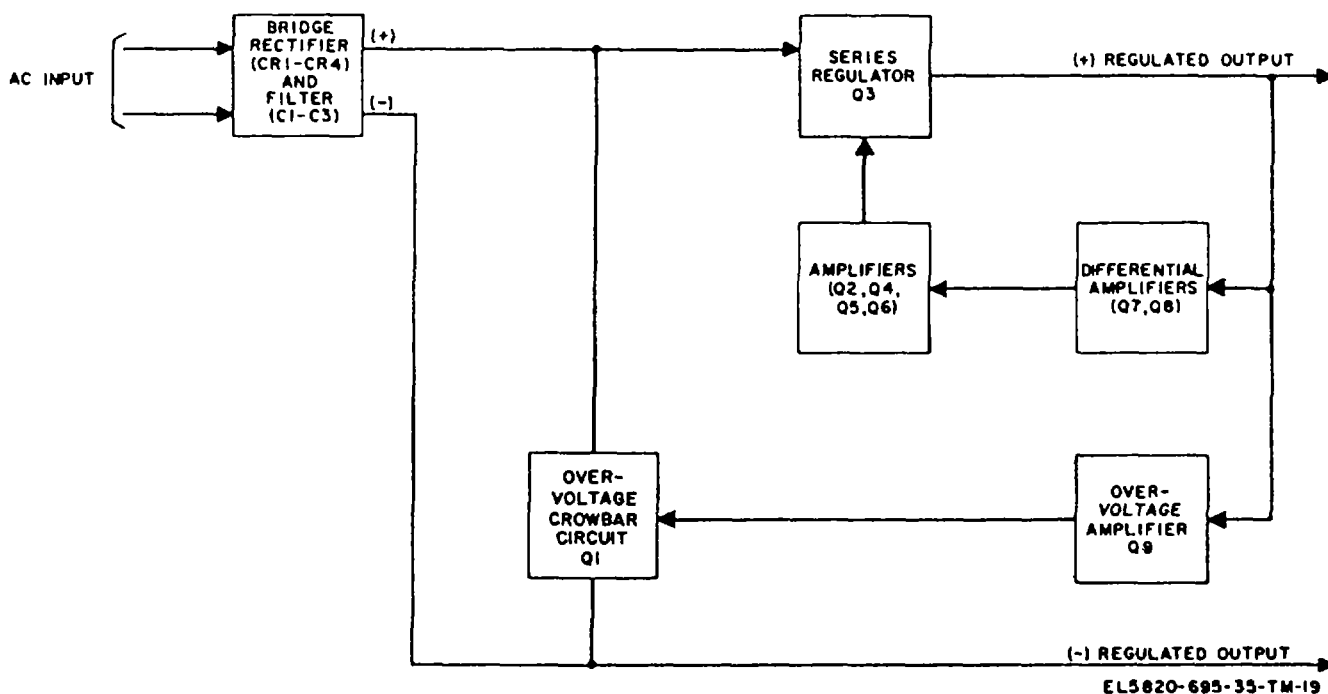


Figure 2-6. Typical voltage regulator 1A1A1-1A1A12, block diagram.

interconnecting diagram (fig. 5-15), and power supply 1A1 interconnecting diagram (fig. 5-17), for point-to-point dc voltage connections.

**2-18. Typical Voltage Regulator 1A1A1 Through 1A1A12 Block Diagram Description (fig. 2-6)**

Since the 5/6v, 12v, and 15/28v voltage regulators are similar, the following description of a 15/28v voltage regulator covers, in general, the operation of all three

regulators. The voltage regulators consist of a bridge rectifier and filter, series regulator, and overvoltage protection circuits. The description is based on the block diagram shown in figure 2-6. Circuit theory descriptions for each regulator are given in paragraph 2-28.

a. Bridge Rectifier and Regulator Circuit  
The output of bridge rectifier CR1 through CR4 is



filtered by capacitors C1 through C3. The filtered output is applied to series regulator Q3. Series regulator Q3, under control of differential amplifier Q7 and Q8, and amplifier Q2, Q4 through Q6, introduces the voltage drop necessary to maintain voltage regulation.

b. Overvoltage Protection Circuit. Overvoltage protection is provided by crowbar circuit Q1. An overvoltage condition at the voltage regulator output is sensed by overvoltage amplifier Q9 which triggers Q1 into conduction. With Q1 conducting, the

bridge rectifier output is short circuited causing the fuse in the ac input line to open.

#### **2-19. Overall Block Diagram Description of Receiver, R-1467(P)/GC-144(V) (fig. 5-18)**

Receiver, Radio R-1467(P)/GRC-144(V) is a superheterodyne receiver which receives an rf input signal in the 4.4 to 5.0 GHz range from a line-of-sight antenna through Duplexer CU-1891/ GRC. The 4.4 to 5.0 GHz rf input signal is

amplified and mixed with a local oscillator signal in the 4.33 to 5.07 GHz range to produce a 70 MHz if signal. The if signal is demodulated to recover the composite pcm and ow signal. The pem and ow signal is amplified for application to digital data modem 1A12 in Transmitter, Radio T-1054/GRC-144. Signal paths through the R1467/GRC-144, the functional relationships between assemblies, and the alarm and metering functions are illustrated in figure 6-18. The signal processing circuits in the R-1467/GRC-44 are functionally divided into rf input circuits, amplifier-mixer circuits, local oscillator circuits, 70 MHz if amplifier circuits and demodulator circuits. Receiver, Radio R-1467/GRC-144 also contains alarm monitoring circuits, meter circuits, and power circuits.

*a. RF Input Circuits.* The rf input circuits consist of preselector bandpass filter 2FL4, tunnel diode amplifier 2A2, and post selector bandpass filter 2FL5. Preselector bandpass filter 2FIA is set to the specific operating frequency in the 4.4 to 5.0 GHz range and passes that frequency. Tunnel diode amplifier 2A2 amplifies the signal, provides isolation, and improves the receiver's noise figure. Post selector bandpass filter 2FL5 is set to the same frequency as 2FL4 and limits the passage of out-of-band noise generated by tunnel diode amplifier 2A2. The operation of an oven within tunnel diode amplifier 2A2 is monitored at meter panel assembly 2A15A2. The amplified output of 2A2 is passed through 2FL5 to amplifier-mixer 2A7.

*b. Amplifier-Mixer Circuits.* Amplifier-mixer 2A7 receives the 4.4 to 5.0 GHz rf input signal from 2FL5 and converts it to a 70 MHz if signal. Conversion is made by mixing the 4.4 to 5.0 GHz rf input signal from 2FL5 with a 4.33 to 5.07 GHz local oscillator signal from 2A8 applied through 2FL6. The local oscillator signal is 70 MHz above or below the rf input signal. Diode currents generated within 2A7 are selectable by a meter selector switch for monitoring on meter panel assembly 2A15A2. The amplified 70 MHz if output of 2A7 is applied through 70 MHz bandpass filter 2A6 to 70 MHz intermediate frequency amplifier 2A6.

*c. Local Oscillator Circuits.* A 4.33 to 5.07 GHz local oscillator signal is developed within receiver frequency mixer stage 2A8 by mixing the 220 MHz output from 220 MHz frequency multiplier-osc 2A13 with the 4.55 to 4.85 GHz output from bandpass filter 2FL21. Frequency mixer currents generated within 2A8 and the 220 MHz output (multiplier-osc meter) of 2A13 are

selectable by a meter selector switch for monitoring on meter panel assembly 2A16A2. The 4.33 to 5.07 GHz output of 2A8 is applied to local oscillator bandpass filter 2FL6 which is set to pass a specific signal within the 4.36 to 5.07 GHz range and which is 70 MHz above or below the 4.4 to 5.0 GHz rf input signal. The 4.65 to 4.85 GHz input to 2A8 is produced by electrical frequency synthesizer 2A14 and amplifier-frequency multiplier 2A10. Electrical frequency synthesizer 2A14 generates a highly stable frequency in the range of 284.375 to 303.125 MHz which is adjustable in 6.260 kHz steps. The output level (synthesizer meter), alarm status (synthesizer monitor), and temperature conditions of 2A14 are monitored at the meter panel assembly. Amplifier-frequency multiplier 2A10 multiplies (times 16) the 284.376 to 303.125 MHz output of 2A14 up to the 4.55 to 4.85 GHz signal which is applied through bandpass filter 2FL1 to receiver frequency mixer stage 2A8.

*d. 70 MHz IF Amplifier Circuits.* The 70 MHz output of amplifier-mixer 2A7 (result of mixing the 4.4 to 5.0 GHz rf input signal with the 4.36 to 5.07 GHz local oscillator signal) is applied to 70 MHz bandpass filter 2A6. Filter 2A6, which has a center frequency of 70 MHz and a 5.0 MHz bandwidth, passes the 70 MHz if signal to 70 MHz intermediate frequency amplifier 2A5. The low level 70 MHz if signal is amplified in 2A5 for application to demodulator 2A4. The gain of 2A5 is controlled by an agc circuit within 2A5. The agc (agc metering) and 70 MHz if carrier (carrier (if) monitor and carrier (if) metering) levels are monitored, through alarm monitor 2A12 and meter selector switch, respectively, at the meter panel assembly. In addition, the agc output, which is proportional to the received rf signal level, is applied to Indicator, Antenna Alignment ID-1708/GRC.

*e. Demodulator Circuits.* The amplified 70 MHz if signal from 2A5 is applied to demodulator 2A4. A discriminator circuit in 2A4 converts the 70 MHz if signal to a base band signal comprised of pcm and orderwire signals. The baseband signal is then applied through 1.0 MHz/3.8 MHz lowpass filter 2A3 to af-rf amplifier 2A11. Af-rf amplifier 2A11 amplifies the signal which is sent to Transmitter, Radio T1054/GRC144. A level control is provided in 2A11 to adjust the signal output level. The amplified signal output (traffic monitor) is monitored at the meter panel assembly.

*f. Alarm Monitor Circuits.* Alarm monitor 2A12 controls the status indicators (TRAF, CARR IF, and SYNTH LOCK) on meter panel assembly 2A15A2. Monitor signals from 70 MHz intermediate frequency amplifier 2A5, af-rf amplifier 2A11 (and electrical frequency synthesizer 2A14 are applied to 2A12. For normal operating conditions, the alarm monitor causes the status indicators to light green. When an alarm condition occurs (alarm monitor detected an abnormal monitor signal), the circuits in alarm monitor 2A12 cause the associated status indicator to light red. Also, when any one of the alarm conditions occur, the alarm monitor activates the receiver summary alarm signal which is applied to Transmitter, Radio T-1054/GRC-144 and causes the ONTRL ALARM indicator on meter panel assembly 1A1A8 to light red and an audible alarm to sound.

*g. Metering Circuits.* Signals from various assemblies in the R-1467/GRC-144 are monitored at meter panel assembly 2A145A2. The metering circuits consist of a meter selector switch and a meter. A signal is monitored by setting the meter selector switch to the appropriate position. Meter calibration resistors are provided for certain meter indications. The meter circuit also provides a test position which allows component test lead voltage monitoring.

*h. Power Supply Circuits.* Power supply 2A1 produces regulated +28vdc, +15vdc, and -12vdc voltages required to operate the circuits and indicators in Receiver, Radio R-1467/GRC-144.

## **2-20. Functional Block Diagram Description of Receiver, Radio R-1467/GRC-144 RF Input and Mixer Circuits (fig. 5-19)**

*a. Preselector Bandpass Filter 2FL4.* Preselector bandpass filter 2FL4 is a four-pole (four-cavity) bandpass filter that is set to the specific incoming rf frequency in the 4.4 to 5.0 GHz band. The filter is directly at the input to the R-1467/GRC-144 and passes only the desired rf signal to tunnel diode amplifier 2A2. Within 2FL4, each of the four tuning cavities is ganged to a single frequency adjust control dial with direct readout of the frequency to which FL1A is set. The bandwidth of 2FL4 is nominally 25 MHz with a maximum insertion loss of 0.65 db.

*b. Tunnel Diode Amplifier 2A2.* Tunnel diode amplifier 2A2 amplifies the rf signal (4.4-5.0 GHz) from 2FL4 and provides a low noise figure. Tunnel diode amplifier 2A2 consists of a tunnel diode assembly and an oven assembly. The oven maintains the tunnel

diode assembly above a predetermined temperature. When the oven is on (heating), the TDA OVEN indicator (press-to-test) on meter panel assembly 2A15A2 lights white. Tunnel diode amplifier 2A2 provides  $21.5 \pm 1.5$  db gain in the frequency range 4.4 to 5.0 GHz at a noise figure of 4.55 db maximum. The output of 2A2 is applied to post selector .bandpass filter 2FL5.

*c. Post Selector Bandpass Filter 2FL5.* Post selector bandpass filter 2FL5 is a two-pole (two-cavity) bandpass filter that is set to the incoming rf frequency in the 4.4 to 5.0 GHz band. In addition to passing the desired rf signal, 2FL5 inhibits out-of-band and image frequency noise from tunnel diode amplifier 2A2 thereby maintaining the correct noise figure. Within 2FL5 tuning cavities are ganged to a single frequency adjust control with direct readout dial of the frequency to which 2FL5 is set. The bandwidth of 2FL5 is nominally 30 MHz with a maximum insertion loss of 0.85 db. The output of 2FL5 is applied to one input of amplifier-mixer 2A7.

*d. Amplifier-Mixer 2A7.* Amplifier-mixer 2A7 converts the rf input signal to the 70 MHz if signal. The conversion is made by mixing the rf input signal (4.4 to 5.0 GHz) with the local oscillator signal (4.3-5.07 GHz) which is 70 MHz above or below the rf input frequency. The output of amplifier-mixer 2A7 is applied to 70 MHz bandpass filter 2A6.

(1) Amplifier-mixer 2A7 consists of a crystal mixer 2A7Z1 and three preamplifier stages, Q1 through Q3. The rf input signal is applied to one input of crystal mixer 2A7Z1, and the local oscillator signal is applied to the second input.

(2) The rf input signal is mixed with the local oscillator signal, to produce the 70 MHz difference frequency. The 70 MHz if frequency produced by mixing the two signals appears at the output of crystal mixer 2A7Z1 and is amplified by preamplifier stages Q1 through Q3. The sum and difference signals from 2A7Z1 are also applied to negative and positive diode current monitor circuits for application to AMPILMIXER CURRENT 1 and AMPL-MIXER CURRENT 2 positions of the meter selector switch on meter panel assembly 2A15A2. Potentiometers 2A7R22 and 2A7R23 provide proper metering of negative and positive crystal currents from 2A7Z1.

(3) IF ADJ control in the input circuit of first preamplifier stage Q1 is adjusted to produce an if

bandpass response centered at 70 MHz by resonating with the sum of the crystal mixer output capacitance and preamplifier stage Q1 input capacitance. Preamplifier stage Q1 is a fixed tuned, wide band low noise amplifier stage which determines the noise figure of amplifier-mixer 2A7. Preamplifier stage Q2 is also a fixed tuned, wide band amplifier stage with adjustable gain, R12. Preamplifier stage Q3, also a fixed tuned wide band amplifier stage is capable of supplying large signal levels linearly at the output. Variable capacitor C22 sets the output impedance of amplifier-mixer 2A7 close to 75 ohms with a minimum reactive component.

## 2-21. Functional Block Diagram Description of Receiver Radio R-1467/G-144 Local Oscillator Circuits (fig. 5-19)

### a. Electrical Frequency Synthesizer 2A14.

Electrical frequency synthesizer 2A14 is identical to electrical frequency synthesizer 1A14 used in Transmitter, Radio T-14/GRC-144 (para 2-12 and 2-13). The 284.375 to 303.125 MHz, 20 milliwatt output of 2A14 is applied to amplifier-frequency multiplier 2A10. A detected sample of the output is applied to the SYNTH position of the meter selector switch on meter panel assembly 2A15A2. The SYNTH OVEN indicator (press-to-test) on meter panel assembly 2A15A2 lights white when the oven in 2A14 stabilizes at the correct temperature. In addition, a synthesizer monitor signal is applied to alarm-monitor 2A12. This signal indicates if the radio frequency oscillator and the standard radio frequency oscillator both in 2A14, are phase locked.

### b. Amplifier-Frequency Multiplier 2A10.

Amplifier-frequency multiplier 2A10 receives the 264.3715 to 303.125 MHz signal from 2A14 and multiplies (times 16) it up to 4.56 to 4.85 GHz. Amplifier-frequency multiplier 2A10 is comprised of a 300-600 MHz frequency doubler, 600 MHz amplifier, 600-4800 MHz frequency octupler, and a coaxial circulator. The 300-600 MHz frequency doubler T1, CR1 and CR2 doubles the 284.375 to 303.125 MHz input producing a 568.75 to 606.25 MHz signal. The 568.75 to 606.25 MHz signal is amplified by 600 MHz amplifier Q1-Q3 sufficiently to drive the 600-4800 MHz frequency octupler. The 600-4800 MHz frequency octupler utilizes varactor diode CR8 and octupler plates L13, L14 and L15 to accomplish a times 8 multiplication. The 4.55 to 4.85 GHz (50 milliwatts, nominal) output of the 600-4800 MHz frequency octupler is sent, through coaxial circulator 2A10HY1 and bandpass filter 2FL21, to receiver frequency mixer stage 2A8. Coaxial

circulator 2A10HY1 has a passband frequency range of 4.5 to 4.9 MHz and provides isolation between the 600-4800 MHz frequency octupler and receiver frequency mixer stage 2A8.

c. *Bandpass Filter 2FL21.* Bandpass filter 2FL21 passes the 4.55 to 4.85 GHz output from amplifier-frequency multiplier 2LA10 to receiver frequency mixer stage 2A8. All other frequencies are inhibited by bandpass filter 2FL21, thereby improving the spurious responses of the R1467/GRC-144. Bandpass filter 2FL21 has an impedance of 50 ohms (nominal) and causes a loss of 0.8 db (maximum) in the 4.56 to 4.85 GHz frequency range.

### d. 220 MHz Frequency Multiplier-Osc 2A13.

220 MHz frequency multiplier-osc 2A13 generates a 220 MHz (70 milliwatts, nominal) output signal which is applied to receiver frequency mixer stage 2A8. The 220 MHz frequency multiplier-osc 2A13 is comprised of 110 MHz rf oscillator 2A13Y1 and amplifier-frequency multiplier 2A13A1. The 110 MHz rf oscillator is a crystal oscillator which produces a 110 MHz ( $\pm 1500$  Hz) output frequency at a power level of 15 milliwatts, nominal. The 110 MHz output signal is applied to input amplifier Q1 of 2A13A1 where it is amplified and applied to frequency doubler Q2 and Q3. Input amplifier Q1 also provides isolation for frequency doubler Q2 and Q3. Frequency doubler Q2 and Q3 multiply the 110 MHz input by two producing an output signal of 220 MHz. The 220 MHz output signal is then applied to output amplifier Q4 which amplifies the low level 220 MHz signal for application to receiver frequency mixer stage 2A8. The 220 MHz output signal from output amplifier Q4 is also applied to metering circuit CR3 where it is detected for application to the MULT OSC position of the meter selector switch on meter panel assembly 2A15A2. Variable resistor 2A15A2R6, mounted on the rear of meter panel assembly 2A15A2, is used to calibrate the MULT OSC meter indication.

### e. Receiver Frequency Mixer Stage 2A8.

Receiver frequency mixer stage 2A8 produces the 4.38 to 5.07 GHz local oscillator signal by mixing the 220 MHz signal from 2A13 with the 4.556 to 4.85 GHz signal from 2FL21. Receiver frequency mixer stage 2A8 consists of 220 MHz bandpass filter 2A8FL1, crystal mixer 2A8Z1, and coaxial circulator 2A8HY1. The 4.56 to 4.86 GHz

signal from bandpass filter 2FL21 is applied to one input of crystal mixer 2A8Z1 and the 220 MHz signal from 2A13 is applied to the input of 220 MHz bandpass filter 2A8FL1. The output of 2A8FL1 is applied to the other input of crystal mixer 2A8Z1. The two signals are mixed producing the 4.33 to 5.07 GHz signal which is 170 MHz away from the 4.4 to 5.0 GHz rf input frequency. The 4.33 to 5.07 GHz output is applied through coaxial circulator 2A8HY1 to local oscillator bandpass filter 2FL6 where the correct frequency (f below) is selected. Coaxial circulator 2A8HY1 has a passband of 4.33 to 5.07 GHz and provides isolation between crystal mixer 2A8Z1 and local oscillator bandpass filter 2FL6. The crystal current outputs of crystal mixer 2A8Z1 are applied to the meter selector switch through crystal current metering circuit to the **FREQ MIXER CURRENT 1** and **FREQ MIXER CURRENT 2** positions of meter selector switch mounted on meter panel assembly 2A15A2 and variable resistors 2A15A2R3 and 2A16A2R4. Variable resistors 2A15A2R3 and 2A16A2R4, mounted on the rear of meter panel assembly 2A15A2, are used to calibrate the **FREQ MIXER CURRENT 1** and the **FREQ MIXER CURRENT 2** meter indications.

*f. Local Oscillator Bandpass Filter 2FL6.*

Local oscillator bandpass filter 2FL6 is a four-pole (four-cavity) rf bandpass filter which passes only the desired translated frequency from receiver frequency mixer stage 2A8. Each of the four tuning cavities is ganged to a single frequency adjust control dial with direct readout of the incoming rf frequency (frequency to which the receiver is set). However, the actual bandpass of 2FL6 is separated by  $\pm 70$  MHz from the incoming rf frequency.

(1) For example, if the dial on 2FL6 is set to 4500 MHz, 2FL6 is tuned to the difference frequency component (4430 MHz) which is 70 MHz below the incoming rf frequency (4500 MHz - 70 MHz = 4430 MHz). The 4480 MHz signal is passed by 2FL6 to amplifier-mixer 2A7 (para 2-20d).

(2) If the dial on 2FL6 is set to 4800 MHz, 2FL6 is tuned to the sum frequency component (4870 MHz) which is 70 MHz above the incoming rf frequency (4870 MHz - 4800 MHz = 70 MHz). The 4870 MHz signal is passed by 2FL6 to amplifier-mixer 2A7 (para 2-20d).

## 2-22. Functional Block Diagram Description of Receiver, Radio R-1467/GK-144 70 MHz IF Amplifier Circuits (fig. 5-19)

a. *70 MHz Bandpass Filter 2A6.* The 70 MHz bandpass filter 2A6 is a five pole gauss filter, which in a bandpass has a center frequency of 70 MHz and a 5.0 MHz bandwidth. The insertion loss at 70 MHz ( $\pm 0.5$  kHz) is 2.0 db maximum. The 70 MHz signal from amplifier-mixer 2A7 is passed through 2A6 to 70 MHz if amplifier 2A5.

b. *70 MHz IF Amplifier 2A5.* 70 MHz if amplifier 2A5 is comprised of amplifiers, agc, metering, and if monitor circuits.

(1) The 70 MHz amplifier circuits amplifies the low level 70 MHz if input signal for application to demodulator 2A4. The IF GAIN control, at the input to amplifier stage Q1, is used to set the 70 MHz if gain. The 70 MHz if signal is amplified by cascaded amplifier stages Q1 through Q5 and attenuated by diode attenuator circuits CR1 through CR4. The amplified 70 MHz if signal from amplifier stage Q5 is then fed to buffer amplifier Q6. The overall gain of cascaded amplifier stages Q1 through Q5 and diode attenuator circuits CR1 through CR4 is controlled by the agc circuit. Buffer amplifier Q6 provides an impedance match between amplifier stage Q5 and output amplifier Q7. Output amplifier Q7 provides a linear power output level of the 70 MHz if signal which is sent to the age circuit and to demodulator 2A4.

(2) The agc circuit controls the overall gain of amplifier stages Q1 through Q5, and maintains each if amplifier output at the same if level ratio as at the if amplifier input. The agc circuit consists of peak detector CR5, CR6, AGC SEL switch S1, dc amplifier Q8, Q9, and emitter follower Q10. TAGC SEL switch S1 is used to select the age mode and connects the proper inputs to the age circuit. When AGC SEL switch S1 is in the TEST position, the age circuit is disabled and maximum if gain is obtained. In the DIV OFF position, the dc output of the peak detector CR5 and CR6 is applied to meter circuit R32 and R37 and to dc amplifier Q8 and Q9. The DIV ON position is not used because the R-1467/GRG 144 is a single channel receiver. Dc amplifier Q8 and Q9 amplifies the dc voltage at its input to control the level of the dc gain voltage applied to diode attenuator circuits CR1 through CR4. The output of the dc amplifier is applied to emitter follower Q10 through AGC GAIN potentiometer which sets the dc gain of the age circuit.

The output of emitter follower Q10 is a dc voltage which is inversely proportional to the age input to the de amplifier. The age input dc voltage increases as the level of the 70 MHz if signal increases. This causes the agc dc output to decrease, proportionally, increasing the attenuation of diode attenuator circuits CR1 through CR4 and decreasing the overall gain of 70 MHz if amplifier 2A5. The agc output of emitter follower Q10 is also applied to Indicator, Antenna Alignment ID-1708/GRC and agc metering circuits and to the if carrier monitor circuit.

(3) The metering circuits provide agc signal level outputs to the meter selector switch on meter panel assembly 2A165A2 and to Indicator, Antenna Alignment ID-1708/GRC. The agc output of peak detector CR5, CR6 is applied to the CARRIER (IF) position of meter selector switch on meter panel assembly 2A15A2 through meter circuit R32 and R37. The agc output of emitter follower Q10 is applied to the AGC position of the meter selector switch (agc meter) and to Indicator, Antenna Alignment ID-1708/GRC through meter circuit R84, R51, and R52. The reference (return lines) for the age metering and ant align ind outputs are applied through meter adjust circuit R46 and R48. The METER ZERO control is used to set the meter on 2A165A2 to electrical zero. To zero adjust the meter, meter selector switch 2A15A2S1 must be set to the AGC position and the AGC SEL switch on 2A5 must be set to the TEST position.

(4) The age output of emitter follower Q10 is also applied through monitor circuit R55 and R56 to alarm monitor 2A12. The reference for the carrier (if) monitor signal is applied to alarm monitor 2A12 through carrier level alarm adjust circuit R60. Alarm monitor 2A12 controls the CARR IF status indicator on meter panel assembly 2A15A2. If the carrier (if) monitor signal is below a predetermined level, the CARR IF indicator lights green (normal indication). If the carrier (if) monitor signal level rises above the predetermined level, the CARR IF indicator lights red (alarm condition). The ALM SET control on 2A5 is used to set the level at which the alarm condition occurs.

## **2-23. Functional Block Diagram Description of Receiver, Radio R-1467/GRC-144 Demodulator and Output Amplifier Circuits (fig. 5-19)**

a. *Demodulator 2A4.* Demodulator 2A4 receives the 70 MHz if signal from 70 MHz if amplifier 2A5 and converts the frequency deviations in the 70 MHz if signal into a composite pcm and orderwire signal. The demodulator consists of input amplifier Q1,

limiter stages Q2 through Q5, discriminator driver stages Q6 and Q7, frequency discriminator T1, CR3 and CR4, and video output amplifier Q8 and Q9.

(1) The 70 MHz if signal from 2A5 is applied through input amplifier Q1 (emitter follower) to the first limiter stage Q2. The emitter follower matches the input impedance of the first limiter stage with the output impedance of 2A5.

(2) Four limiter stages, Q2 through Q4, remove amplitude variations in the 70 MHz signal. Each limiter stage is operated as an overdriven common base amplifier to clip the positive and negative peaks of the 70 MHz if signal. A LIM TUNING control is provided for tuning each limiter stage. The output of the fourth limiter stage is applied to discriminator driver stages Q6 and Q7.

(3) Discriminator driver stages Q6 and Q7 consist of emitter follower Q6 and common base amplifier Q7. Emitter follower Q6 is used to match the output impedance of fourth limiter stage Q5 to the input impedance of common base amplifier Q7. The output of discriminator driver stages Q6 and Q7 is applied to frequency discriminator T1, CR3 and CR4.

(4) Frequency discriminator T1, CR8 and CR4 detects the frequency variations in the 70 MHz if signal and converts the variations in the composite pcm and orderwire signal. The DISCR PRIM control is used to tune the primary winding of frequency discriminator transformer T1. The DISCR SEC control in the secondary of the frequency discriminator transformer T1 is used to set the discriminator crossover frequency. The composite pcm and orderwire output is applied to 1.0 MHz low pass filter 2A3 through video output amplifier Q8 and Q9. Video output amplifier Q8 and Q9 amplifies the signals and isolates the frequency discriminator from 2A3.

b. *Low Pass Filter OAS.* Low pass filter 2AS passes the composite pcm and orderwire signal to af-rf amplifier 2A11. In the synchronous mode, the 1.0 MHz low pass filter (684448) is used. In the asynchronous mode, the 3.8 MHz low pass filter (684449) is used. Both filters have a source impedance of 50 ohms and a load impedance of 150 ohms. The insertion loss of the 1.0 MHz filter is 0.5 dB maximum at 20 kHz. The insertion loss of the 8.8 MHz filter is 0.3 dB maximum at 20 kHz.

c. *AF-RF Amplifier 2A11.* Af-rf amplifier

2A11 consists of video amplifier stages Q1 and Q2 and emitter follower Q3. The composite pcm and orderwire signal is applied to video amplifier stages Q1 and Q2 through the TRAFFIC LEVEL ADJ control which is adjusted to provide a 1.0 volt peak-to-peak output. The composite pcm and orderwire signal is amplified by video amplifier stages Q1 and Q2 and applied to the output through emitter follower Q3. Emitter follower Q3 provides an impedance match between video amplifier Q2 and the output and also provides negative feedback to video amplifier stage Q1. The amount of negative feedback determines the overall gain and bandwidth of af-rf amplifier 2A11. The pcm and orderwire (receiver traffic) output of 2A11 is applied to Transmitter, Radio T-1054(P)/GRC-144(V) and to alarm monitor 2A12 which monitors the level of the receiver traffic output signal.

**2-23.1. Functional Block Diagram Description of Receiver, Radio R-1467(P)/GRC-144(V) Demodulator and Output Amplifier Circuits (fig. 5-19.1)**

a. Demodulator 2A4. Demodulator 2A4 receives the 70 MHz IF signal from IF amplifier 2A5 and demodulates the signal to provide the composite data/orderwire ,baseband (video) signal. Input amplifier stages Q1/Q2 provide impedance matching and frequency response control. Limiter stages Q3 through Q6 provide amplification with amplitude limiting. A Crosby-type discriminator (CR8/CR9) converts the frequency variations of the frequency modulated IF signal into the video signal. Video amplifier stages Q9 and Q10 amplify the video signal and couple the output signal through emitter follower Q11 to low pass filter 2A3.

b. Low Pass Filter 2A3. The filter assembly used for 2A3 varies according to the data rate as shown in figure 5-19.1.

c. AF-RF Amplifier 2A11. Refer to paragraph 2-23c.

## 2-24. Alarm-Monitor 2A12 Block Diagram Description (fig. 5-20)

a. Alarm-monitor 2A12 receives the traffic, carrier (if), and synthesizer monitor signals and controls associated alarm indicators on meter panel assembly 2A15A2. Depending upon the signal level received, the associated indicator lights either green (normal indication) or red (alarm indication). Alarm-monitor 2A12 also contains a summary alarm circuit which is enabled when any one of the alarm condition occur. The traffic monitor signal is received from af-rf amplifier 2A4 and indicates the composite pcm and orderwire signal level at the output of the R-1467(P)/GRC-144(V). The synthesizer monitor signal is received from electrical frequency synthesizer 2A14 and indicates if the signals from radio frequency oscillator 2A14A1 and standard radio frequency oscillator 2A14A7 are phase locked. The carrier (if) monitor signal and associated reference signal are received from 70 MHz intermediate frequency amplifier 2A5 and indicate if the 70 MHz if carrier signal in 2A5 is above a predetermined level.

b. The TRAF, SYNTH LOCK, and CARR IF indicators on meter panel assembly 2A15A2 are controlled by Schmitt trigger circuits in alarm monitor 2A12. Each Schmitt trigger circuit causes an associated indicator to light green (normal indication) or red (alarm indication). The input signals to the alarm monitor control the operation of an associated Schmitt trigger circuit.

(1) The traffic monitor signal is received from af-rf amplifier 2A11 and is applied to operational amplifier (integrated circuit) AR1 through an attenuator circuit. The operational amplifier output is detected by detector CR1 and CR2 and applied as a traffic meter signal to the TRAFFIC position of the meter selector switch on 2A15A2 through potentiometer R8. The same output is also applied to Schmitt trigger circuit Q5 and Q6 through emitter follower Q1. If the traffic monitor signal exceeds a predetermined level, the dc voltage developed by detector CR1 and CR2 will cause Q5 to turn on causing Q6 to turn off and Q7 to turn on. With Q7 turned on, a low impedance path to ground is provided for the traffic normal indicator lamp, and the TRAF indicator lights green. Since Q6 is turned off, a high impedance path to ground is provided for the traffic alarm indicator lamp (red) causing it to remain off. When the input traffic monitor signal falls below the

predetermined level, the dc voltage applied to the base of Q5 is not sufficient to keep Q5 conducting. With Q5 turned off, Q6 turns on and Q7 turns off. For this condition, a high impedance path to ground is applied to the traffic normal indicator lamp and a low impedance path to ground is applied to the traffic alarm indicator lamp. Consequently, the TRAF indication changes from green to red. Also with Q7 turned off, the Q7 output dc voltage is high enabling the OR gate which causes O23 to turn on. With Q23 turned on, a receiver summary alarm indication is applied to r-1054(P)/GRC-144(V).

(2) The synthesizer monitor signal is received from electrical frequency synthesizer 2A14 and is applied directly to Schmitt trigger circuit Q14 and Q15. Circuit operation is identical to that described above for the traffic monitor circuit. If the synthesizer signal exceeds a predetermined dc level, the SYNTH LOCK indicator on 2A15A2 lights green (normal indication). If the synthesizer monitor signal is below the predetermined level, the associated indicator lights red (alarm indication) and, in addition, the summary alarm circuit is enabled.

(3) The carrier (if) monitor signal is received from 70 MHz intermediate frequency amplifier 2A5 along with a predetermined reference signal level. The two signals are applied to differential amplifier Q3 and Q4. The carrier (if) monitor signal is derived from the agc signal developed in 2A5 (para 2-22b(2)). As the 70 MHz if input level to 2A5 increases, the age signal decreases; consequently, the carrier (if) monitor input to the alarm monitor decreases. With the carrier (if) monitor input at a lower level than the reference input to differential amplifier Q3 and Q4, the output of Q4 is high. The high output is applied through potentiometer R35 to Schmitt trigger Q17 and Q18. Potentiometer R35 is used to set the input level to Schmitt trigger Q17 and Q18. The high output from differential amplifier Q3 and Q4 causes Q17 to turn on, which in turn causes Q18 to turn off and Q19 to turn on. With Q19 turned on, the CARR IF indicator on meter panel assembly 2A15A2 lights green (normal indication). If the carrier (if) monitor signal input to differential amplifier Q3 and Q4 is at a higher level than the predetermined reference input, Q17 turns off, Q18 turns on, and Q19 turns off causing the CARR IF indicator to change from green to red. The red



CARR IF indication informs the operator that the 70 MHz if carrier is at a low level or is not present. Also, for this condition, the receiver summary alarm circuit is activated.

(4) The summary alarm circuit is comprised of diode OR gate CR12, CR15 and CR16 and transistor Q23. Each of the normal outputs is connected to the OR gate. For normal operation, transistor Q23 is off (nonconducting). When any one of the alarm conditions occur, the OR gate switches Q23 turn on (conducting state) causing a receiver summary alarm condition.

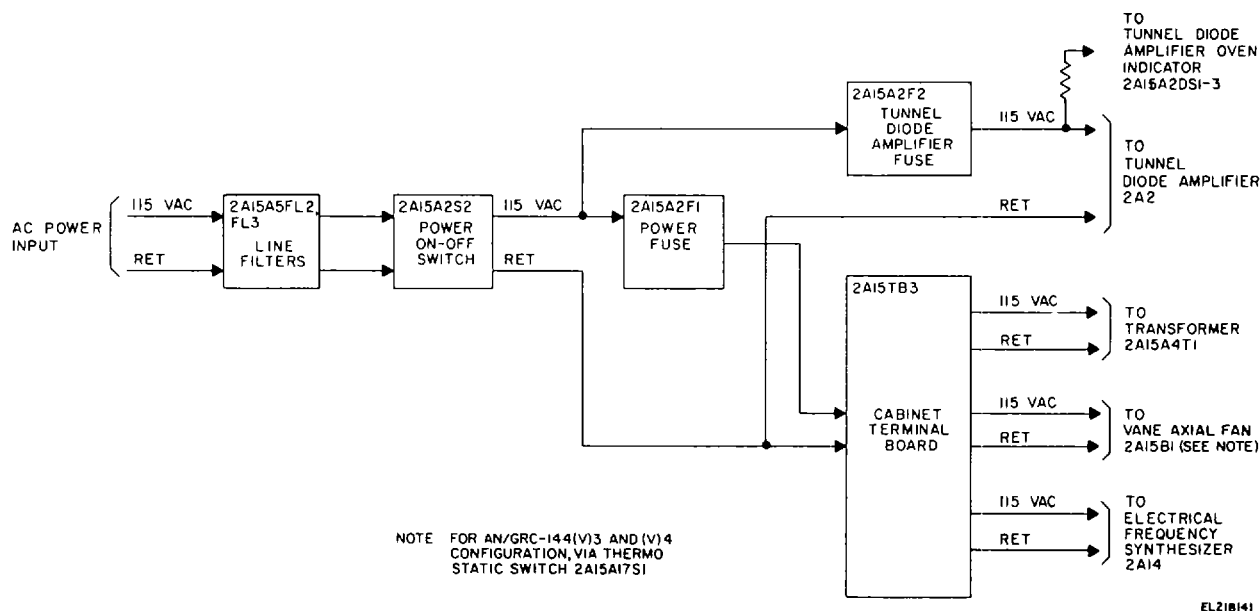
**2-25. Receiver, Radio R-1467(P)/GRC-144(V) Primary Power Distribution (fig. 2-7)**

The 115 vac primary power is applied to Receiver, Radio R-1467(P)/GRC-144(V) through AC POWER INPUT connector 2A15A5J5. The 115 vac input passes through line filters 2A15A5FL2 and FL3 to POWER ON-OFF switch 2A15-A2S2 on meter panel assembly 2A15A2. When the POWER ON-OFF switch is set to ON, 115 vac passes through the fuse 2A15A2F1 to

terminal board 2A15TB3 and through the tunnel diode amplifier fuse (2A15A2F2) to tunnel diode amplifier 2A2 and to tunnel diode oven amplifier Indicator 2A15A2DS13. Terminal board 2A15TB3 distributes 115 vac primary power to power transformer 2A15A4T1, vane axial fan 2A15B1, and electrical frequency synthesizer 2A14. Refer to the Receiver, Radio R-1467(P)/GRC-144(V) interconnecting diagram (fig. 5-21) for point-to-point primary power connections. For the AN/GFC-144(V) 3 and 4 configurations, 115 vac passes to fan 2A1581 through thermostatic switch 1A15A17S1.

**2-26. Receiver, Radio R-1467(P)/GRC-144(V) DC Power Distribution (fig. 2-8)**

The 115 vac input from 2A15TB3 is applied to power transformer 2A15A4T1 where it is transformed into four ac outputs: 29 vac (w), 19 vac (x), 18 vac (y), and 30 vac (z). Each output is applied to a voltage regulator in power supply 2A1. Three 15/28v voltage regulators and one 12v voltage regulator are utilized. A typical voltage regulator is described in paragraph 2-18. The voltage regulators provide four regulated dc voltage outputs:



**Figure 2-7. Receiver, Radio R-1467(P)/GRC-144(V) and R-1467(P) A/GRC-144(V), Primary Power Distribution**

+28 vdc (w), +28. vdc (z), +15 vdc (x), -12 vdc (y), and four associated dc returns. The voltages are distributed to the components through plate assembly terminal board 2A16TB1. The +28 vdc (z) voltage is also used for the status and oven indicators. Refer to the

Receiver, Radio R-11467/GRC-144 interconnecting diagram (fig. 5-21) and power supply 2A1 interconnecting diagram (fig. 5-22) for point-to-point dc voltage connections.

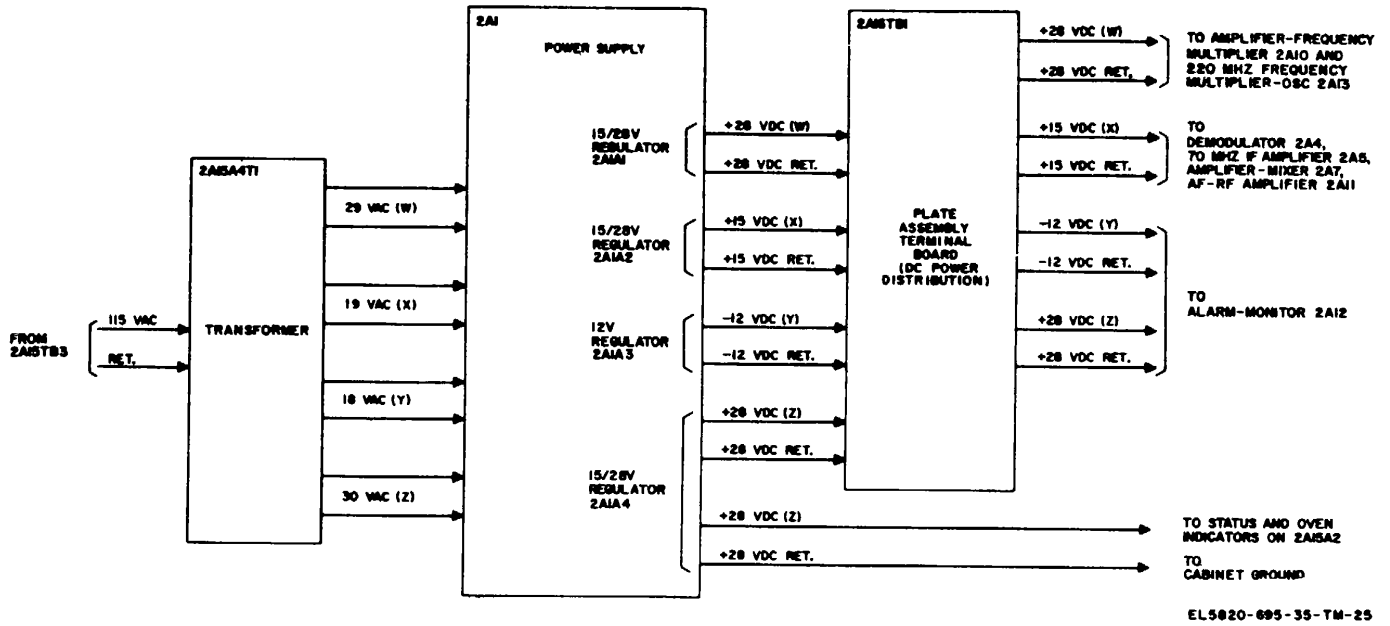


Figure 2-8. Receiver, Radio R-147/GRC-14, dc power distribution.

## Section II. FUNCTIONING OF TRANSMITTER, RADIO T-1054(P)/GRC-144(V) AND T-1054(P)/GRC-144(V) CIRCUITS

### 2-27. General

This section covers the functioning of circuits used in the T-1054(P)/GRC-144(V) and T-1054(P)/GRC-144(V). The coverage is presented in sequential reference designation order and is at the schematic diagram level. Circuit functioning and schematic diagrams are not provided for the non-repairable assemblies (i.e. coaxial circulator 1HY1, directional coupler 1DC1, etc.). Circuit descriptions for cabinet mounted components (metering circuits, indicators, radio patch panel, etc.) and the nonrepairable assemblies are covered in the block diagram description for the T-1054(P)/GRC-144(V) (para 2-1 through 2-18). All cabinet mounted circuits and all interconnections in the T-1054(P)/GRC-144(V) are shown in figure 5-15. (The T-1054(P)/GRC-144(V) circuits are shown in figure 5-15.1). All references to the T-1054(P)/GRC-144(V) also apply to the T-1054(P)/GRC-144(V) unless otherwise specified.

### 2-28. Power Supply 1A1 Circuit Functioning

Power supply 1A1 contains the voltage regulators (1A1A1 through 1A1A4 and 1A1A6 through 1A1A12) which provide the dc supply and control voltages required in the T-1054/ GRC-144. Power supply chassis 1A1A13 provides: (1) a connector for each voltage regulator, (2) an ac fuse at the input of each voltage regulator, and (3) a failure lamp and a test point at the output of each voltage regulator. Figure 5-17, power supply 1A1 interconnecting diagram, shows the chassis mounted components and the voltage regulator connections. The circuit descriptions for the voltage regulators are provided in the following subparagraphs.

a. 5/6v Voltage Regulator 1A1A1 through 1A1A4 (fig. 2-9). The rectified dc voltage from bridge rectifier CR1 through CR4 is filtered by capacitor C1 and applied to the collector of series regulator Q3. The series regulator, controlled by differential amplifier Q7, Q8, in conjunction with amplifiers Q4, Q5, Q6 and driver amplifier Q2, introduces a voltage drop which maintains voltage regulation at the emitter output. An overvoltage condition at the voltage regulator output terminal is

sensed by Q9, which triggers Q1. When triggered, Q1 short circuits the rectifier output causing the fuse in the ac input supply to blow (this circuit is referred to as a crowbar configuration).

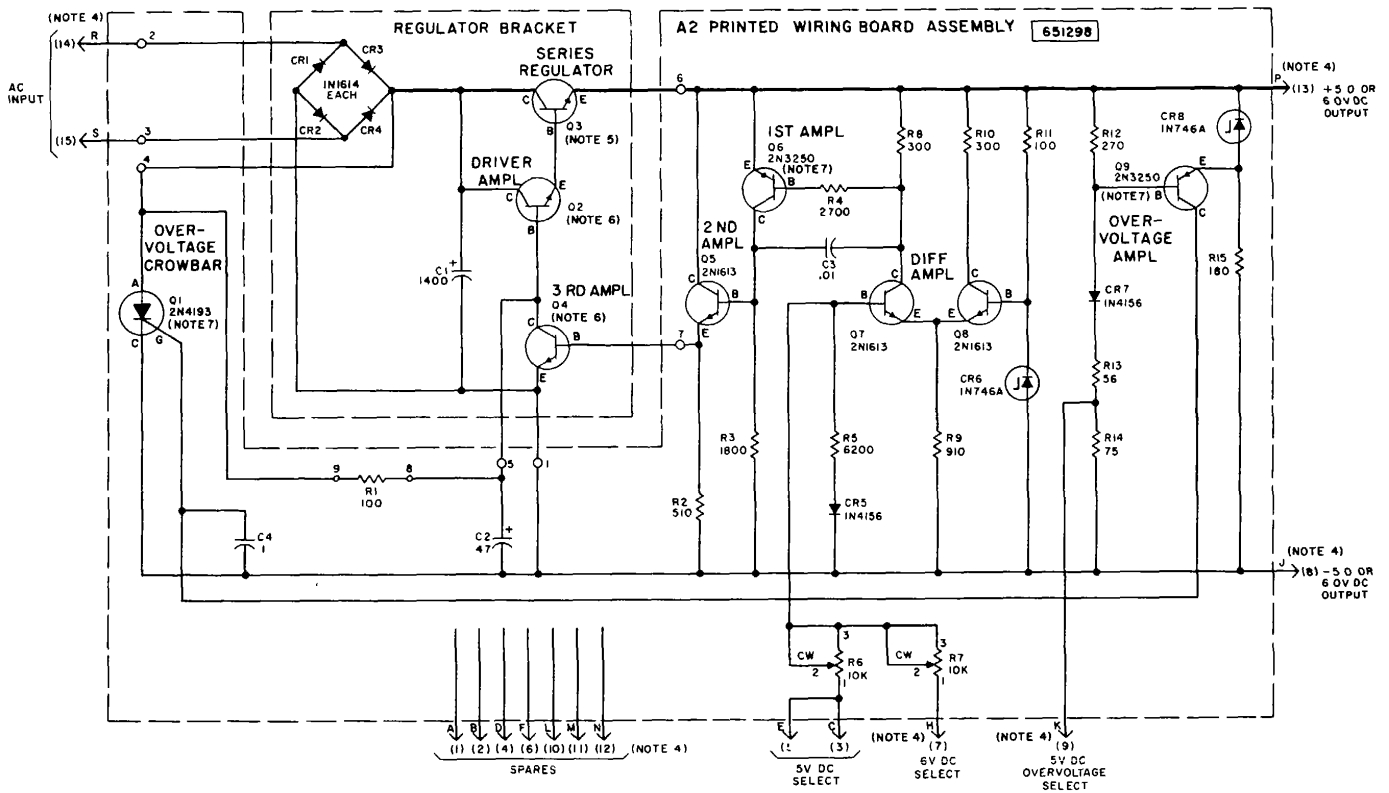
(1) The base of differential amplifier stage Q8 is clamped to 3.3 volts above ground by reference diode CR6 and diode current limiter R11. The voltage at the base of Q7 is determined by a voltage divider consisting of R5 and either R6 or R7. Variable resistor R6 or R7 is connected through the chassis connector jumper to the power supply positive output lead (pin 13). Resistor R6 is used to adjust the output to 5 vdc and resistor R7 is used to adjust the output to 6 vdc. Emitter resistor R9 maintains a constant emitter current which is determined by the reference voltage. Since R9 is the common emitter resistor to both stages Q7 and Q8, changes in the operating conditions in one stage interact with the other stage. An increase of the Q7 base voltage above 3.3 volts causes the transistor to draw higher collector current. An increase in Q7 collector current causes an equal decrease in Q8 collector current. As a result, the voltage across R8 increases. The voltage developed across R8 is applied to the base of Q6 through base current limiting resistor R4. Collector current in Q6 increases raising the voltage across R3 and causing Q5 to conduct more. Due to the increase in current, the voltage across R2 rises and causes Q4 to conduct more. Since the current source for Q4 is through R1 and R16 the voltage at terminal 5 will decrease lowering the voltage at the base of Q2 and thereby decreasing its collector current. Transistor Q2 supplies base current to series regulator Q3, therefore, transistor drive is reduced which increases its collector to emitter voltage drop. Thus, the voltage regulator output voltage is restored to the desired regulated level.

(2) An overvoltage condition is sensed by Q9. The emitter of Q9 is clamped 3.3 volts below the output Voltage by reference diode CR8; resistor R15 limits the

current through CR8. The base voltage for Q9 is derived from the voltage divider consisting of R12, R13 and R14. When the voltage regulator is configured to operate at 5 volts, resistor R14 is short circuited by connecting pin 9 to the negative output lead pin 8. When the output is in regulation, the voltage at the base of Q9 is approximately 3.0 volts below the regulator output voltage. The emitter is clamped at 3.3 volts

below the output voltage; the transistor is turned off. When the output voltage rises above the regulated level, the base of Q9 becomes negative with respect to its emitter and the transistor conducts. This gates on silicon-controlled rectifier Q1 and short circuits the rectifier output voltage. The short circuit current is limited by the transformer winding resistance.

**Change 6 2-55**



- NOTES
- 1 UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS
  - 2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, PREFIX REFERENCE DESIGNATIONS WITH 1A1A1, 1A1A2, 1A1A3, OR 1A1A4
  - 3    INDICATES MARKING ON EQUIPMENT
  - 4 TERMINAL DESIGNATIONS IN ( ) ARE THOSE APPEARING ON MATING CONNECTOR OF POWER SUPPLY CHASSIS
  - 5 CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM-B-650729
  - 6 CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM-B-650730
  - 7 ON CONTRACT DAAB05-72-C-5507, TRANSISTOR TYPE 2N4185 REPLACES 2N4193, AND TYPE 2N3250A REPLACES 2N3250

EL 21 8001

Figure 2-9. 5/6v voltage regulator 1A1A1 through 1A1A4, schematic diagram.

(3) Oscillations and noise in the high gain feedback regulator are prevented by C2 and C3. Capacitor C2 shunts any disturbances at Q2 base to ground. Capacitor C3 supplies negative feedback to the base of Q6 to prevent oscillations. Capacitor C4 suppresses any noise which otherwise could trigger Q1 during normal operating conditions. Diodes CR5 and CR7 are temperature compensating diodes in the base circuits of Q7 and Q9.

b. *12v Voltage Regulator 1A1A6 through 1A1A9* (fig. 2-10). This circuit functions the same as the 6/6v voltage regulator previously described in a above. The difference between the circuits is that 6.2-volt zener diode references are used (CR5 and CR6) in place of the 3.3-volt type (CR6 and CR8) used in the 5/6v voltage regulator. Only one potentiometer (R4) is provided in the voltage divider path (R4 and R6) and the temperature compensating diodes in the base circuits of Q7 and Q9 are not used. Also, capacitor-resistor network Z1 is used in the base circuit of Q6 to eliminate possible oscillations under a low load condition. An identical 12v voltage regulator is used in position 2A1A3 of Receiver, Radio R-1467/GRC-1144.

c. *15/28v Voltage Regulator 1A1A10 through 1A1A12* (fig. 2-11). This circuit functions the same as the 5/6v voltage regulator previously described in a above. The difference between the circuits is that 6.2-volt zener diode references are used (CR-5 and CR6) in place of the 3.3-volt type (CR6 and CR8) used in the 5/6v voltage regulator. Also, certain circuit resistance values are different to accommodate the higher voltages and the temperature compensating diodes in the base circuits of Q7 and Q9 are not used. In addition, resistor R16 is required to limit the crowbar current and capacitor-resistor network Z1 is used in the base circuit of Q6 to eliminate possible oscillations under a low load condition. Identical 15/28v voltage regulators are used in positions 2A1A1, 2A1A2, and 2A1A4 of Receiver, Radio R-1467/GRC-144.

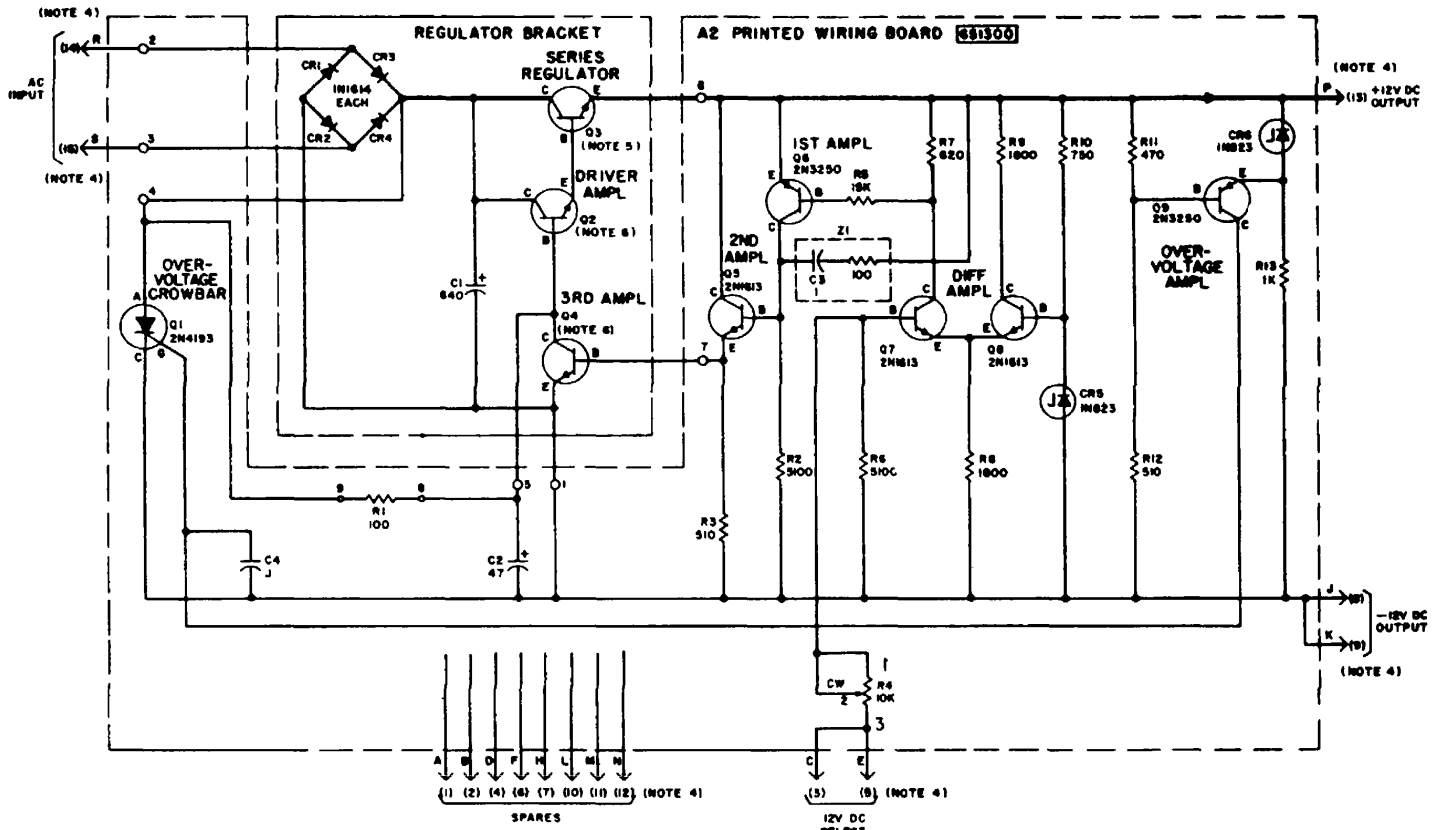
## **2-29. 100 MHz Radio Frequency Oscillator 1A2 Circuit Functioning (fig. 5-23)**

a. The 100 MHz radio frequency oscillator 1A2, functionally part of the radio test set, produces a precise 100 MHz signal, which is mixed with the output signal of the T-1054/GRC-144 to produce a signal offset by 100 MHz from the rf output frequency. The signal is used in aligning, testing, and troubleshooting the R-1467/GRC-144. The basic oscillator consists of

transistor Q1, crystal Y1, and tank circuit L3, C7, C10. Crystal Y1 operates in series resonance on the fifth overtone. Transistor bias is provided by resistors R3, R4 and R5. Resistor R5 is also in the oscillator's feedback path. Inductor L4 tunes out stray capacitance in the crystal unit. Capacitor C6 provides rf bypass. Dc power is applied through switch S1, and two filter sections (L1, C1, C3 and L2, C4, C5). The switch also controls the RADIO TEST SET lamp on meter panel assembly 1A15A8 and on-off lamp DS1 on the front panel of 1A2 through current dropping resistor R2.

b. When voltage is applied, the initial transient causes oscillations to start. Crystal oscillations are fed through C21 and R5 to the emitter of Q1, amplified in the transistor, and applied to the tank circuit. The tank circuit, closely tuned to the crystal frequency, resonates and feeds a reinforcing signal through C8. The signal builds up in the loop until the transistor gain has decreased to unity, at which point a sustained level is maintained. Small changes are made in operating frequency by means of variable capacitor C10 in the tank circuit. When the tank circuit is tuned to resonate above the natural frequency of the crystal, the feedback signal to the crystal leads the crystal signal. This causes the crystal to oscillate at a higher frequency and restores a zero phase condition. Since the crystal Q is very high, compared to that of the tank, the change in crystal frequency required to restore zero phase is very small relative to the change in resonant frequency in the tank circuit. The oscillator output is taken off at the upper tap of L3, through coupling capacitor C9. The signal is fed to a power splitter (R10 through R14) which also isolates the oscillator from the load. Each output is coupled by blocking capacitors C13 and C14 to the output cables W1 and W2. These cables are connected to balanced mixer unit 1Z1. The blocking capacitors prevent diode currents in the mixer from feeding back to the oscillator stage.

c. Several metering circuits are provided. A diode detector circuit, consisting of CR1, R8, R0 is capacitively coupled by C11 to the variable arm of R7 (LEVEL ADJ). This circuit produces a dc level proportional to the signal level. The dc level (osc output level) is applied to the meter selector switch on the radio test set panel. Potentiometer R9 (cal adj 4th-5th ech only) is used to adjust the meter deflection and capacitor C12 is an rf bypass. Circuits for metering the

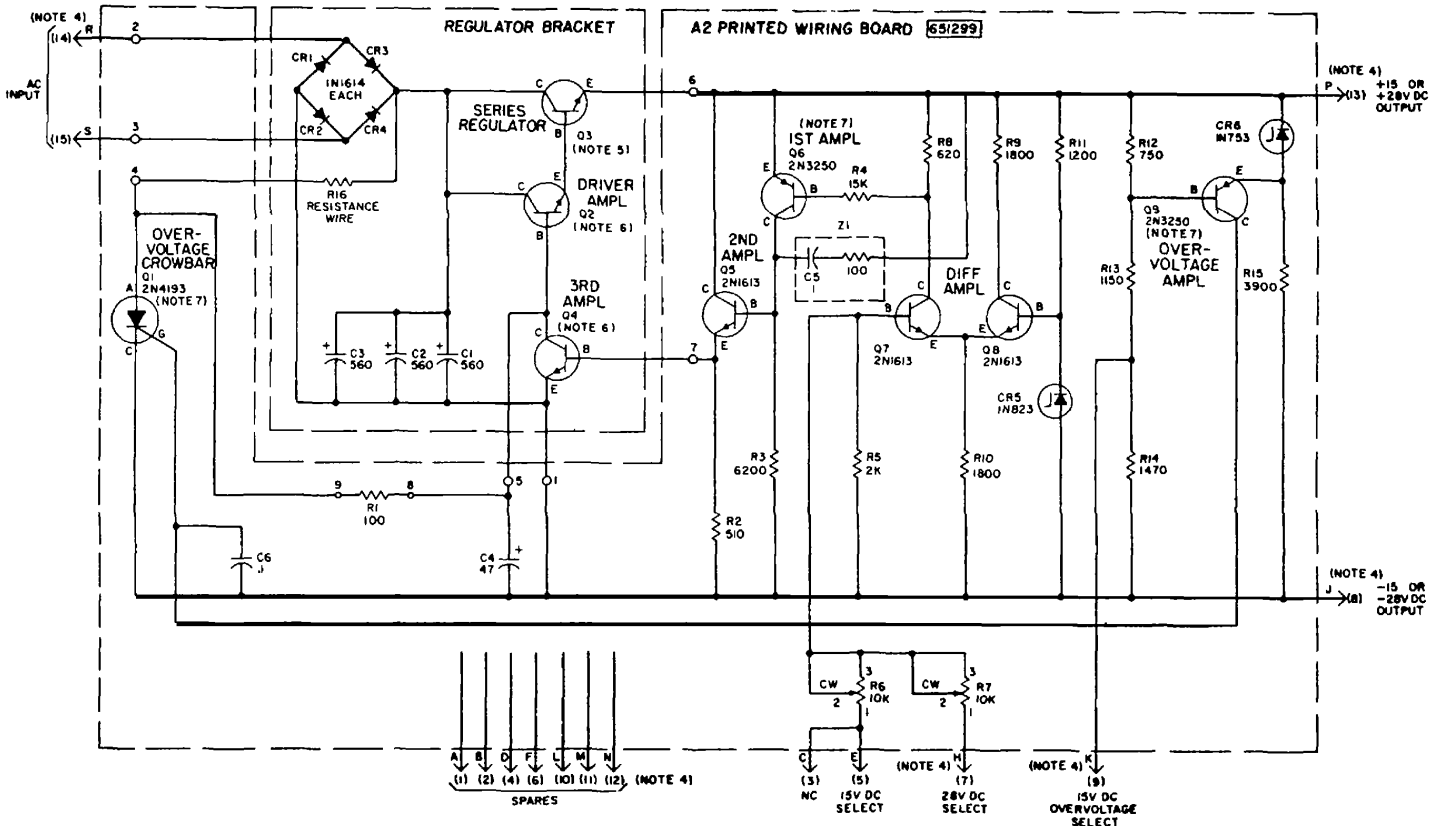


- NOTES:
- 1 UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS. CAPACITANCES ARE IN MICROFARADS.
  - 2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX REFERENCE DESIGNATIONS WITH IA1AS, IA1AT, IA1AB, IA1AD OR ZA1A3.
  - 3   INDICATES MARKING ON EQUIPMENT.
  - 4 TERMINAL DESIGNATIONS IN ( ) ARE THOSE APPEARING ON MATING CONNECTOR OF POWER SUPPLY CHASSIS.
  - 5 CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM-B-650723.
  - 6 CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM-B-650730.

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Figure 2-10. 12v voltage regulator 1A1A6 through 1A1A9 through 2A1A3, schematic diagram.





- NOTES**
- 1 UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS CAPACITANCES ARE IN MICROFARADS.
  - 2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; PREFIX REFERENCE DESIGNATIONS WITH IA1A10 THROUGH IA1A12 OR 2A1A1, 2A1A2 OR 2A1A4
  - 3   INDICATES MARKING ON EQUIPMENT
  - 4. TERMINAL DESIGNATIONS IN ( ) ARE THOSE APPEARING ON MATING CONNECTOR OF POWER SUPPLY CHASSIS
  - 5 CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM-B-650729
  - 6 CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM-B-650730
  - 7 ON CONTRACT DAAB05-T2-C-6507, TRANSISTOR TYPE 2N 4185 REPLACES 2N 4193, AND TYPE 2N 3250A REPLACES 2N 3250

EL 21 8003

Figure 2-11. 15/28v voltage regulator 1A1A10 through 1A1A12, 2A1A1, 2A1A12, and 2A1A4, schematic diagram.

crystal mixer currents in mixer 1A16Z1 are also provided. The CR1 metering and CR2 metering outputs are applied to the meter selector switch on the radio test set panel. Since the metering circuits are identical, only the CR1 metering circuit is described. Blocking, bypassing and filtering is accomplished by L5, C15, C17, C19 and L7. These components prevent loading of the rf signal and also prevent rf from appearing at the output. R15 and R17 comprise a voltage divider which establishes the proper level for the meter. TP1 provides a means to monitor the B + voltage (+ 15v). Resistor R1 is a dropping resistor and capacitor C2 provides rf bypass.

### 2-30. Attenuator Assembly 1A3 Circuit Functioning (figs. 2-12, 1-12.1 and 1-12.2)

a. Attenuator assembly 1A3 consists of a pcm attenuator/phase shift circuit, two (48 or 96 channel) orderwire attenuator/metering circuits, and two (48 or 96 channel) traffic monitor attenuation circuits.

b. The pcm attenuator circuit consists of R1 through R5, C1 and C2. Its input impedance is 50 ohms resistive and its output impedance is 150 ohms. With an input signal of 350 millivolts at 5 kHz, the attenuator provides an output signal of 5.3 millivolts. The circuit also provides a pcm signal phase shift of  $21 \pm 6$  degrees at 300 Hz.

c. The 48 CH/96 CH selector switch is set to the 48 CH position to select the 48 channel attenuator/metering circuits for the orderwire signal. The 96 CH selector switch position and associated attenuator and metering circuits are provided for future applications of Radio Set AN/ GRC-144. The orderwire input signal is applied across resistor network R6, R7 and R8. OW LEVEL ADJUST control R8 is used to set the orderwire signal to the proper level for combining with the pcm signal in af-rf amplifier 1A4. The orderwire signal is then routed through section 01 of the selector switch, resistor R9, and section C3 of the selector switch to af-rf amplifier 1A4. The attenuator circuit has an input impedance of 600 ohms and an output impedance of 40 ohms. With an input of 780 millivolts at 1.0 kHz, the attenuator circuit provides an output of 10.5 millivolts (adjustable by OW LEVEL ADJUST control). The orderwire signal is also coupled through C8 to the metering circuit, detected by CR1, CR2, filtered by C4 and attenuated by R10, R11 for application to the meter selector switch on meter panel assembly 1A15A8. Variable resistor R10 is used to calibrate this metering level.

d. A detected sample of the combined pcm and orderwire signal from radio transmitter modulator 1A8 is applied to the traffic monitor attenuation circuit R15, R16 through section C2 of the selector switch and pin 8. Resistor R15 and R16 provide the proper attenuation before the signal is applied to alarm monitor 1A5 through section C1 of the selector switch and pin 9. With an input of 35 millivolts the traffic attenuator circuit provides an output of 3.5 millivolts.

### 2-31. AF-F Amplifier 1A4 Circuit Functioning (fig. 2-13)

Af-rf amplifier 1A4 is a wideband video amplifier which provides a continuously adjustable gain (TRAFFIC LEVEL ADJ control). The maximum gain of the amplifier is 25 db. Af-rf amplifier 1A4 consists of first video amplifier Q1, second video amplifier Q2, and emitter follower Q3. The B + supply, + 15 vdc, input is through P13. Three decoupling capacitors C2, C5, and C6, are used in the B+ circuit to remove ac ripple from the circuit. Test point TP1 (+ 15v) can be connected to the meter selector switch with a test lead. Resistor R10 is a metering resistor. Af-rf amplifier 1A4 is also used in position 2A11 of R-1467(P)/GRC-144(V)(refer to para 2-74).

a. *1st Video Amplifier.* The pcm signal from attenuator assembly 1: A3 is applied to input jack J1 IN. TRAFFIC LEVEL ADJ potentiometer R2 determines the input level of the pcm signal coupled through C1 to the base of first video amplifier A1. The input impedance is 150 ohms (parallel combination of R1, R2, and input impedance of first video amplifier Q1). Transistor Q1 amplifies the pcm signal which is direct coupled to the base of second video amplifier Q2. Resistor R17, in the base circuit of Q1, stabilizes the input impedance of Q1. Resistor RX is the collector load for this stage and resistor R5 provides decoupling. Negative feedback is utilized to reduce distortion. A feedback path is used from the emitter of Q3 (junction R9 and R15) to the emitter circuit (R4) of Q1. A feedback path is also used from the emitter circuit (junction of R7 and R8) of Q2 to the base circuit (junction of R13 and C3) of Q1.

b. *2nd Video Amplifier.* Second video amplifier Q2 amplifies the pcm signal. The amplified output is direct coupled to the base of emitter

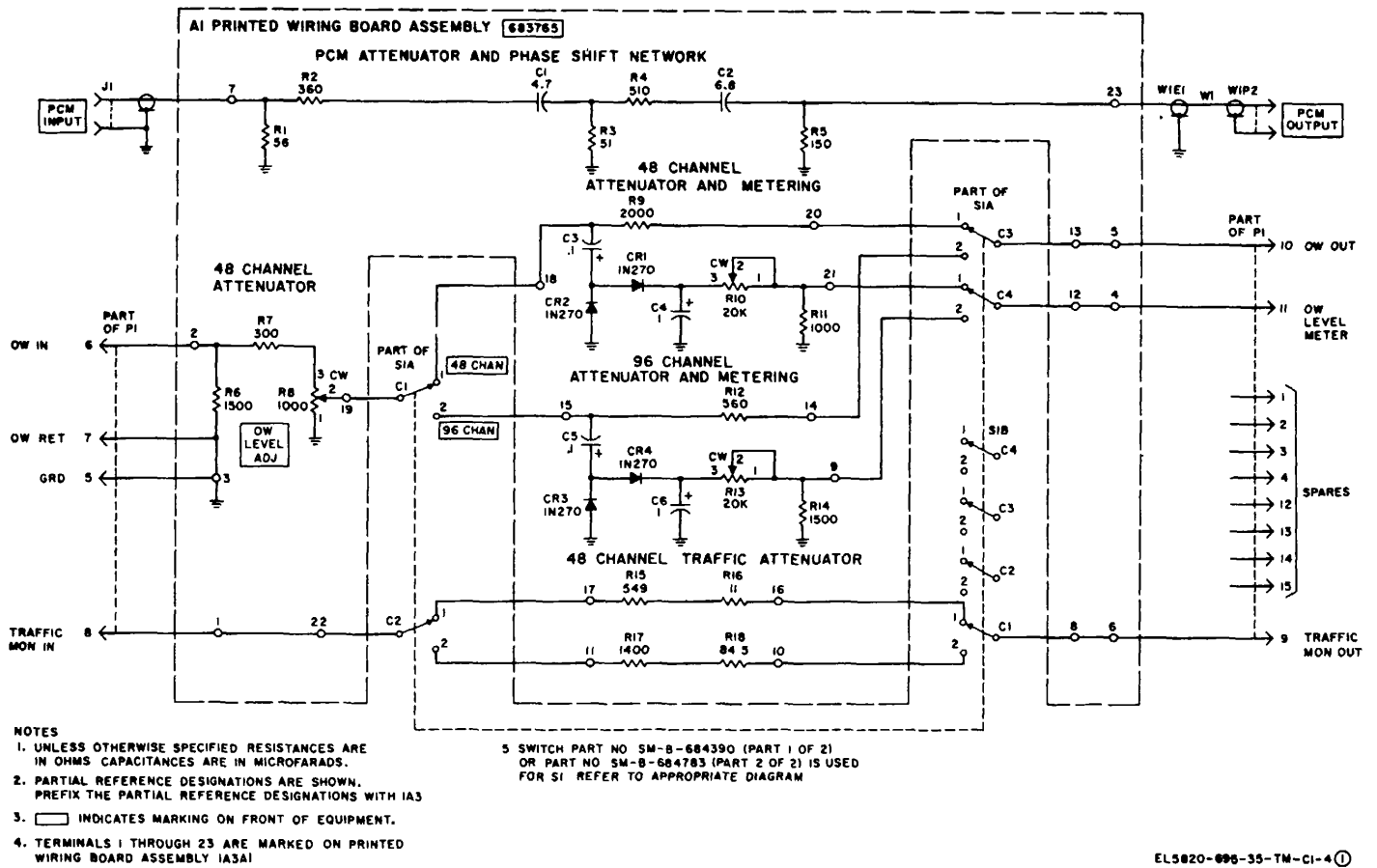
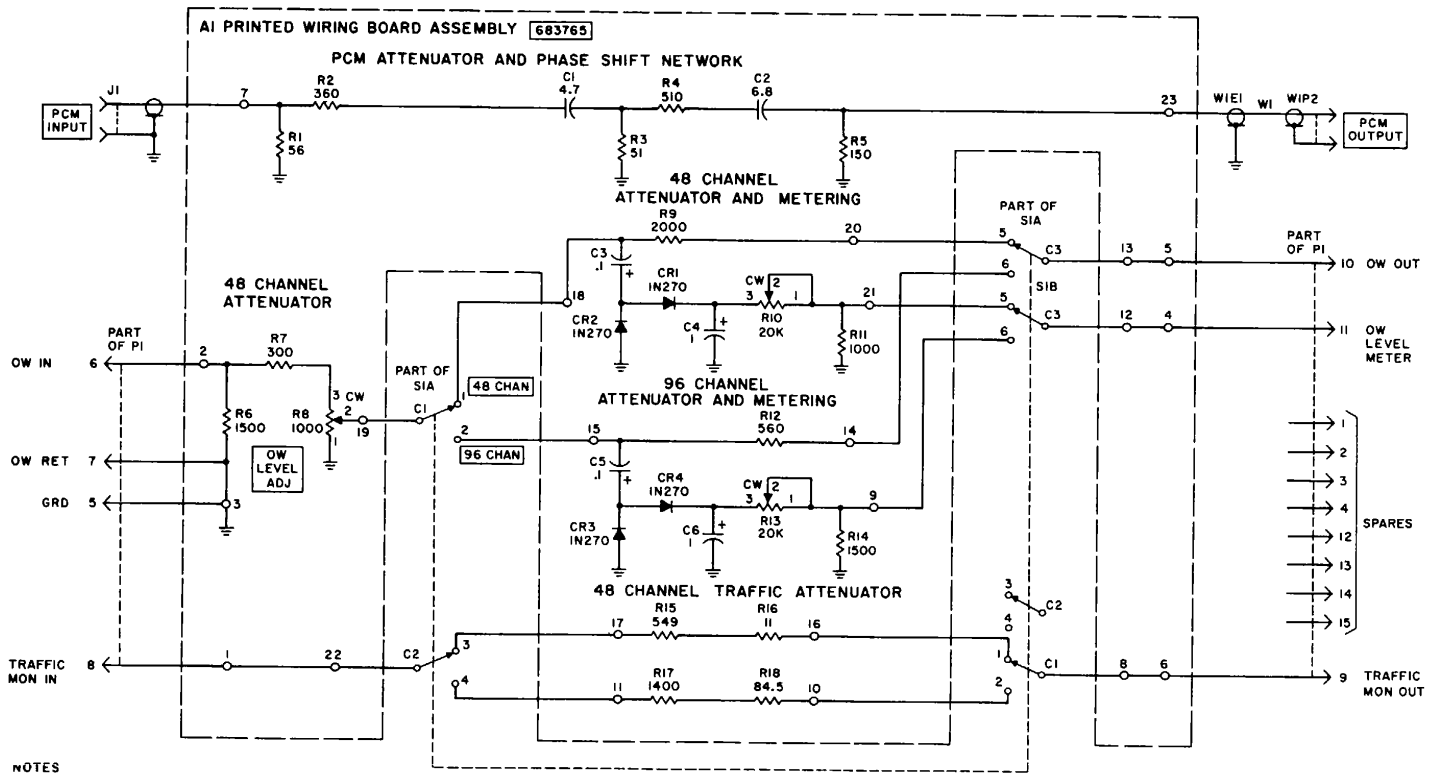


Figure 2-12(1). Attenuator Assembly 1A3, (683635) schematic diagram (Sheet 1 of 2).

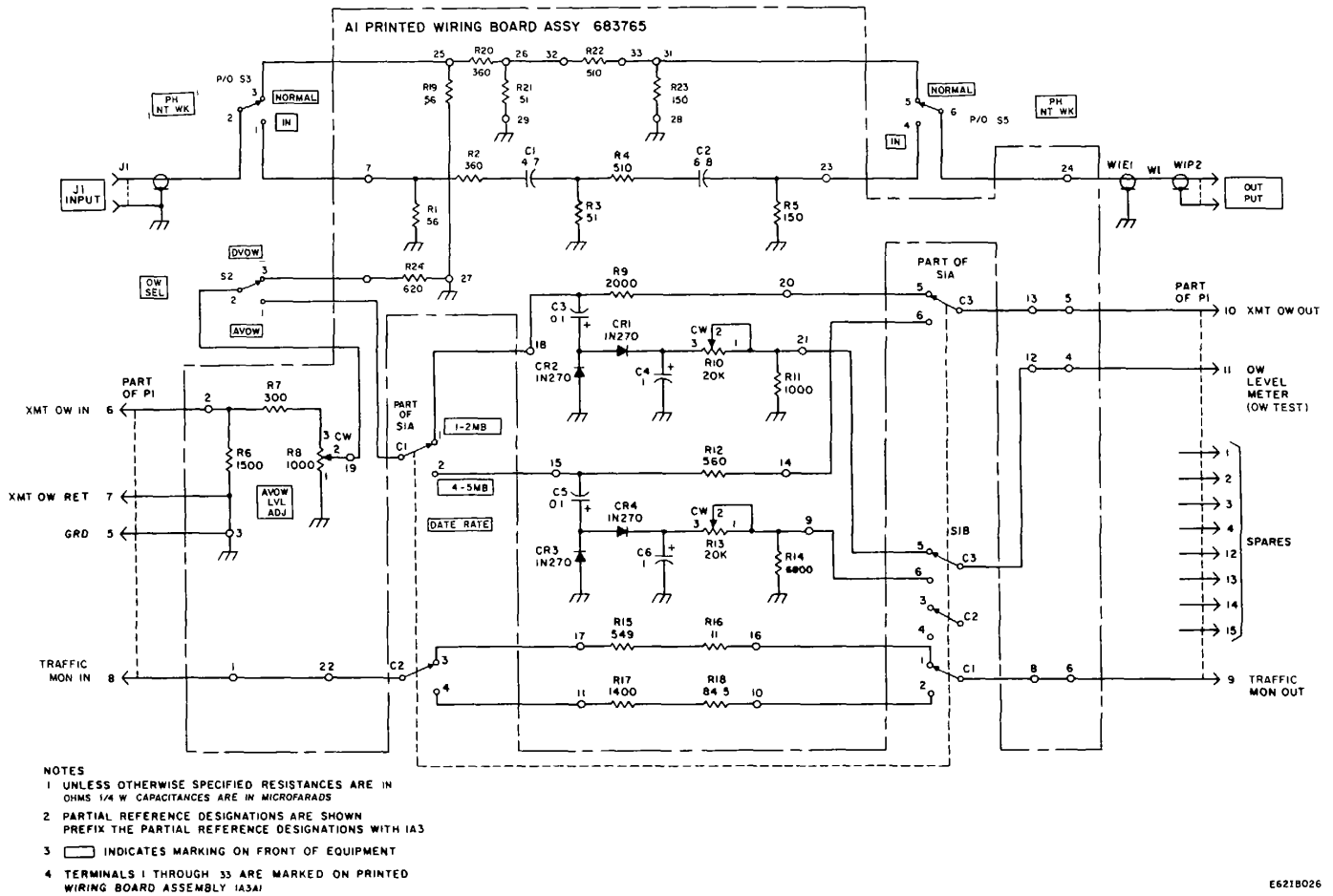


- NOTES
1. UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS.
  2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX THE PARTIAL REFERENCE DESIGNATIONS WITH IA3.
  3.   INDICATES MARKING ON FRONT OF EQUIPMENT.
  4. TERMINALS 1 THROUGH 23 ARE MARKED ON PRINTED WIRING BOARD ASSEMBLY IA3A1

5 SWITCH PART NO SM-B-684390 (PART 1 OF 2) OR PART NO SM-B-684783 (PART 2 OF 2) IS USED FOR S1 REFER TO APPROPRIATE DIAGRAM

EL5820-695-35-TM-C1-4 ②

Figure 2-12(2). Attenuator Assembly 1A3, (683635) schematic diagram (Sheet 2 of 2).



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Figure 2-12.1. Attenuator Assembly 1A3, (956429) schematic diagram.

Change 6 2-62.1

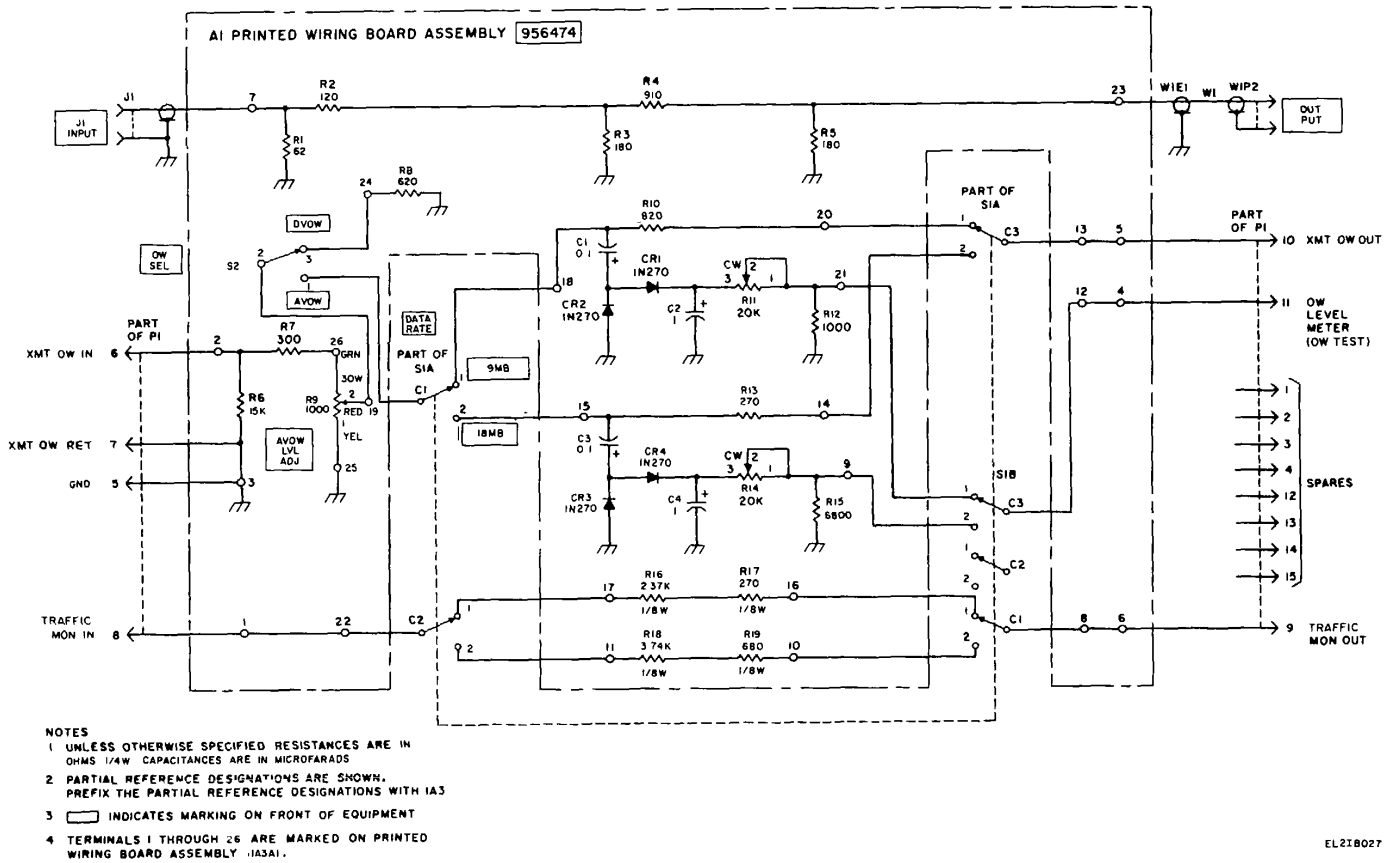
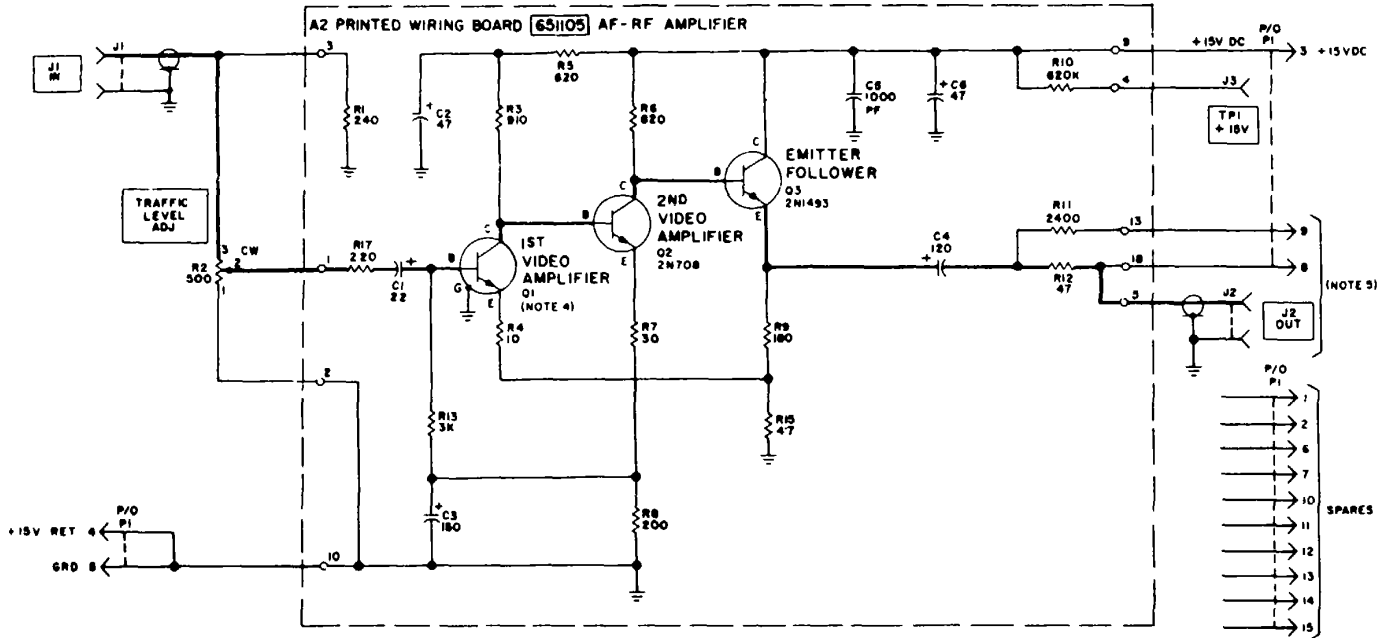


Figure 2-12.2. Attenuator Assembly 1A3, (956431) schematic diagram.

Change 6 2-62.2



NOTES

- 1 UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS CAPACITANCES ARE IN MICROFARADS
- 2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN PREFIX THE PARTIAL REFERENCE DESIGNATIONS WITH 1A4 OR 2A11
- 3    INDICATES MARKING ON EQUIPMENT
- 4 CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM B 55321
- 5 REFER TO TABLE FOR FUNCTIONAL IDENTIFICATION OF RECEIVER AND TRANSMITTER SIGNALS

RECEIVER	
CONNECTOR	FUNCTION
J1 IN	PCM/ORDERWIRE
J2 OUT	TRAFFIC OUT
P1 PIN 9	TRAFFIC MONITOR
P1 PIN 8	NOT USED
TRANSMITTER	
CONNECTOR	FUNCTION
J1 IN	PCM
J2 OUT	TRAFFIC OUT
P1 PIN 8	ORDERWIRE IN
P1 PIN 9	NOT USED

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Figure 2-13. Af-rf amplifier 1A4/2A11,) schematic diagram.

Change 6 2-62.3/(2-62.4 blank)

follower Q3. Resistors R7 and R8 are in the emitter circuit of Q2. C3 is an ac bypass capacitor.

c. *Emitter Follower.* Emitter follower Q3 provides an impedance match between the second video amplifier and the output. Q3 also provides negative feedback to Q1. The amount of negative feedback determines the overall gain and band-width of af-rf amplifier 1A4. The pcm signal is coupled by C4, R12 from the emitter of Q3 to the output jack (J2 OUT). The orderwire input signal from attenuator assembly 1A3 is also routed to the J2 OUT jack by P1-8. The combined pcm and orderwire signal is routed to the 4.5 MHz low pass filter (1A6) by the J2 OUT jack. The alarm output (P1-9) is not used in af-rf amplifier 1A4.

### 2-32. Alarm-Monitor 1A5 Circuit Functioning (fig. 2-14)

a. The alarm monitor circuits are shown in figure 2-14. Low level alarm-monitor input signals are amplified by operational amplifiers AR1, AR2 and AR4 (fig. 2-14, part 3). Operational amplifiers AR1, AR2, and AR3 are type U5B-770231X integrated circuits, see figure 5-24. The amplifiers are connected in different configurations to accommodate each particular alarm monitor input signal. The inverting input of the integrated circuit amplifier is pin 2, the non-inverting input is pin 3, and the output signal is taken from pin 7. The feedback resistance connected from the output pin 7 to inverting input pin 2 establishes gain of the amplifier.

#### NOTE

**The alarm monitor is used in position 2A12 of the R-1467/GRC-144 (refer to para 2-75).**

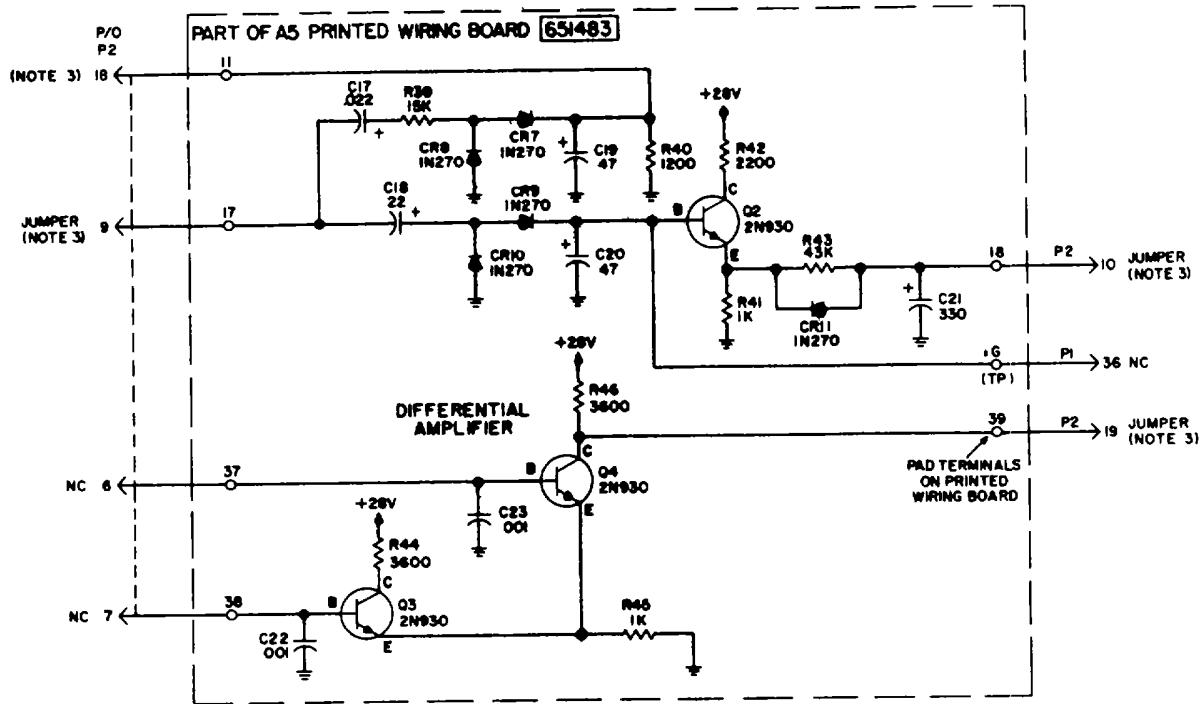
b. The traffic monitor signal from attenuator assembly 1A3 is coupled in pin A3 to the inverting input pin 2 of amplifier ARI1 (fig. 2-14(3)). Network C1 and R4, connected across the differential inputs pins 2 and 3, provides lag compensation which increases the high frequency response. The amplified traffic signal is applied to a diode peak detector circuit consisting of capacitor C4, diodes CR11 and CR2, and capacitor C5. The positive peak-detected dc voltage forward biases transistor Q1 which couples the signal through attenuator network R10, R11 and R12 to its associated Schmitt trigger circuit on board A5 (fig. 2-14(2)). It is also fed through R8 and pin 12 to the selector switch on meter panel assembly 1A15A8. The Schmitt trigger

circuit for the traffic signal consists of transistors Q5 and Q6. When no signal is present, transistor Q6 conducts and holds transistor Q5 off due to the voltage developed across common emitter resistor R48. The incoming peak-detected traffic signal will forward bias transistor Q5 when the magnitude of the peak-detected traffic signal exceeds the magnitude of the voltage developed across R48. When this occurs, the states will reverse with transistor Q5 conducting and transistor Q6 off until the peak-detected signal again drops below the voltage level of the common emitter resistor R48. The output of the Schmitt trigger is a series of positive square pulses which are developed at the collector of transistor Q6. These pulses are applied to the base of transistor Q7 and forward biases it into conduction. When transistor Q7 is conducting, its collector is at a low level; this provides a low impedance path to ground to light the normal (green) traffic indicator lamp. The inverted output level at the collector of transistor Q6 is applied to the alarm (red) traffic indication lamp. This transistor provides a low impedance path to ground for the alarm lamp when no traffic signal is detected (quiescent state of the Schmitt trigger circuit).

c. The reflected rf power monitor signal is developed by a diode detector in directional coupler 1,DC1 and coupled in pin 14 to the non-inverting input pin 3 of operational amplifier AR2 (fig. 2-14(3)). Resistors R19, R20 and potentiometer R22 provide a variable pad at the amplifier input. The incoming detected signal is also coupled through resistor RJ17 and out pin 15 to the meter selector switch on meter panel assembly 1A15A8. Capacitor C10, at the non-inverting input, integrates the input signal which is amplified and is coupled to the input of its associated Schmitt trigger circuit by a jumper wire from pin P2-8 to pin P2-11 through series resistor R55 (fig. 2-4(2)). The Schmitt trigger circuit consists of transistors Q8 and Q9 which functions in an identical manner to Schmitt trigger Q5 and Q6 previously described in b above with the exception that the normal indication is taken from the collector of Q9 and the alarm indication is taken from the collector of Q10. The presence of an input signal (high reflected power) will cause an alarm indication, the absence of an input signal (low reflected power) will produce the normal indication.

d. The rf power monitor signal, representing a sample of the forward power, is developed by a diode detector in directional coupler 1DC1 and





NOTES

- 1 UNLESS OTHERWISE SPECIFIED. RESISTANCES ARE IN OHMS CAPACITANCES ARE IN MICROFARADS
- 2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN PREFIX REFERENCE DESIGNATIONS WITH 1A5 OR 2A12
- 3 THE ALARM MONITOR MODULE IS USED IN TRANSMITTER MODULE POSITION 1A5 AND RECEIVER MODULE POSITION 2A12. REFER TO THE TABLES I THROUGH III TO DETERMINE THE CONNECTIONS USED FOR EACH MODULE POSITION. TABLE I LISTS P2 CONNECTIONS, TABLE II LISTS P1 CONNECTIONS AND TABLE III LISTS THE JUMPER CONNECTIONS MADE ON THE MATING CONNECTORS AT EACH MODULE POSITION. FUNCTIONS FOR P1 AND P2 THAT DO NOT CHANGE IN THE MODULE POSITIONS ARE SHOWN ADJACENT TO THE PIN CONNECTIONS.

TABLE I

CONNECTION	SIGNAL NAME	
	T-1054/GRC-144 (1A5)	R-1467/GRC-144 (2A12)
P2 - 2	RF PWR MON	NOT CONNECTED
P2 - 4	RF PWR MTR	NOT CONNECTED
P2 - 6	NOT CONNECTED	CARR (IF) MON
P2 - 7	NOT CONNECTED	CARR (IF) MON REF
P2 - 13	NOT CONNECTED	TRAFFIC MON
P2 - 14	REFL PWR MON	NOT CONNECTED
P2 - 15	REFL PWR MTR	NOT CONNECTED
P2 - A3	TRAF MON	NOT CONNECTED

4 INTEGRATED CIRCUITS AR1, AR2 AND AR3 ARE TYPE U5B770231X

TABLE II

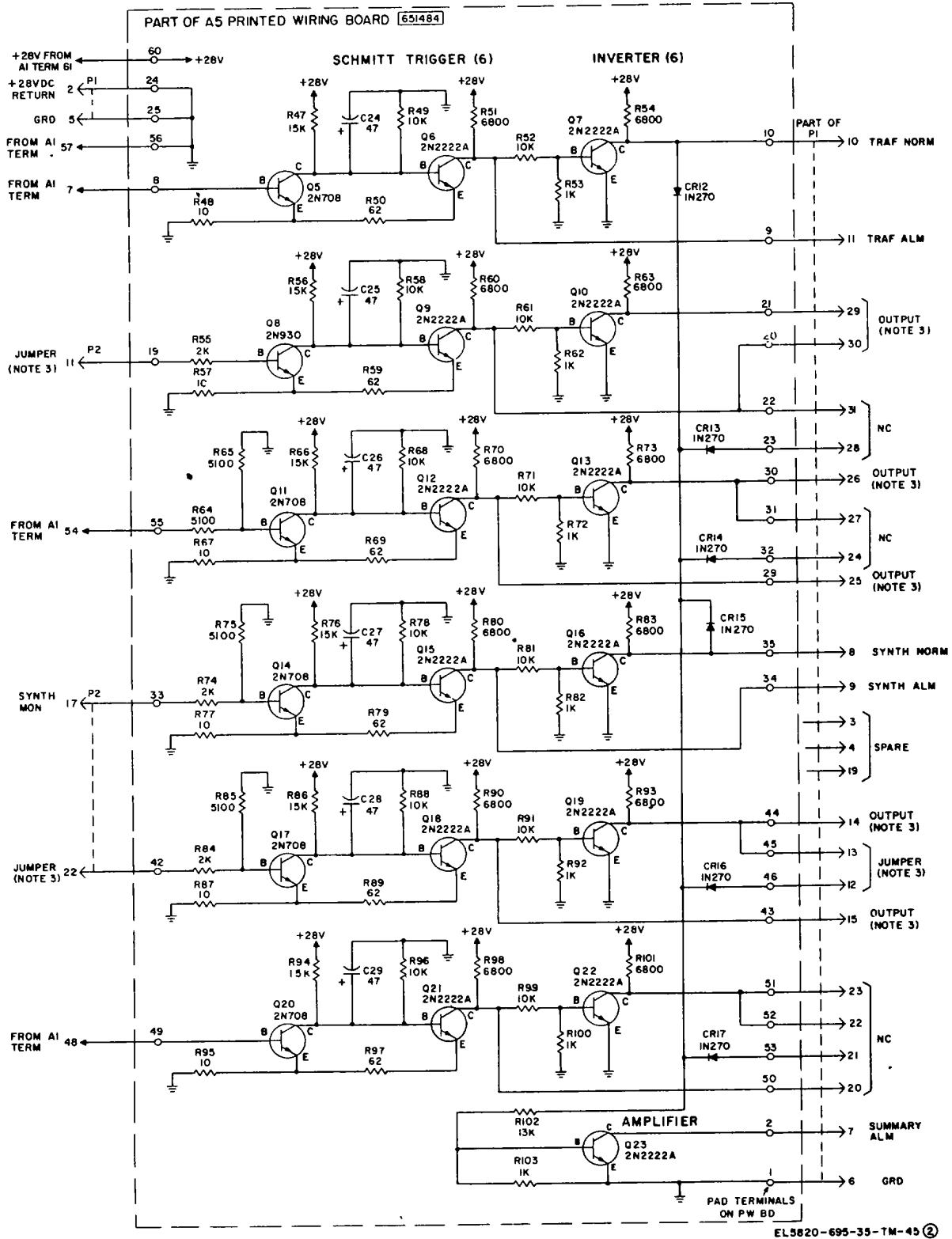
CONNECTION	SIGNAL NAME	
	T-1054/GRC-144 (1A5)	R-1467/GRC-144 (2A12)
P1 - 14	NOT CONNECTED	CARR (IF) NORM
P1 - 15	NOT CONNECTED	CARR (IF) ALM
P1 - 25	RF PWR ALM	NOT CONNECTED
P1 - 26	RF PWR NORM	NOT CONNECTED
P1 - 29	REFL PWR ALM	SPARE ALM
P1 - 30	REFL PWR NORM	SPARE NORM

TABLE III

JUMPER CONNECTIONS	
T-1054/GRC-144 (1A5)	R-1467/GRC-144 (2A12)
P2 - 11 TO P2 - 8	NOT CONNECTED
NOT CONNECTED	P2 - 22 TO P2 - 21
NOT CONNECTED	P2 - 19 TO P2 - 20
NOT CONNECTED	P1 - 12 TO P1 - 13

EL5820-695-TM-CI-5 ①

Figure 2-14(1). Alarm monitor 1A5/2A12, schematic diagram.



EL 5820-695-35-TM-45 ②

Figure 2-14(2). Alarm monitor 1A5/2A12, schematic diagram (part 2 of 3).

coupled in pin 2 to the noninverting input pin 3 of operational amplifier AR3 (fig. 2-14(3)) and through R25 and pin 4 to the meter selector switch on meter panel assembly 1A15A8. Resistors R26, R27 and R28 in the signal input path form a pad that provides approximately 15 db of attenuation. The amplified output from operational amplifier AR3 is connected by a jumper between terminal E54 and terminal E55 to the base of transistor QL1 (fig. 2-14(2)). Transistors Q11 and Q12 form a Schmitt trigger circuit that functions in a similar manner to Q5 and Q6 previously described in b above. When the rf power is above a minimum threshold level, established by the setting of the input attenuator, output transistor Q13 is conducting and provides a low impedance ground path for the normal indicator. When no signal is present, transistor Q12 is conducting and provides a low impedance ground path for the alarm indicator.

e. A synthesizer monitor signal is developed in electrical frequency synthesizer 1A14 and applied transistor to Q14 through pin P2-17 (fig. 2-14 (2)). This signal indicates when electrical frequency synthesizer 1A14 is not phase locked and is in a search mode attempting to correct the oscillator frequency. The Schmitt trigger consists of transistors Q14 and Q16. When electrical frequency synthesizer 1A14 is phase-locked, a +2 volt level is applied to input pin 17 to forward bias transistor Q14. This in turn, cuts off transistor Q15 and turns on transistor Q16 providing the normal (green) indication. When electrical frequency synthesizer 1A14 is not phase locked, the input signal drops to zero volts which turns on transistor Q15 producing the alarm (red) indication.

f. A four-input diode OR gate and inverting transistor provides the summary alarm function. This circuit consists of diodes CR12 through CR15, transistor Q23, and resistors R102 and R103 (fig. 2-14(2)). When the anode of any input has a positive voltage level applied to it, it conducts and forward biases transistor Q23 into conduction producing a summary alarm condition. When all of the diodes have a low (or zero) voltage applied to their anodes, they are nonconducting and transistor Q23 is turned off producing a normal indication.

g. Two zener diodes are incorporated on board 1A1, these provide regulated positive and negative voltages for the integrated circuits (fig. 2 14(3)). Zener diode CR5 in conjunction with resistor R31 provides a regulated plus 10 volts. Zener diode CR6, in

conjunction with resistor R33 provides a regulated minus 8.2 volts.

### **2-33. 4.5 MHz Low Pass Filter 1A6 Circuit Functioning (fig. 2-15)**

The 4.5 MHz low pass filter is connected in the orderwire/pcm signal path between af-rf amplifier 1A4 and radio transmitter modulator LA8. It aids in the overall shaping of the pulses before frequency modulation. The filter is a five-pole low pass filter and is tuned to approximate Gaussian shaping and has a nominal 3dB bandwidth of 4.5 MHz. At 6.4, 9.1, and 12.5 MHz the filter attenuation is 6, 12, and 20 dB, respectively. Source impedance is 50 ohms and load impedance is 150 ohms. The filtering components are L1, L2, and C1 through C5 and resistor R1 provides impedance matching. For Transmitter, Radio T-1054(P)A/GC-144(V), low pass filter 1A6 is not used for data rates 9 and 18 MB/s; it is replaced by cable assembly 1A6W1.

### **2-34. Electronic Frequency Control 1A7 Circuit Functioning (fig. 5-25)**

Electronic frequency control 1A7 produces an afc signal which stabilizes the center frequency of the 150 MHz vco in radio transmitter modulator 1A8. Electronic frequency control LA7 is comprised of the following circuits: (1) 70 MHz frequency modulated input, (2) reference crystal oscillator, (3) multivibrator, (4) amplifier-limiter chain, (6) discriminator, (6) ac amplifier, and (7) phase detector.

a. *70 MHz Frequency Modulated Input Circuit.* The 70 MHz frequency modulated signal (FREQ CONT INTERCONN) from 1AS is applied to emitter follower Q3 via coupling capacitor C5 and connector J'1 (INPUT). This stage isolates the input from the load. Resistor R8, which is rf grounded by capacitor C9, provides the proper termination at the input. The stage is biased by resistors R9, R10, and R26. The output from R11 is fed to a diode gate through C14. Capacitors C27 and C30 provide bypass and L9 is an rf choke. The diode gate consists of CR4,

CR5, CR6, coupling capacitors C21., C22, and load resistors R18, R19. Approximately 3 vdc is impressed on the cathode of CR6 from a voltage divider consisting of R12 and R13 (L8 is an rf choke). Depending on the

operating state of Q5, the anode of CR4 is at either approximately + 14 volts (Q5 cut off) or below 1.0 volt (Q5 saturated). When this voltage is high, the diodes are forward biased, and the signal from .3 appears

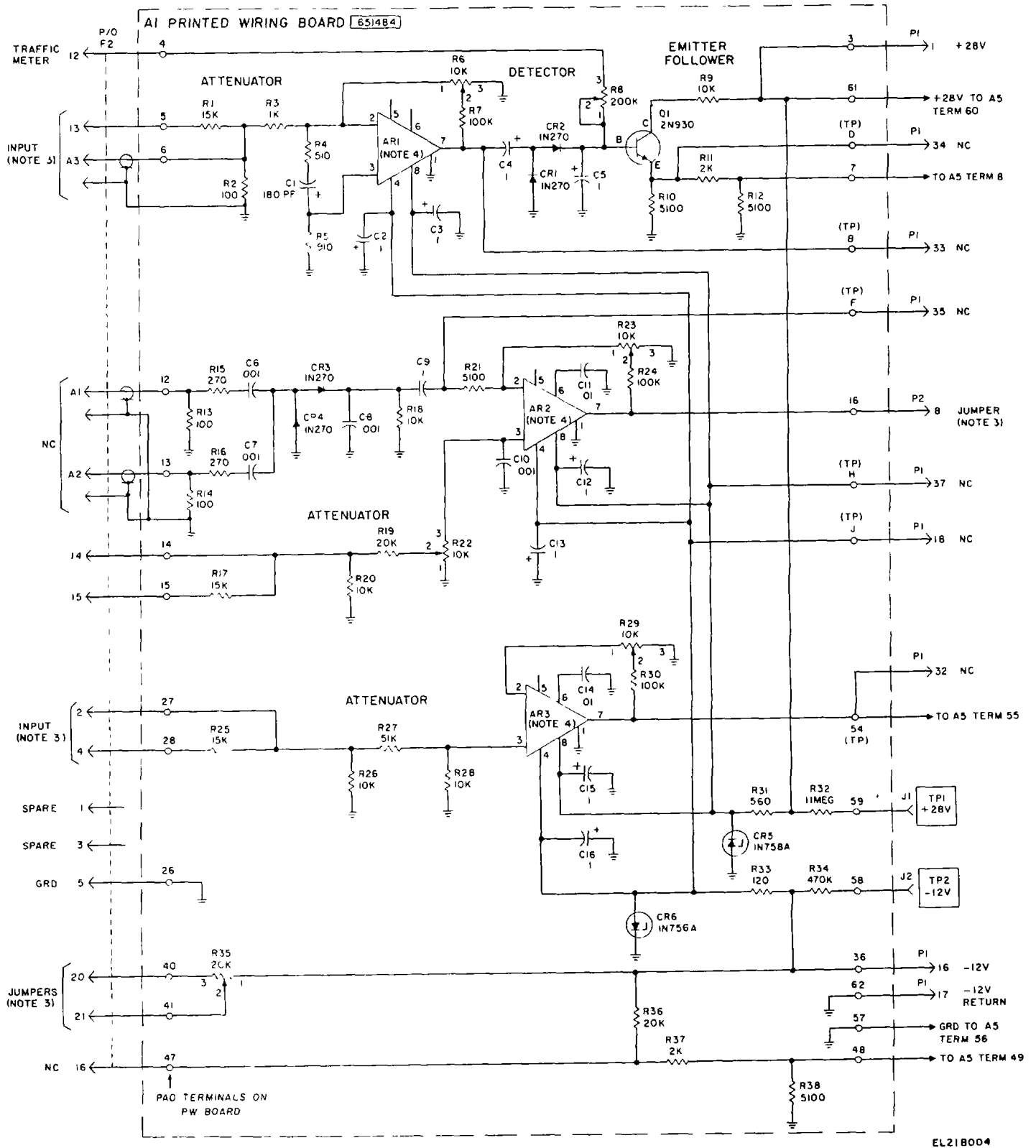
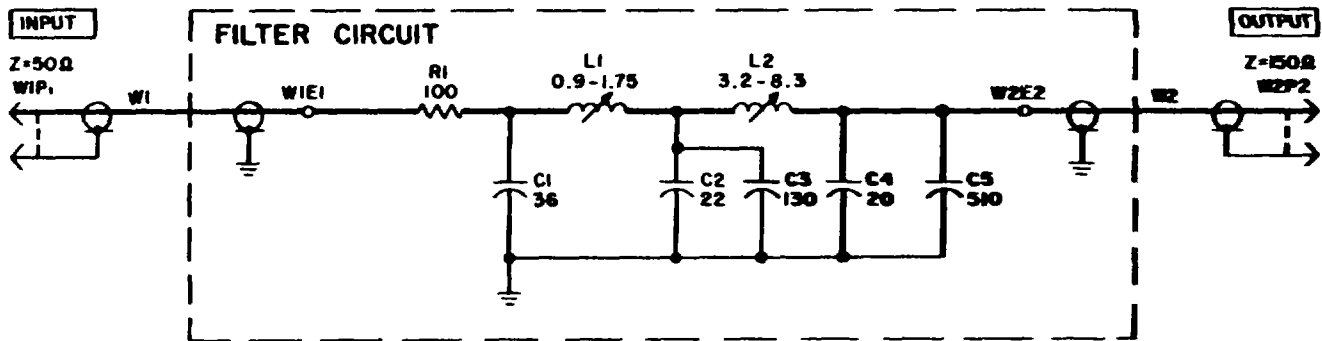


Figure 2-14 (3) Alarm monitor 1A5/2A12, schematic diagram (part 3 of 3)



**NOTE:**

1. UNLESS OTHERWISE SPECIFIED:  
CAPACITANCES ARE IN PICOFARADS  
INDUCTANCES ARE IN MICRONENRIES.  
RESISTANCE VALUES ARE IN OHMS.
2. PARTIAL REFERENCE DESIGNATIONS ARE  
SHOWN; PREFIX REFERENCE DESIGNATIONS  
WITH IAG.
3.  INDICATES MARKING ON EQUIPMENT.

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at the output With CR4 anode low, the diodes are reverse biased and no signal flows. b. Reference Crystal Oscillator The reference crystal oscillator generates a precise 70 MHz reference signal which is compared with the sampled 70 MHz signal from radio transmitter modulator 1A8. The oscillator stage is comprised of transistor Q1, crystal Y1, tank circuit C7 and L2 bias resistor R1, R2, R3., R5 and R6, loading resistor R4, rf choke L1, bypass capacitors C1, C2, C3 and C10, and coupling capacitor C4 and C6. The crystal operates in series resonance on the fifth overtone When voltage is applied, the initial transient causes oscillations to start. The crystal signal at Q1 emitter base an amplified signal to appear at Q1 collector. The tank circuit which is tuned closely to the crystal frequency, resonates and feeds a reinforcing signal back to the crystal through C6. is causes further buildup in the signal level of the tank, and increased feedback to the crystal. This increase in level continues until the transistor gain drops to unity, at which time a sustained level is maintained.

Variable inductor L2 in the tank is used to adjust the frequency of oscillation by a small percentage. With the tank turned above the crystal frequency, the tank appears capacitive to the signal at the collector, causing the feedback signal to lead the crystal frequency. The crystal pulls to a higher frequency in order to restore a zero phase condition. Since the crystal has a very high

Q, while that of the tank is quite low, the crystal frequency shift is very small compared to that of the tank. The crystal oscillator is dc coupled to emitter follower Q2 through resistor R75. The collector is isolated from +15 volts BY L3 and C11. This stage decouples the oscillator from the following circuit. The output is taken from the following circuit. The output is taken from the junction of the bias resistors R14 and R15 and is coupled to a diode gate through capacitor C12. The gate circuit consists of diodes CR1, CR2, CR3, coupling capacitors , C19, C20, load resistors R16, R17, and decoupling networks L5, C13, and L7, C18. The operation of this gate is identical to the CR4, CR5, gate previously described.

c. Multivibrator. The multivibrator is a symmetrical, free running, multivibrator consisting of transistor stages Q4, Q5. Its function is to supply gating signals to the previously described diode gates. These signals consists of positive rectangular pulses appearing alternately at the Q4 and A5 collectors. When the pulse is present at Q4 collector, diode gate CR1, CR2, CR3, is enabled. During this period the pulse is absent at Q5 collector, so that is associated gate, CR4, CR5, CR6 is open. The mulivibrator drive to the gates is applied through S1. When this switch is in the OPR position, the gates are under control of the multivibrator. In the TEST position, the multivibrator is disconnected and CR1, CR2

CR3 gate is held on by the +15 volt applied through R7.

(1) When voltage is applied, one transistor conducts more heavily due to noise or small component variations. For discussion purposes, assume that Q4 is initially conducting. Q4 collector voltage drops from + 16 volts to a lower value. Since the charge across a capacitor cannot change instantaneously, the voltage at the negative plate of C15 drops causing Q5 base voltage to decrease. Q5 conduction decreases, and its collector voltage rises. This increase is coupled to Q4 base through capacitor C23 causing the Q4 collector current to increase further. This loop is repeated until Q5 is driven below cutoff, and Q4 goes into saturation. The above occurs so rapidly that the resulting wave is essentially a step function. CR8 is now forward biased and current flows through it and resistors R21, R24, and R25 to ground. As a result, Q5 collector is at approximately + 14 volts and the drop across R25 is approximately +13 volts. Diode CR7 is reverse biased and therefore blocks the +11 volts from Q4 collector.

(2) Since the charge across C16 and the bias of R26 are aiding, C15 discharges through Q4, R25 and R23, in an exponential fashion. When Q6 reaches cutoff, it begins to conduct, causing its collector voltage to drop, pulling down Q4 base. Q4 collector voltage increases, and this increase is coupled back to Q5 base through C15. The feedback process as previously described results, but, in the reverse order, causing Q4 to be cutoff and Q5 to go into saturation. CR7 is now forward biased and current flows through it and resistors R20, R24, and R25 to ground. The charge across C23 discharges through Q5, R25, and R22. Thus, a square wave is produced alternately at the Q4 and Q5 collectors.

*d. Amplifier-Limiter Chain.* The amplifier limiter chain is comprised of transistor stages Q7 through Q11. The two diode gates, previously described, provide alternate input signal to the amplifier-limiter chain. This results in the 70 MHz frequency modulated signal from 1A8 and the 70 MHz reference signal from the crystal oscillator appearing alternately at the junction of C25 and C26. Since the multivibrator is symmetrical, these signal samples are of equal duration.

(1) Each signal sample is impressed across gate load resistor R29 at the base of emitter follower Q7, through coupling capacitor C29. Q7 is biased by R28, R30 and R31, the latter also serving as the emitter load. C28 and C32 are bypass capacitors and J10 provides decoupling. C54 prevents oscillation.

The output of Q7 is coupled, via C37, to limiter stage Q8, which is in the common base configuration. Inductor L12 is used to tune the collector to the signal frequency. L11 provides isolation and C33, C35, and C36 are bypass capacitors.

(2) Common base limiter stage Q8 operates with approximately 12.2 volts fixed bias on the base, derived from voltage divider R32 and R33. The emitter current through R34 and R36 produces a quiescent emitter voltage of approximately 11.5 volts, so that the quiescent base to emitter voltage is approximately 0.7 volt. Thus, when the instantaneous signal level during the positive half cycle exceeds about 0.7 volt, the transistor cuts off, clipping the positive portion at the collector. Transistor Q9 operation is identical to that of Q8 and is driven by Q8 through C40. Fixed bias is provided by resistors R37-R40. Signal tuning is provided by L15. L18 and L14 provide isolation and C42 are bypass capacitors.

(3) Emitter follower Q10 is driven by common base amplifier Q9 through coupling capacitor C46 and attenuating resistor R45. The transistor is fixed biased by R43, R44, R46 and R47. The collector is bypassed by C47, and decoupled by L16, L17, and C46.

(4) The final stage in the amplifier-limiter chain is discriminator driver Q1, which is operated in the common base configuration. The drive signal is applied at the junction of R51 and R52, through C49. The base is dc biased at +2.1 volts by voltage divider R48 and R49 and bypassed by C48. The quiescent emitter voltage is approximately + 1.4 volts, giving a base to emitter of 0.7 volt.

(5) A metering circuit is also provided at the output of limiter stage Q9. This is a diode detector, consisting of CR9, C43, C044, R41 and R42. Variable resistor R41 provides output level adjustment. The dc output at J3 permits observing the response, and is used, for example, when tuning variable inductors L12 and L15.

*e. Discriminator.* The discriminator is comprised of transformer T1., diode detectors CR10 and CR11E, diode equalizing resistors R76 and RT7, load resistors R53 and R54, coupling capacitor C51, tuning capacitors C62 and C56, temperature compensating capacitor C68, bypass capacitor C54, and decoupling network L18 and C50. The discriminator operates on the phase shift principle. The output is a square wave in which the differential level represents the frequency difference between the reference signal from 1A8

and the signal from the reference crystal oscillator.

(1) Both the primary and secondary of T11 are tuned to 70 MHz. Connector J4 (TP4 DISCR) is used for observing the response during alignment. Tuning is accomplished by means of variable capacitors C52 and C53. Q11 output is connected to the primary at terminal 3 through parasitic suppressor resistor R50, and to the secondary center tap (terminal '5) through dc blocking capacitor 051. At resonance (input signal at 70 MHz), the voltages across two halves of the secondary are in quadrature with the voltage across the primary and in opposition to each other. When the input signal frequency is higher or lower than the resonant frequency, the phase angle between one half of the secondary and primary will be greater than 90 degrees. The phase angle between the other half secondary and the primary will be less than 90 degrees, and as in the resonant conditions will be 180 degrees out of phase with the other half secondary.

(2) The signal at the anodes of CR10 and CR11, are the vector sums of the primary and associated half secondary voltages. At resonance, they will be of equal amplitude; in all other cases they will be unequal. The circuit is arranged so that CR10 anode voltage exceeds that at CR11 anode when the input frequency is below resonance, resulting in a positive signal appearing at R55. Each diode conducts when its anode is positive with respect to its cathode. Thus CR10, conducts on one half cycle, while CR11, conducts during the next half cycle. Consequently, the output from the discriminator is the difference between the two. At resonance, the levels are equal and the output is zero. Above resonance the signal at CR11 is higher and therefore a negative signal is produced. Actually, because of the phase difference between the two voltages, the output is a pulsating wave with a repetition rate at the input frequency. This wave is average by RC network (R55, C56) to produce an essentially dc level.

*f. AC Amplifier.* The discriminator square wave output is amplified in an ac amplifier chain consisting of transistor stages Q12, Q13, Q14, and Q115. Negative feedback is employed for stabilization. The input appears at Q12 base through R57 and C57, which, drives Q13, and Q12 emitter being tied directly to Q13 base. To prevent positive feedback, Q12 collector is isolated by R61 and bypassed by a capacitor C58. The output of Q13 is developed across R59 and is dc coupled to Q14 base. Bypass capacitor C60 removes high frequency components from Q14. The input to

Q14 goes to ground through R63 which is also connected to the base circuit of Q12 through R58 to provide a dc bias at Q12. Bypass capacitor 062 prevents positive feedback to Q12. The output of Q14 is developed across R62 and is dc coupled to the base of emitter follower Q15. Resistor R65 in the emitter circuit of Q15 and Q13 provides negative feedback to Q13. The output of the agc amplifier appears at Q15 emitter across R64 and R65, and is coupled to the phase detector through C65 and R66. Power supply decoupling is provided by L20 and C59.

*g. Phase Detector.* The output from the agc amplifier is an ac square wave with the peak amplitude representing the frequency difference between the sampled modulator frequency and the reference crystal oscillator frequency. However, the signal does not identify whether the modulator frequency is high or low. This information is provided by the phase detector. The phase detector is comprised of transformer T2, detector diodes CR12 and CR-13, and associated components.

(1) The Q15 output is applied to the primary of T2 where high frequency components are bypassed by capacitor C64. This signal is also applied to J5 (TP3) for monitoring. The drive to the secondary center tap is supplied by the Q4, Q5 multivibrator through R27 of emitter follower Q6, coupling capacitor C31, and R36. Emitter follower Q6 is driven through R74 from the square wave used to trigger the diode gate which controls the modulator frequency sample input. This signal also appears at J2 (TP) and is used as an oscilloscope sync for waveforms taken at J3, J4, and J5. The positive portion of the signal from Q6 is synchronized with the half cycle from Q1,5 and corresponds to the modulator frequency error signal.

(2) During the positive half cycle of the gating pulse, diodes CR12 and CR13, conduct. The ground return for this current path is located in the differential amplifier in the modulator module. When the modulator error signal is positive during this period a current flows through resistor R70 from top to bottom. Conversely, when the modulator error signal is negative, the current flows from bottom to top of R70. When the gating signal goes negative, both diodes are back biased and only a small current flows through R70. Thus, the phase detector output is a positive or negative square wave above or below the zero axis. The square wave is converted to a dc signal by RC networks in the mod-



ulator differential amplifier. Diodes CR14 and CR15 comprise a limiter, which limits the voltage amplitude at the input to CR12 and CR13.

Resistor R78 and capacitor C69 are used to set the ac ground point. Resistors R68 and R69 are diode load resistors. The circuit is arranged so that the FREQ CONT lead at P1-8 is positive with respect to the FREQ CONT RETURN lead at P11 when the modulator frequency is high. A metering signal (CENTER FREQ METERING) is also applied to the meter selector switch through metering resistors R71, and R72.

(3) The supply voltage (+15 volts) is supplied from an external source to P113. Inductors IA, L19, L21, and L22, and capacitors C&3, C66, and C67 provide power supply isolation. The + 16 volts is applied to J6 through R67 for monitoring.

### **2-35. Radio Transmitter T-1054(P)/GRC144(V) Modulator 1A8 Circuit Functioning (fig. 5-26)**

Radio transmitter modulator 1A8 is comprised of modulator circuits and frequency control circuits. The modulator circuits produce a 160 MHz subcarrier which is frequency modulated by the baseband input signal (pcm/ow). The frequency control circuits produce a 70 MHz signal (sample of modulator frequency) which is applied to electronic frequency control 1A7 where it is compared with a precise, locally generated, 70 MHz signal. A dc signal, proportional to the modulator frequency error, is generated in electronic frequency control 1A7 and applied to the modulator circuits for center frequency correction (para 2-34).

a. Modator Circuits. The modulator circuits consist of a baseband amplifier, differential amplifier, 160 MHz voltage controlled oscillator, and limiter-amplifier stages.

(1) The pcm/ow input at J1, is applied to operational amplifier A1 through coupling capacitor C28 from parallel terminating resistors R1 and R2. Variable resistor R2, is a front panel control which is used to adjust the baseband level into the vco, thereby setting the system deviation. Resistors R4 and R6 establish bias and C3 provides bypass. Resistors R6, R8, R29, and capacitors C5 and C6 are compensation elements which set the gain and shape the amplifier response. The supply voltage to this stage is BY % passed by C8. The output at pin 7 of A1 is applied from load resistor R67 to the tank circuit of the 150 MHz vco, through coupling capacitor C7. Emitter follower A2D, also connected to the input at J11 through coupling capacitor C1, samples the baseband input. Resistors R3 and R9

set the bias for emitter follower A2D. The output A2-D is routed from load resistor R7 through coupling capacitor C4 to alarm monitor 1A4, and to the meter selector switch on meter panel assembly 1A15A8 through attenuator assembly 1A3. With the meter selector switch in the TRAFFIC position, the meter indicates the presence of a baseband signal at the modulator input.

### **NOTE**

**Amplifiers A1 and A2 are integrated circuits. A1 is type A702 and A2 is type CA3018. These circuits are illustrated in figure 5-24('11).**

(e) Differential amplifier A2A and A2B is driven by the low level dc correction signal from electronic frequency control 1A7. Resistors R10, R11, R12, and R13 provide bias for the base circuits and R16, R17, and R18 set the emitter voltages. C9 through C13 are bypass capacitors. The correction signal is applied between the bases of A2A and A2B through isolating resistors R20 and R21,. With no driving signal present, both transistors will conduct. Since they are identically biased, their collector currents will be essentially equal. Therefore the output of A2A (junction of RP4 and R16) will be positive with respect to the output of A2B (collector of A2B). This results in a reverse bias being impressed (through isolating resistor R77 and rf choke L3, IA) across varactor diodes CR1 and CR2 in the 160 MHz voltage controlled oscillator. When the correction signal at A2A goes positive with respect to A2B, A2A will conduct more and A2B will conduct less. With increased current through collector resistor R14, the output voltage of A2A will decrease. Similarly, the output (collector) voltage of A2B will increase because of the reduced voltage drop across R19. Thus, the voltage difference between these outputs decreases resulting in a decrease in the bias voltage applied to the varactor diodes in the 160 MHz voltage controlled oscillator. It will also be seen that when A2B input signal is positive with respect to A2A, the bias applied to the 160 MHz voltage controlled oscillator will increase. EFC DISABLE switch S1 is connected across the error signal input from electronic frequency control 1A7. With this switch closed, the error signal is disabled, and A2A and A2B conduct under internal bias conditions. The EFC DISABLE switch is used

while adjusting the 150 MHz voltage controlled oscillator center frequency.

(3) The 150 MHz voltage controlled oscillator consists of transistor Q11, bias resistors R22, R23, R24, R26, coupling capacitors C16, C18, bypass capacitors C14, C17, C19, C20 and tank circuit L2, C16, CR1, CR2, R73. Varactor diodes CR11 and CR2 are always operated reverse biased. They exhibit an inverse square law capacitance reverse bias characteristic, that is, the capacitance varies approximately as the inverse of the square root of the reverse bias voltage. By varying the bias voltage, or baseband input signal, the resonant frequency of the tank is made to vary. With only the bias voltage from the differential amplifier applied, the tank resonant frequency will determine the oscillator frequency. If the bias is increased, the diode capacitance will decrease, causing the tank to resonate at the higher frequency. Similarly, a decrease in bias will cause a decrease in the resonant frequency. Since this bias voltage represents the center frequency error, as detected in electronic frequency control 11A7, the voltage controlled oscillator center frequency follows the frequency of the reference oscillator in electronic frequency control 1A7. The center frequency is initially set during alignment by means of front panel variable capacitor C15. If a baseband signal is applied at the junction of CR1' and CR2, the frequency will be made to vary about the center frequency; thereby producing a frequency modulated 160 MHz output. Since electronic frequency control 1A7 senses the average frequency, it only corrects for center frequency drift and has no effect on the frequency modulation of the carrier. The output across load resistor R25 is applied to emitter follower Q2 which prevents loading of the 150 MHz voltage controlled oscillator stage. The collector of this stage is bypassed by C21 and its output is developed across R27. The output of Q2 is applied through coupling capacitor C22 and resistor R28 to the base of limiter-amplifier stage QS.

(4) Limiter-amplifier Q3 amplifies the input signal. The operating point of Q3 is set by biasing resistors R31, P2, and R34 and load resistor R33. The emitter is bypassed by capacitor C26 and provides power supply isolation. Diode limiter CR3, CR4, and C24 is connected to the Q3 collector output. Its purpose is to prevent amplitude variations (amplitude modulation) from appearing at the modulator output. CR3 and CR4 are silicon diodes and the limiting action is achieved by utilizing a semiconductor junction

characteristic, known as junction barrier potential. Essentially this means that, with forward voltage applied to the diode forward conduction cannot start until the junction barrier potential is exceeded. In silicon junctions this potential is approximately 0.65 volt. During the positive half cycle of the signal, CR3 is forward biased while CR4 is reversed biased. When the instantaneous signal level reaches approximately 0.05 volt, OCR conducts bypassing higher levels through bypass capacitor C24 to ground. During the negative half cycle, the bias conditions of CR3 and CR4 are reversed. At an instantaneous signal level of -0.65 volt, CR4 conducts, bypassing higher amplitude (more negative) voltages to ground. Thus, the output of limiter-amplifier stage Q3 is a frequency modulated sine wave, but clipped at a peak amplitude of  $\pm 0.65$  volts. The output of Q6 is coupled through capacitor C25 to amplifier Q4, which in turn is coupled through capacitor C27 to amplifier Q8. Transistor Q4 and Q8 are conventional, dc biased voltage amplifiers. Biasing is by means of resistors R85, R36, R37, and R54, R05 and R56. C29 and C48 are emitter bypass capacitors. At each amplifier output (Q4 and QS) is a low pass matching section consisting of L23, C28 and L16, C47. The low pass matching sections suppress the harmonics generated by the clipping action in the limiter. Q4 is decoupled from the 28v supply by L22, R72, FLM, and L5. L17, FF16, and L15 provide isolation for Q8. Capacitor C49 couples the output of Q8 to power amplifier Q9, which operates class C. The operating point is set by bias resistors R69 and R70. Resistor R9 is variable and permits bias adjustment. L18, R71, and FL8 block signal currents from the bias circuit. The Q9 collector output is tuned by L19 and C01 and coupled by C52 to low pass filter L20 and C63. The filter suppresses harmonics produced in the amplifier. This stage is decoupled from the 28v supply by FL7, C50, O54, and L21. The filter output (frequency modulated 150 MHz signal) is applied to transmitter frequency mixer stage 1A9 via connector P1 (150 MHz OUTPUT) and attenuator/matching network R63, R64, R65 and to the meter selector switch on meter panel assembly 11A15A8 through a metering circuit and pin P8-9 (OUTPUT LEVEL METERING). The metering circuit consists of coupling capacitor C60, load resistors R59 and R61 diode detector CR10, and metering resistors R62 and R66. Resistor R66 is variable and is used to adjust the meter deflection. Capacitor C61 bypasses ripple. The 150 MHz output of low pass filter L20 and C53 is also applied to transformer mixer T3 in

the frequency control circuits through attenuator network R60, R68, and R74.

*b. Frequency Control Circuits.* The frequency control circuits consist of a 100 MHz crystal controlled oscillator, a frequency doubler, a mixer, and two 70 MHz amplifier stages.

(1) The 110 MHz crystal oscillator consists of transistor Q5, crystal Y1, tank circuit L6, C31, C32, and C33, bias resistors R40, R4J1, and R42, load resistors R76, bypass capacitor C30, coupling capacitor C34, and isolating network FL3, L9, C37. The crystal operates at series resonance in the fifth overtone. When voltage is applied, the starting transient causes oscillations to start. The crystal signal at Q5 emitter is amplified and appears at the collector of Q5. The tank circuit follows the oscillation, and feeds a regenerative signal to the crystal oscillator. By this process, the oscillator signal builds up until the transistor gain is reduced to unity, at which point a stable level is sustained. Variable capacitor C33 provides a means of varying the frequency by a small incremental value. To illustrate, assume the tank is tuned to a frequency above that of the crystal. This will cause the tank to appear slightly capacitive to the collector signal. As a result, the signal fed back to the crystal leads the crystal oscillating signal. For this condition, the crystal frequency will pull to a higher frequency, in an attempt to restore a zero phase condition. This will result in a reduced phase difference between the collector signal and the tank, and consequently a smaller lead angle in the crystal feedback signal. As a result, the crystal will assume a frequency of oscillation above its normal frequency at which the phase is essentially zero. The crystal frequency shift is very small compared to that of the tank, because the crystal Q is very high and the Q of the tank is relatively low.

(2) The 1,10 MHz crystal oscillator signal at the collector of Q5 is applied to the primary of T2 in the frequency doubler. This circuit is, in effect, a full wave rectifier, in which CR5 and CR6 alternately pass a half cycle of the input signal. The fundamental of this composite output is twice the input frequency. The output also contains significant higher order harmonics, which are blocked by the output tuned circuit made up of C35, L8, and the inductance contributed by T3. The 220 MHz output of the frequency doubler is added to the mixer circuit.

(3) The 220 MHz doubler output is connected to the primary of transformer T3 in the mixer, while the sampled 1.50 MHz from the modulator is

applied to the center tap of T3 secondary. The voltage appearing across the transformer secondary is, therefore, the 220 MHz oscillator frequency superimposed on the 1.50 MHz modulator frequency. When terminal 3 of T3 is positive with respect to terminal 5, both diodes, CR7 and CR8 conduct, and the composite signal appears at the top of C38. With the reverse polarity, both diodes are reverse biased and no signal flows. As a result, only the portion of the composite signal above the zero axis appears at the C38, L10 junction. The envelope of this clipped wave is the 70 MHz difference frequency. A low pass filter comprised of C38, C39 and L10 extracts the 70 MHz envelope.

(4) The 70 MHz output from the mixer applied to 70 MHz amplifier Q6 through coupling capacitor C40. This stage contains bias resistors R44, R45, R47; collector load resistor R46, and emitter bypass capacitor C42. Isolation is provided by FL4, L11 and 42. The stage is coupled to the second amplifier stage Q7 through coupling capacitor C41. The second stage is similar to the first. Dc bias is provided by R48, R49, R50 and R51. However, in the emitter circuit only R51 is rf bypassed by C43 and R50 provides negative feedback for stabilization. The collector output is taken off at tap 2 of transformer T4. The stage is decoupled from the 115 volt supply by F115 and L13. The 70 MHz output signal is applied to cable W2 through coupling capacitor C44. Cable W2 is connected to P2 (FIRE CONTROL INTERCONN) connector which supplies the 70 MHz reference signal to electronic frequency control 1A7. A metering circuit is also connected to the output of Q7, at the load side of 044. The metering circuit produces a dc signal proportional to the 70 MHz level, which is fed to the meter selector switch on meter panel assembly 1A15A8. Diode detector circuit CR9 and R.52 operates in an identical manner to the 1,50 MHz oscillator output metering circuit previously described. Ripple is filtered at the output by D14 and C46. Variable resistor R53 is used to adjust the CONT LEVEL METERING output.

### **2-35.1. Transmitter, Radio T-1054(P) A/GRC-144(V) Modulator 1A8 Circuit Functioning (fig. 5-26.1)**

Modulator 1A8 in Radio Transmitter T-1054(P)/A/MC-144(v) is basically the same as that for modulator 1A8 in Radio Transmitter T-1054(P)/CM-144(v). That is the same circuit functions are performed in both modulators and signal routing is

the same. The paragraphs below highlight the differences.

a. Modulator Circuits.

(1) The data/orderwire signal at J1 INPIT is coupled through C157 to switch BANDSET S102. Switch S102 either couples the signal straight through or through unity gain inverter amplifier Q11. At the output side of S102, the signal is connected to switch BANDSET S101 and to emitter follower stage Q10. The output of Q10 is coupled through C4 and routed through P1-8 to attenuator assembly 1A3. Switch S101 couples the signal straight through for C-band position and through 10 dB attenuator R101/R102 for K-band position. The signal at the output side of S101 is applied to the input of the baseband amplifier through the network R148, R149, R103 and C140. The input level is set at R149 to provide a modulation index of 20 MHz/volt. The output of the 3-stage baseband amplifier is coupled into the VDC stage Q103 through the baseband frequency response control network C109, R113, R117, L102. The center frequency of the VGC is controlled by a dc signal from differential amplifier A101, and the VGO is frequency modulated by the signal from the baseband amplifier.

(2) Differential amplifier A101 is driven by the frequency correction signal from frequency control 1A7 (P1-6, -7). A reference voltage derived from +15 vdc through R115, R116, C152 and CR105 is applied through R150 at A101-3. AFC disable switch S1 in the input circuit is normally open and it is used to set the output level of A101. With S1 closed, R116 is adjusted to provide an output level of +5 vdc at A101-6. The AFC signal from 1A7 is applied to differential amplifier A101 through R20 and R144. With an AFC signal applied (S1 open), the output at A101-6 varies above or below +5 V' according to the AFC error voltage. The output signal at A101-6 is applied through decoupling network R153, R118, C111, C113 and L102 to the cathodes of varactor diodes CR101 and CR102.

(3) The frequency of 150 MHz VO) Q103 is determined by resonant circuit C114, L103 and the capacity of varactor diodes CR101 and CR102. Varactor diodes CR101 and CR102 are always operated reverse biased. They exhibit an inverse square law capacitance-reverse bias characteristic, that is, the capacitance varies approximately as the inverse of the square root of the reverse bias voltage. By varying the bias voltage, or baseband input signal, the resonant frequency of the tank is made to vary. With only the bias voltage from the differential amplifier applied, the tank resonant frequency will determine the oscillator frequency. If the bias is increased the diode capacitance will decrease, causing the tank to resonate at the higher frequency. Similarly, a decrease in bias will cause decrease in the resonant frequency. Since this bias voltage represents the center frequency error, as detected in electronic frequency control 1A7, the voltage controlled oscillator center frequency follows the frequency of the reference oscillator in electronic frequency control 1A7. The center frequency is initially set during alignment by means of front panel variable capacitor C114. If a baseband signal is applied at the junction of CR1 and CR2, the frequency will be made to vary about the center frequency; thereby producing a frequency modulated 150 MHz output. Since electronic frequency control 1A7 senses the average frequency, it only corrects for center frequency drift and has no effect on the frequency modulation of the carrier. The output across load resistor R120 is applied to buffer stage Q109 through C116 and the buffer output is coupled through C119 to the input of 3-stage limiter amplifier Q104, Q105 and Q106. Diodes CR103 and CR104 limit the output level to 0 dBm +3 dB.

(4) The three stages of the limiter amplifier operate at saturation level and provide an amplitude limited output level of +28 dBm at the collector of Q106. The middle stage, Q105, has a network to provide for flat frequency response across the bandwidth. This network is comprised of the collector

load (L106, R133) and the negative feedback circuit (L105, R131, R132, C127). The output at Q106 is coupled to power amplifier stage Q108 through an impedance matching network. Power amplifier Q108 operates from a regulated +12 vdc supplied by voltage regulator stage Q107. The output at Q108 (nominal 2W) is developed across collector load L112 and coupled through frequency response control network L113, C146 and C148, through output decoupling network R154, R155 and R156 and through impedance matching network L117, C154 and C155. The output signal (150 MHz OUTPUT) is routed to frequency mixer stage 1A9 (para 2-36). A sample of the frequency modulated 150 MHz output signal is coupled through attenuator network R157, R68 and R74 to mixer transformer T3 in the frequency control circuits. This

signal is also used for output signal level monitoring and metering as described in paragraph 2-35a(4).

b. Frequency Control Circuits. Refer to paragraph 2-35b.

### **2-36. Transmitter Frequency Mixer Stage 1A9 Circuit Functioning (fig. 2-16)**

a. The transmitter frequency mixer stage mixes the 4.55 to 4.85 GHz signal from the frequency multiplier chain with the 150 MHz fm modulated signal from radio transmitter modulator 1A8 to produce the 4.4 to 5.0 GHz transmit carrier frequency. The mixer consists of crystal mixer 1A9A1 and coaxial circulator 1A9HY1.

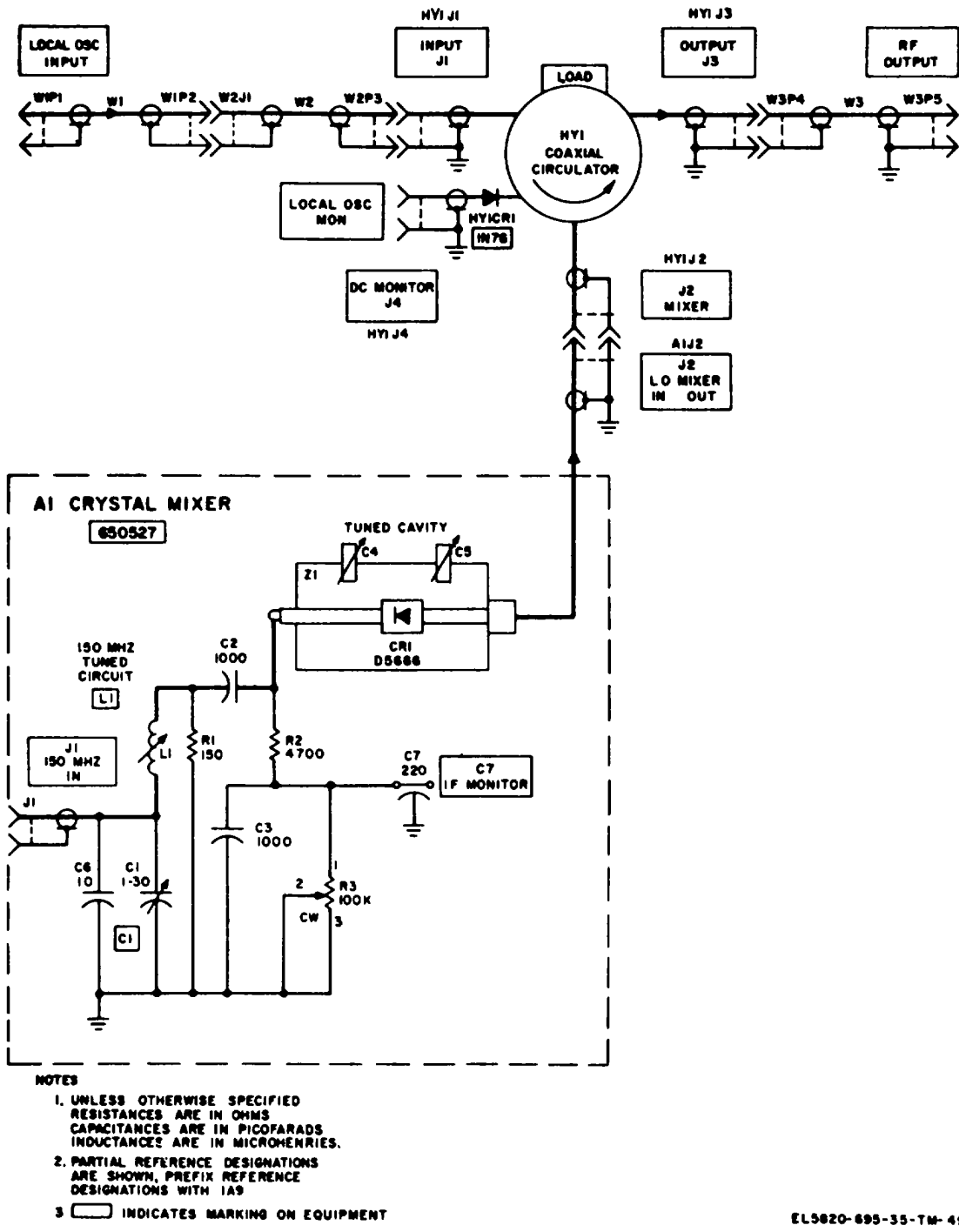


Figure 2-16. Transmitter frequency mixer stage 1A9, schematic diagram.

b. Crystal mixer 1A9A1 uses varactor diode OR1 to provide frequency conversion (due to the nonlinear capacitance-voltage relationship of the varactor diode). Resistors R<sub>e</sub> and R<sub>3</sub> provide bias return for CR1. The 1,50 MHz fm signal is applied to jack J1 and is coupled to the mixer cavity through

resonant circuit L1, and C1, C6. This circuit is tuned to the 15) MHz if frequency and is used to tune out the varactor capacity at the if frequency. Isolation of rf from the if cir-

ducts is accomplished by a quarter-wave choke in the tuned cavity. Two tuned stubs CA and CA suppress the fundamental LO frequency. The resulting sidebands are reflected out of the diode cavity Z1 and enters coaxial circulator 1A9HY1 at port No. 2 (J2).

c. The coaxial circulator has a bandpass from 4.4 to 5.0 GHz with a maximum insertion loss of 0.6 db (port 2 to port 3). This is a four-port coaxial circulator with a resistive termination at port 4. The reflected sidebands enter the circulator at port No. 2 (J2) and leave at port No. 8 (J3). A tunable bandpass filter is connected at port No. 3 and is tuned to the desired sideband which is passed by the filter. The unwanted sideband is reflected back to port No. 3 of the circulator which couples it to the dummy load at port 4.

d. A diode type amplitude detector is incorporated in the circulator for monitoring the local oscillator chain pass band shape. The monitor dc output is taken from Connector J4.

### **2-37. Transmitter Frequency Multiplier Group 1A10 Circuit Functioning (fig. 2-17)**

a. Transmitter frequency multiplier group 1A1010 multiplies the 113S75 to 121125 M local oscillator frequency by four. The 4.55 to 4.85 GHz output frequency is at a level of 1.7 watts (minimum) and is applied to transmitter frequency mixer stage 1A9. The transmitter frequency multiplier group consists of transmitter 2nd stage frequency multiplier 1A10A1 (times 2), 22752425 KMHz e-v-i-l circulator 1A10HY1, and transmitter 3rd stage frequency multiplier 1A10A2 (times 2).

b. The input signal to transmitter 2nd stage frequency multiplier 1A10A1 is applied to the low-pass filter consisting of C1, L1 and C2. Variable capacitor C1 provides impedance matching at the input. Series variable capacitor C3 provides impedance matching to the varactor diode impedance (typically 1-10 ohms). The varactor diode is a step-recovery type. The step recovery diode stores a charge as it conducts in the forward direction; when the applied voltage is reversed the diode will conduct for a brief period in the reverse direction until the stored charge is removed, conduction then ceases abruptly. The abrupt step in current through the diode produces a waveform that is rich in harmonic power.

The 2nd harmonic of the incoming frequency is selected by tuned coaxial cavities Z11 and Z2A. These cavities

are resonant lines, with tuning provided by a plunger and the input and output coupling is provided by adjustable probe

c. Coaxial circulator 1A10HY1 isolates the transmitter 2nd stage frequency multiplier from the transmitter 3rd stage frequency multiplier. The input (J1 INPUT) and output (J2 OUTPUT) impedances are 60 ohms resistive. The monitor output (J3 DC MONITOR) provides a sample of the transmitter 2nd stage frequency multiplier output signal level to the meter selector switch on meter panel assembly A15AS. The insertion loss for the circulator is 0.3 db maximum

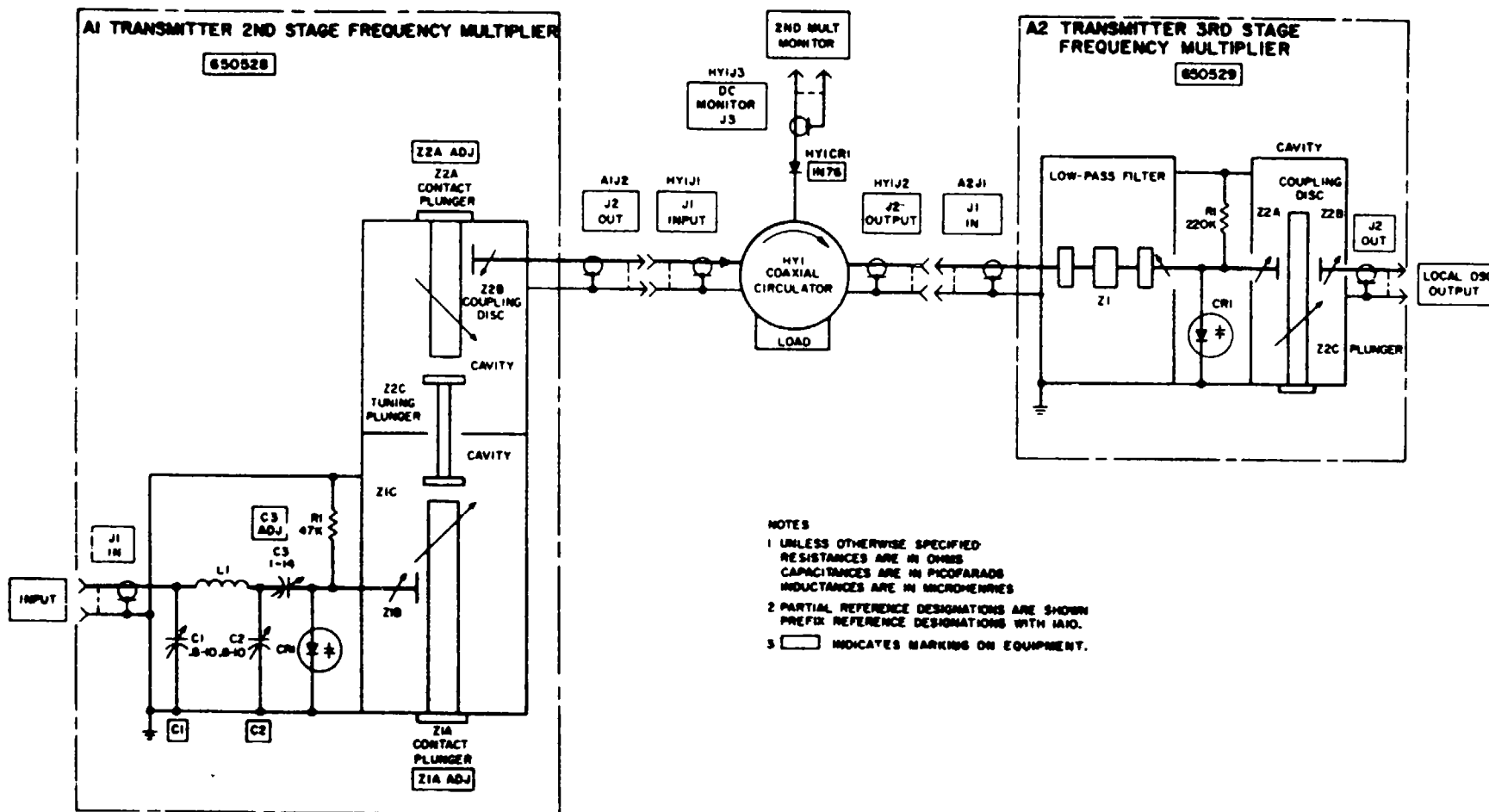
d. Transmitter 3rd stage frequency multiplier 1A10A2 functions in a similar manner to the transmitter 2nd stage frequency multiplier. However since the frequencies are higher, the input signal is coupled to the Varactor diode by a tuned cavity and the second harmonic output is selected by a single coaxial cavity. Tuning the coaxial cavity is provided by adjustable probes

### **2-38. Transmitter Amplifier-Frequency Multiplier 1A11 Circuit Functioning (fig. 5-27)**

The transmitter amplifier-frequency multiplier amplifies and multiplies (times 4) the 2848-375 to 303.125 (20 milliwatts, nominal) input signal to a 1137.5 to 1212.5 MHz (8 watts, nominal) output signal. Transmitter amplifier-frequency multiplier 1A1-1 is comprised of a 300 to 600 MHz doubler, 600 MHz amplifier, isolator, and a 600 to 1200 MHz frequency doubler.

a. *300 to 600 MHz Frequency Doubler.* The 284.375 to 303.125 Hz signal from electrical frequency synthesizer 1A.14 is applied to the primary of transformer T1. The secondary of T1 is connected to the anodes of diodes CR1 and CR2. This circuit is, in effect, a full-wave rectifier, in which CR1 and CR2 alternately a half cycle of the input signal. Therefore, the output frequency (568.760 to 606.250 MHz) is twice the input frequency. The 568.750 to 606.250 MHz signal is coupled to the base of Q1 in the 600 MHz amplifier circuit through capacitors C1 and C51. Conductor 12 is used in conjunction with C1 and C51 to filter out the 300 MHz component of the signal that appears at the output of the full-wave rectifier. R1 is a dc load resistor and inductors L1 and LA are rf chokes.

b. *600 MHz Amplifier.* The 600 MHz amplifier includes transistor stages Q1 to Q4



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Figure -17. Transmitter frequency multiplier group 1A10, schematic diagram

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Transistor stages Q1 and Q2 are low level amplifier stages which operate class A. Adjustable resistor R24 permits varying the emitter bias of Q2, thereby adjusting the gain. Capacitors C3, C4, C10, and C11 are emitter bypass capacitors. Dc bias for the base circuits of Q1 and Q2 is provided by R3, R4, R8, and R9. Dc bias for the emitter circuits of Q1 and Q2 is provided by R5, R10, R24, and R25. Capacitors C2, C5, C8, and C12 are feed-through bypass capacitors for the +28 vdc power supply input. Capacitors C20, C52, C53, C9, C64, and C55 are used to tune the base circuits of Q1 and Q2. The low output appears at the collector of Q2 and is coupled to the base of Q3 through L9, C14, and C13. Transistor stages Q3 and Q4 are driver stages which operate class C. Capacitors C15, C47, C59, C19, C61, and C62 are used to tune the base circuits of Q3 and Q4. Inductor L12 and capacitor C17 match the collector of Q3 to the base of Q4. The output of Q4 is coupled to power amplifier stages Q5 and Q6 through matching section L16, L14, C22, C23, and R29 and coaxial cable W6. Two quarter wave (72 ohms) sections (W1 and W2) form a power divider which divides the Q4 output and provides isolation between the power amplifier stages. L17, C24, and L18, C27 are used to match the output of quarter wave sections W1 and W2 to the base circuits of Q5 and Q6. Resistors R17 and R20 provide a path for the unbalanced currents in the base and collector circuits of Q5 and Q6. Power amplifier stages Q5 and Q6 also operate class C. Their outputs are fed through matching networks to an output hybrid consisting of quarter wave sections (72 ohms) W3 and W4. C30, L23, C32 and C31, L24, C33 match the collector output of Q5 and Q6 to the hybrid (W3, W4). The output hybrid combines the Q5 and Q6 outputs and also provides isolation between the Q5 and Q6 output circuits. The 568.750 to 606.250 MHz (18 watts, nominal) output is fed to the 600 to 1200 MHz frequency doubler stage through cable W6.

c. 600 to 1200 MHz Frequency Doubler. This stage multiplies (times 2) the 568.750 to 606.250 MHz signal up to 1137.6-1212.5 MHz. The frequency doubling action is achieved by varactor diode CR3. The input circuit consists of capacitors C34, C35, C46, and inductor plates L25 and L26. Resistor R22 provides stabilization and is also the dc return for CR8. The input circuit is tuned to the 568.750 to 606.250 MHz input signal. The output circuit of C36, C38, and L27 is tuned to the second harmonic of the input frequency and the 1137.5 to 1212.5 MHz output signal (8 watts, nominal) appears at the J5 OUTPUT connector.

## 2-39. Digital Data Modem 1A12 Circuit Functioning

Digital data modem 1A12 contains the plug-in components and chassis mounted components which provide the signal interface between Radio Set AN/GRC-144 and the cable equipment. Also, the circuits in digital data modem 1A12 complete a direct, current path between the cable input terminal and the cable output terminal. The following paragraphs describe circuit operation of chassis mounted components that are not discussed in paragraph 2-5 and 2-6. The direct current path is described in paragraphs 2-5d and 2-e. Electrical operation of discrete piece parts for the plug-in components is described in paragraphs 2-40 through 249. The complete functional description of the plug-in components is provided in paragraphs 2-5 and 2-6. Refer to paragraph 2-4 for the meaning of the signal mnemonics. The chassis mounted component connections are shown in digital data modem A12 interconnecting diagram (fig. 528). The chassis mounted components provide signal interface between the plug-in components, selection and indication of operating modes, filtering of signals, and power distribution.

a. Capacitors 1A12A12A1TB2C15 through C23 and capacitors 1A12A12A1TB2C37 and C38 filter noise from the alarm monitor signal lines. Capacitors 1A12A12A1TB2C26 and C28 through C32 filter the orderwire signals. Capacitors 1A12A12A1C36 and J.A12A12A2C34 provide input bandwidth control for 1A12A1 and 1A12A11. Capacitors 1A12A12A1TB2C33 and C35 filter the +5v supply to 1A12A1 and 1A12A11. Capacitors 1A12A12A1TB2C24 and C25 are not used. Resistor 1A12A12A2R2 is a voltage dropping resistor in series with level adjustment resistor 1A12A12A2R1.

b. The ADDM TRAFFIC SELECT switch 1A12A12A1S2 is not used in the synchronous mode of Radio Set ANIGRC-144. In the asynchronous mode, it is used to select either the 48-channel or the 96-channel data rate. To accomplish this, it supplies logic 1 (+6v) and logic 0 (ground) signals to the baud generator and pcm retiming circuits of radio control comparator 1A12A9. To make switch 1A12A12A1S2 operative in the asynchronous mode and inoperative in the synchronous mode, the logic signals from the switch are routed through jumper (interlock) connections on plug-in component 684092

(1A12A10). This plug-in component is used only in the asynchronous mode. In the synchronous mode, plug-in component 683696 is used in chassis position A10. This plug-in component does not have the corresponding jumper connections and when it is in place the switch is not connected. Terminals 1 and 6 of switch S2 are connected to ground; terminals 3 and 4 are connected to +5vdc (via terminal 20 of 1A12A12A1TB2). The moveable arms, terminals 5 and 6, of the switch connect these voltages to pins 8 and U of plug-in component 1A12A10. In the asynchronous mode, plug-in component 684092 is in use and the internal jumpers route the input signal at pin 8 to output pins N and 7, and route the input signal at pin U to output pin R. Pins N, R and 7 of 1A12A10 then supply the required logic signals to input pins 4, 5, 9 and 10 of 1A12A9. The position of the ADDM TRAFFIC SELECT switch determines which inputs receive logic 1 and which logic 0. See paragraph 2-6b.1.

c. The power distribution bus on 1A12A12TB3 connects the power supply voltages to the various plug-in components in digital data modem 1A12. Capacitors 1A12A12A2TB1C5, C7, C9, C11, and C13 provide rf filtering of the power lines; capacitors 1A12A12A2TB1C6, C8, C10, C12, and C14 provide filtering of low frequency transients. All the ground lines from each plug-in module terminate at the common ground bus on terminal board 1A12A12TB3. This bus is connected to chassis ground by a ¼4-inch braid and a lug connected to the top rear of the case. Resistors 1A12Ai2A2R13 and 1A12A12A1R14 are isolating resistors that connect the modulation input voltages (RVCOI and CVCO) to test points TP6 and TP7. The signal ground for modules 1A12A1 and 1A12A11 is pin 3; the case ground connection is provided at pin 7. Resistors 1A12A12A2TB1R5 through R9 are isolating resistors that connect supply voltages to test points TP1 through TP5. Resistor 1A12A12A1TB2R11 limits current from the +5v power supply when switch 1A12A12A1'1 is in test position. Resistor 1A12A12A1TB2R12 is not used.

d. Indicator lamps 1A12A12A2DS1 through OS4 illuminate in response to the jumper plugs that are inserted onto printed wiring boards 1A12A2 and 1A12A10. The +5 volt power supply potential is connected to one side of the selected cable length indicator lamp by the jumper plug inserted into cable digital regenerator 1A12A2. The +5 volt power supply return is connected to the other side of the selected cable length indicator lamp by the jumper plug inserted into radio digital processor 1A12A10. The selected cable length indicator lamp will light provided that the

same cable simulation networks are connected at each board.

#### **2-40. VCO 1A12A1, 1A12A11 and 1A12A18 Circuit Theory**

Voltage-controlled oscillators 1A12A1 and 1A12A11 are sealed units that produce a frequency-stable squarewave timing signal at a frequency of 4608 kHz. They are used only in the synchronous mode. In the asynchronous mode, voltage controlled oscillator 1A12A18 is used. Its frequency is 9830.4 kHz. Chassis position 1A12A1 has a blank panel. The frequency can be adjusted by means of a manual control to permit compensating for the frequency effects of aging. The output impedance is 470 ohms.

#### **2-41. Cable Digital Regenerator 1A1 2A2 and 1A12A 13 Circuit Theory (fig. 5-30 and 5-30.1)**

The integrated circuits used on cable digital regenerator 1A12A2 and 1A12A13 are shown functionally in figure 5-30 for the synchronous mode and in figure 5-30.1 for the asynchronous mode. Figures 5-30 and 5-30.1 also specify each integrated circuit type. Figure 5-24 provides a circuit diagram for each type of integrated circuit used in Radio Set AN/GRC-144. The complete functional description of cable digital regenerator 1A12A2 is provided in paragraph 2-5a (synchronous mode) and for 1A12A13 in paragraph 2-5a.1 (asynchronous mode). Electrical operation of discrete piece parts not discussed in paragraphs 2-5a and 2-5a.1 is provided in a through below.

a. *Cable Simulation Networks.* The cable simulation networks consists of three ¼4-mile sections. Selection is provided by plug P2. Resistors R1 through R7, capacitors C2, C3, and inductor L4 form on-4-mile network; R8 through R14, C4, C5, and L5 form a second network, and R15 through R21, C6, C7 and L6 form the third network. For example, if the cable length is ¼4 mile, set the plug connections to Y4 mile. With the arrangement three simulated ¼4 mile networks are in series with the input ¼4 mile of cable providing a total equal to one mile of physical cable.

#### *b. Amplifiers.*

(1) Amplifier Q1 is a grounded emitter voltage amplifier with a peaked response at 2304 kHz, due to tuned network R26, R22, C10 and L8. The signal input to amplifier Q1 is through

transformer T1 which provides a voltage gain of two. The +12 volt supply voltage is connected to transistor Q1 through voltage dropping resistor R27 which is bypassed by capacitor C8. Capacitor C9 is a high frequency bypass that provides signal ground for the tuned circuit. Resistors R24 and R25 in the emitter circuit of transistor Q1 provide dc bias. Resistor R25 is bypassed for ac by capacitor C12. Since resistor R24 is not bypassed, it provides a small amount of signal (ac) feedback. Resistor R23 is an impedance match for the secondary of transformer T1 because the input impedance of Q1 is high. Resistor R33 at the secondary side of transformer T2 has the same function. Cable traffic alarm signal XCPCM is taken from the secondary of T1 and sent to alarm monitor 1A12A6.

Resistor R46 is an isolating resistor to protect T1 and Q1 in the event of a malfunction in the external circuit.

(2) Amplifier Q2 is a grounded emitter amplifier with a voltage gain of approximately 35. The input signal to this amplifier is direct coupled from transistor Q1. Resistor R28 is the collector load resistor and resistor R29, R30, and R31 provide dc bias. Resistors R30 and R31 are bypassed for ac by capacitors C11 and C13. Resistor R29 is not bypassed and provides a small amount of signal feedback. Dc feedback from the junction of resistors R30 and R31 to the base of transistor Q2 provides temperature compensation between transistors Q1 and Q2.

(3) Amplifier Q3 is an emitter follower which couples the output signal of transistor Q2 to the primary windings of transformer T2 with minimum loading on transistor Q2. Resistor R32 is the emitter load resistor. The ac signal is coupled to transformer T2 through capacitor C14. Transformer T2 provides a voltage gain of four.

(4) Dual transistor circuit Q5 contains a common emitter amplifier Q5A and a temperature compensating bias network consisting of Q5B, resistor R34 and bypass capacitor C15. This type of biasing results in a linear output which is direct coupled to the input (pin 2) of slicer A1. Resistor R35 functions as the collector load resistor. Resistor R36 provides dc bias and is bypassed for ac by capacitor C16.

(5) Amplifiers Q7 and Q8 are a pnp-npn common-collector complementary pair designed to eliminate temperature drifting effects. Resistors R37 and R40 are the emitter load resistors. Resistor R38 is a current limiting resistor to protect Q8 against current surges, at turn on time or any time when C17 is discharged. The signal at the base of Q8 is rectified by the base emitter junction to provide a dc reference in

direct proportion to the signal level at the base, and is filtered by C17. Resistor R39 provides a minimum voltage across C17. This reduces the time required for input pulses to fully charge C17. Resistor R40 is variable so that the dc input level to the reference input of A1 can be adjusted.

c. *Slicer A1* Slicer A1 is an integrated circuit (fig. 5-24). Capacitors C18 and C19 provide supply voltage decoupling. The -6 volts through resistor R41 speed up transitions from logic one to logic zero. When the input signal (pin 3) is more positive than the reference voltage (pin 2), the output is low (logic zero); when the input signal is negative with respect to the reference voltage, the output is high, (logic one).

d. *Integrator and Lamp Driver.* The integrator (transistor Q9) is an emitter follower. Resistors R42 and R43 and capacitor C20 determined the base emitter bias. Pulses of 1CSPCM charge capacitor C20 and maintain a positive dc voltage as long as signal 1CSPCM is active. The output voltage is coupled through current limiting resistor R44 and keeps transistor Q10 (which acts as a switch) turned on. Lamp DS1 then remains lighted as long as 1CSPCM activity continues. If the pcm signal fails, Q9 turns off, capacitor C20 discharges through R43 and Q10 turns off. Output signal 1CRFAIL is then logic one and lamp DS1 is off. When transistor Q10 turns off, lamp DS1 receives a small current to keep it warm through R45. Since a warm lamp has a higher resistance than a cold lamp, when Q10 turns on, the current surge is not as great.

e. *Voltage Filtering Components, Synchronous Mode (1A12A2).* Voltage filtering components L9 through L11 and C21 through C25 limit the coupling of switching transients and other stray signals to the power circuits.

f. *Voltage Filtering Components, Asynchronous Mode (1A12A13).* Voltage filtering components L13 and C26, C27, and C30 (for the +5 vdc supply voltage) and L15, L16 and C29, C33, and C34 (for the +6 vdc supply voltage) limit coupling of switching transients and other signals to the power circuits. The +12 vdc supply voltage is filtered at the input by L1 and C1, voltage regulated by R1 and CR1 and filtered by C2. It is then distributed to various circuits through decoupling circuits as follows: 1. through L2 and C3 and C4 to integrated circuit A4 and transistors Q1 and Q2; 2. through L8 and C25 to transistor Q4; 3. through L3 and C8 to integrated circuit A1; 4. through L14 and C28 to integrated circuit A3.

## 2-42. Cable Control-Comparator 1A12A3 and 1A12A14 Circuit Theory (fig. 5-31 and 5-31.1)

The integrated circuits used on cable control comparator 1A12A3 are shown functionally in figure 5-31 for the synchronous mode and for 1A12A14 in figure 5-31.1 for the asynchronous mode. Figures 5-31 and 5-31.1 also specify each integrated circuit type. Figure 5-24 provides a circuit diagram for each type of integrated circuit used in Radio Set AN/GRC-144. The complete functional description of the cable control comparator is provided in paragraphs 25b for 1A12A3 and 2-5b.1 for 1A12A14. Electrical operation of discrete piece parts for the synchronous mode is provided in a through g below, and for both modes in h.

a. *Flip-Flops.* The J and K inputs of flip-flops A7A and A7B are maintained at logic one by connection to the +5 volt supply voltage through resistors R1 and R15.

b. *Positive Pulse Generator.* When 1PP is logic zero (ground) diode CR1 is forward biased and the emitter of transistor Q1 is at logic zero (approximately +0.7 volt). Voltage division in resistor R3 and diode CR6 provides the +1.4 volts at the base of Q1. Capacitor C4 filters this voltage. Transistor Q3 has -1.4 volts at the base which is provided by a voltage divider consisting of resistor R9 and diode CR7. The voltage is filtered by capacitor C5. With transistor Q1 off, -12 volts through resistor R4 forward biases Q3. Current flow from +12 volts through resistor R5, Q3 and resistor R4 to -12 volts produces voltage drops that make the voltage at the collector of Q3 negative. Diode CR5 clamps this voltage at -0.7 volt. This is the low voltage output of the positive pulse generator. When 1PP is high, diode CR1 is reverse biased. Transistor Q1 is forward biased by the positive voltage through resistor R2 and its emitter is at approximately +2 volts. When Q1 is on, current flow from +12 volts through R2, Q1 and R4 to -12 volts produces voltage drops that make the voltage at the collector of Q1 positive. This voltage is clamped at +0.7 volt by diode CR2. This is the voltage at the emitter of Q3, therefore, Q3 is reverse biased. With Q3 off, current flow from +12 volt through R5, diode CR3 and zener diode CR4 to ground drops the voltage at the collector of Q3 to +5 volt. This voltage is determined by the clamping action of diode CR3 and zener diode CR4. Zener diode CR4 is protected against current surges by capacitor C1. Resistor R6 provides additional current flow through zener diode CR4 to assure that the diode is operating at its specified current rating to assure the specified zener

voltage rating. The +5 volt output signal is coupled to integrator A8 through diode CR12B and resistor R7.

c. *Negative Pulse Generator.* When 1NP is logic one (approximately +3.5 volt), diode CR8 is reverse biased, and Q2 is forward biased by +12 volts through R10. Current flow from -12 volts through R11, Q2 and R10 to +12 volts makes the voltage at the collector of Q2 positive which is clamped at -0.7 volt by diode CR11. This is the low voltage output of the negative pulse generator. When 1NP is logic zero (ground), diode CR8 is forward biased, the emitter of transistor Q2 is at +0.7 volt and Q2 is reverse biased. With Q2 off, current flow from -12 volts through resistor R11, diode CR9 and zener diode CR10 drops the voltage at the collector of Q2 to -5 volts. This voltage is determined by the clamping action of diode CR9 and zener diode CR10. The functions of resistor R12 and capacitor C6 are the same as for resistor R6 and capacitor C1 (b above). The -5 volt output signal is coupled to differential integrator A8 through diode CR12A and resistor R13.

d. *Differential Integrator.* The differential integrator is composed of capacitors C2, C3, C7, C8, C9, resistor R14 and differential amplifier A8. Capacitor C2 is a high frequency bypass. Capacitor C3 provides band-width limiting to prevent oscillation. Capacitors C7 and C8 are supply voltage decouplers. Resistor R14 and capacitor C9 form a long time constant signal feedback path. The feedback signal maintains the output signal and bridges over intervals when the positive and negative pulse inputs are both absent. Resistor R8 is an isolating resistor to couple the signal to test point E14.

e. *Positive/Negative Clamp Detector.* Resistors R22 and R25 form a voltage divider which provides +0.75 volt as the reference voltage for the positive clamp detector. Similarly resistors R26 and R27 provide -1V for the negative clamp detector. Resistors R21, R23, and R24 form a voltage divider that couples the signal output of A8 into the clamp detectors. The tapoff point at the center arm of resistor R23 is connected to the inputs of both clamp detectors and is bypassed by capacitor C15.

f. *Narrow Clock Pulse Generator and 48-Channel Baud Generator.* Resistors R16 and R17 connect the supply voltage into pin 13 of narrow clock pulse generator A5. Variable resistor R17 and capacitor C10 set the time constant which determines the time duration of the

negative pulse output signal. Capacitor C1 is a supply voltage filter. The functions of capacitors C12 and C13 and resistors R18 and R19 at 48-channel baud generator A1 are similar to the functions of corresponding parts at A5.

*g. Lamp Driver.* The -6 volt supply voltage through resistor R28 speeds up transitions from high (logic one) to low (logic zero) at the input of A10C. Resistor R29 provides a current to keep lamp DS1 warm when the output of A4A is high. When the output of A4A returns to low, the current surge through A4A is not as great due to the lamp warming current.

*h. Voltage Filtering Components.* In the synchronous mode (1A12A3) voltage filtering components (L1 through L4 and C17 through C24) limit the coupling of switching transients and other stray signals to the power supply circuits. The +6 volt supply for A8 is derived internally by dividing the +12 volt supply voltage. This is accomplished by resistor R20 and zener diode CR13. This voltage is filtered by capacitor C14. In the asynchronous mode (1A12A14), the +5vdc supply voltage is filtered by L1 and C3, C4 and C5.

#### **2-43. Cable Digital Processor 1A12A4 Circuit Functioning (fig. 5-32)**

Cable digital processor 1A12A4 contains integrated circuits designated A1 through A6. Figure 5-24 provides a diagram for each type of integrated circuit used. The complete functional description of cable digital processor 1A12A4 is provided in paragraph 2-5c. Electrical operation of discrete piece parts is provided in subparagraphs below.

*a. Level Converters.* Resistors R1, R2, and R3 of level converter 1 are voltage dividing resistors that also provide impedance matching for the 1TRPCM output signal. The logic zero output is 0 volts to 0.5 volt at 15.5 ohms impedance. The logic one output is 1.5 volts at 22 ohms impedance. In level converter 2, resistors R9, R10 and A11 perform a similar function for signal 1RRPCM.

*b. Alarm Circuits.* In alarm circuit 1, resistor R7 connects the +5v supply to A6 and capacitor C5 is a supply voltage filter. Resistor R4 and capacitor C4 determine the time constant for monostable multivibrator A6 and thus determine the duration of the logic one output (pin 8) when the input (pin 1) goes negative. If the pcm signal is active, this occurs constantly and the output of A6 remains at logic one

(+5v). The output signal from A6 is coupled to the base of Q1 through bias resistor R8. When the output from A6 is +5v, Q1 is turned on and output signal 1CRLFAL is logic zero (normal). Lamp DS1 is lighted because it has a ground connection through Q1. When the pcm signal fails, A6 times out and the output signal at pin 8 returns to 0v. Q1 is turned off and output signal 1CRLFAL is logic one (alarm condition). Lamp DS1 is turned off but it has a quiescent current through resistor R5 which keeps the filament warm. This reduces the current surge through Q1, when Q1 and DS1 turn on.

*c. Voltage Filtering Components.* Voltage filtering components L1 and C1, C2 and C3 limit the coupling of switching transients and other stray signals to the power supply circuits.

#### **2-44. Alarm Monitor 1A12A5 and 1A12A15 Circuit Theory (fig. 533 and 5-33.1)**

The integrated circuits used in alarm monitor 1A12A5 and 1A12A15 are shown functionally in figure 5-33 for the synchronous mode and in figure 533.1 for the asynchronous mode. Figures 533 and 533.1 also specify each integrated circuit type. Figure 6-24 provides a circuit diagram for each type of integrated circuit used in Radio Set AN/GRC-144. The complete functional description of the alarm monitor is provided in paragraphs 2-5f and g and 2-6h and i. Electrical operation of discrete parts not discussed in paragraphs 2-5f and g and 2-6h and i is provided in a, b, and c below which apply specifically to the synchronous mode (1A12A5); however, they apply also to the asynchronous mode (1A12A15) since the only change is that the reference designators of the logic circuits are different. The cable traffic detector is discussed in d (1A12A5) and d.1 (1A12A15) below. The circuit description for voltage filtering components in the asynchronous mode (1A12A15) is similar to that provided in e below for the synchronous mode (1A12A5).

*a. Lamp Drivers.* The lamp driver circuits conduct 40 ma. to operate the 28 vdc lamps with standard logic inputs. Each circuit is a simple npn transistor inverter with a series 150 ohms collector current limiting resistor (required to limit the current surge because of a cold filament when turning on the lamp). When the input is a standard logic one, the transistor is saturated and the lamp driver provides maximum current (40 ma.). When the input is a logic zero, the transistor is cut off and the output is open (equal to lamp supply voltage).

(1) Lamp drivers Q1, Q3 and Q9 have a resistor in series with the transistor base. The resistor serves to limit the base current of the transistor and reduce the loading on the logic circuit that controls the transistor.

(2) Lamp drivers Q2, Q4, Q8 and Q11 have +5v connected to the base through a resistor, in addition to the logic signal connection. This is called a base pull-up resistor. It is required because the inverters that supply the logic signal to the base do not have the capability to supply enough base drive current in the logic one state. When the output of A3A is low, the +5v is dropped across R3 and Q2 is off. When the output of A3A is high (+5v), R3 supplies additional drive current to the base of Q2 to assure turn-on. Operation of lamp drivers Q4, Q8 and Q11 is the same.

(3) Inverter A3E drives A2A, A3F, and A4C in addition to Q10, so a base pull-up circuit is required at Q10 for either logic state of A3E. When the output of A3E is low, CR6 is forward biased and current flow through R24 and CR6 drops the voltage at the junction point of CR6, CR7 and R24 to +0.7v. Current flow through R25, CR8 and CR7 drops the voltage at the base to -1.4v and Q10 is off. When the output of A3E is high (+5v), CR6 is reverse biased. Current flow through R25, CR7, CR8 and R24 drops the voltage at the base to approximately +2v and Q10 turns on.

b. Relay Driver. Relay driver Q7, which generates the bypass orderwire 1BPOW signal, has the cathode of CR4 connected to its output, with the anode returned to ground. Diode CR4 is a 27-volt zener diode which provides protection against normal transient voltages generated by the relay. The components associated with the circuit are: CR2, R16, CR3, R17, C2, Q7, CR4 and R18. The components (R16, R17, CR2 and CR3) are used to convert the logic input signal into a base turn-on, turn-off signal. Capacitor C2 prevents the relay from following a transient (false) alarm input. Resistor R18 is a current limiting resistor. When the input signal to Q7 is logic one (high), CR2 is reverse biased. Electron flow from ground through C2, CR3 and R16 to +5 volts charges C2 and turns on Q7. When the input signal changes to logic zero (low), CR2 is forward biased. Electron flow is then from the cathode side of CR2 to the positive voltage and also from negative voltage and through R17 to C2, and from ground through Q7 emitter and base to CR3. This delays the turn-off of C2. With C2 discharged, the negative voltage through R17 has two paths, through

CR3 and through C2 to ground. As soon as C2 is discharged Q7 turns off. C2 continues to charge with negative polarity on the side connected to the base of Q7. When the input goes high, this reverse voltage on C2 must be discharged before it can be recharged with positive polarity. Thus, turning on Q7, which occurs after a failure has been corrected, is slow, and turn-off, which occurs when the failure is detected, is also delayed. This allows Q2 to maintain an on or off condition with interruptions in either state.

c. Integrator Driver. The integrator driver Q5, Q6 consists of the following components: R10 R15, CR5, R11, R12, C1, R13, R14. The input network (R10, R11, R12, R15, and C1) is comprised of a level converter and integrator for the driver circuit. The output of the integrator the base of Q5 which, in turn, controls transistor Q6. Resistor R14 provides current limiting to transistor Q6. There is no inversion of an input signal and a logic one input will become +28 volts at the output; a logic zero input will become zero volts. The output major alarm summary signal (OMARY) is integrated to prevent a false input from triggering this major alarm output. When the input signal (from A3D) is high, electron flow from -6 volts through R11, CR5 and R15 and R10 produces a positive voltage at the junction of CR5 and R11 because most of the voltage is dropped across R11. C1 charges to this positive voltage and turns on Q5. Resistor R14 is a current limiter. With Q5 at saturation, Q6 has zero volts at the base and is off. When the input changes to low (ground), the positive charging voltage is removed from C2 and it discharges. When the voltage at the cathode side of CR5 goes negative (as C1 discharges), Q5 is reverse biased and turns off. The positive voltage through R13 then turns on Q6 and the output signal major alarm summary (OMARY) is logic zero.

d. Cable Traffic Detector, Synchronous Mode (650545).

(1) The cable traffic detector consists of four sections: cable traffic amplifier AS, 2304 KHz crystal with slicer bias and dc tracking network Q13A and Q13B, slicer comparator A6, and transistor integrator Q12. The cable traffic input signal XCPCM to the traffic detector is ac coupled to the input of high gain amplifier AS. Amplifier AS drives crystal Y1 which resonates at 2304 KHz (nominal pcm cable component); the two transistors, Q13A and Q13B, provide bias (Q13B) and dc tracking with temperature (Q13A). The components used in the bias network are: R37, C13, Q13B, R39, C14 and R38. The

parts used to attain dc temperature tracking are: R33, C9, Q13A, R34, R35, R36 and C10.

(2) The output of the dc temperature tracking circuit is added to the crystal output. This composite signal is fed to the noninverting input pin 2 of the comparator A6 while Q13B bias is applied to the inverting input pin 3. The output of the comparator will be low for small amounts of cable traffic, due to the 10% offset supplied by R34 and R36 (in the dc tracking network). When the traffic is normal the comparator output will be switching and turn on the transistor integrator (R32, Q12 and C8). The integrator will allow small gaps in the pcm cable signal to go undetected by the alarm gating circuits.

(3) Cable traffic amplifier A5 is a high gain video amplifier. The supply voltage at pin 9 is derived by dividing the +12 volts supply through resistor R29 and zener diode CR9. This voltage is filtered by capacitor C6. It is also the collector voltage for Q13. Capacitor C17 determines the low frequency cutoff and C18 determines the high frequency cutoff. Capacitor C5 and resistor R30 form a high pass filter. Dc blocking capacitor C7 isolates the high pass filter so that dc voltage at pin 1 of A5 is not changed. The cable traffic signal from cable digital regenerator 1A12A2 is amplified by A5 and the output signal is connected to crystal filter Y1 and to Q13A and Q13B. Crystal filter Y1 offers a low impedance to a very narrow frequency band centered at 2304 kHz and a high impedance outside the passband. Thus, the signal at the output side of Y1 is the pcm signal minus most of the noise and transients. Q13A and Q13B are emitter followers which pass the pcm signal to the inputs of A6 but in the process they generate an average dc bias from the signal. Q13A has a high frequency cut off at the input comprised of R33 and C9. Q13B has a similar input circuit, R37 and C13, but it has a higher cut-off frequency and thus, Q13B passes more high frequencies than Q13A. The emitter load resistance of Q13A is R34 and R36. Since the output is coupled to A6 through isolating resistors R35 and R31, only 90% of the output signal of Q13A is used. The emitter load resistance of Q13B is R39. Capacitor C10 and C14 become charged to the average dc level of the input signal and determine the dc level about which the pcm signal varies. The dc level of the signal at E13 is lower than the dc signal at E14 because the output taken from Q13A is only 90% of the available signal. The pcm signal at E13 is greater than at E14 because of the signal coupled through Y1. This is the

condition that exists when the pcm (cable traffic) signal is present. The voltage at E13 then alternately exceeds and falls below the voltage at E14 and the output (pin 7) of A6 switches from high to low at the pcm rate. This signal coupled through isolating resistor R32 alternately turns Q12 on and off. When Q12 is off, C8 charges to a plus voltage and when Q12 is on, it discharges through Q12. Thus, when the pcm (cable traffic) signal is present, Q12 switches on and off and prevents C8 from holding a charge (logic one). The source of the charging voltage for C8 is in A3E. When the pcm signal is absent, the signal inputs to A6 at E13 and E14 are determined by the noise and transients, but no switching takes place. C8 can then charge up until its output is logic one (high).

*d.1. Cable Traffic Detector, Asynchronous Mode (684091).* The cable traffic detector comprises a differential amplifier, integrated circuit A1, and a voltage comparator, integrated circuit A2. The +12 vdc supply voltages for A1 and A2 are filtered by L4 and C8 (A1) and L6 and C18 (A2) and the -6vdc supply is filtered by L7 and C19 (A2). Bias voltage for the input circuits of A1 is provided by voltage divider R29 and R30; the voltage is applied to input pins 1 and 3 through isolating resistors R31 and R32. Tune-a circuit L8 and C7 determines the bandwidth of the input circuit of A1. Bias voltage for the input circuits of A2 is provided by voltage divider/filter networks R38, R41 and C10 (pin 3) and R39, R42 and C13 (pin 2).

(1) The input signal to A1 is capacitively coupled through C5 and C6 which also isolate the dc bias of the input circuit from the external circuit. When the signal voltage (XCPCM) at pin 1 goes more positive than the bias voltage, the output at pin 7 goes positive and remains positive until the input signal falls below the bias level. At this time the signal at pin 2 is negative with respect to the bias and there is no output at pin 6. When the input signal is negative-going at pin 1, the signal at pin 2 is positive-going and a positive pulse output is produced at pin 6. In the output circuit of A1, the cathodes of diodes CR9 and CR10 are connected to a fixed dc voltage provided by voltage divider R34-R35. Because of the positive bias voltage at the cathodes, diodes CR9 and CR10 rectify only the upper half of the positive pulse outputs from pins 6 and 7 of A1. The resulting current pulses in resistor R35 produce positive voltage pulses at the signal frequency (4915.2 kHz). This signal is the input to A2.

(2) The input circuit of A2 is a sharply tuned, crystal controlled bandpass filter comprising crystal Y1, capacitors C9, C14 and C17, inductor L5 and resistors R36 and R37. Capacitor C9 is used to peak tune the circuit to the crystal frequency. Crystal Y1 and capacitor C9 also block the dc at the input. The bandpass filter has single-ended input and balanced output. Capacitor C17 is used to balance the circuit so that equal voltages are applied at pins 2 and 3 of A2. As the signals at pins 2 and 3 alternately go positive with respect to the dc bias, A2 produces positive pulses at the output (pin 7).

(3) The positive pulses at the output of A2 are rectified and filtered by CR11 and C20. This positive voltage, applied through resistor R43 to the base, forward biases transistor Q12. The output signal of Q12 is then Ov (logic 0); this signal, inverted by A6C, is applied to NOR gate A7A (para 2-5g). The time constant of C20-R43 is long relative to the signal frequency and it bridges over short gaps in the signal such as many consecutive logic zeroes. As long as cable traffic is active, the output of Q12 remains logic 0 (normal). When cable traffic fails, capacitor C20 discharges through R43 and Q12, then Q12 returns to cut-off. When Q12 turns off capacitor C21 charges from a positive voltage source in inverter A6C and A6C then has a logic 1 input (alarm).

*e. Voltage Filtering Components.* Voltage Filtering components L1, L2 and L3, C3, C4, C11, C12, C15, and C16 limit the coupling of switching transients and other stray signals to the power supply circuits.

#### **2-45. AF Amplifier 1A12A6 Circuit Functioning (fig. 5-34)**

The complete functional description of af amplifier 1A12A6 is provided in paragraph 2-5e. Electrical operation of discrete piece parts is provided below.

*a.* The incoming cable extracted orderwire signal CCEXOW is developed across R1, and is amplified by Q1. Dc bias is provided by R1, R2, R4, and R5. The gain of the amplifier is determined by the ratio of R3 to R4 and the low frequency cutoff is determined by C1, R4 and RS. The amplified output signal is delivered to the power amplifier Q2, Q3, through resistor R6 and capacitors C2 and C3 which form an audio low pass filter. The filter cut-off frequency is approximately 2 kHz. Transistors Q2 and Q3 are a power amplifier which provide current gain but no voltage gain; the circuit operates essentially as an emitter follower. Resistor R10 and capacitor C5 provides output coupling to the load with R10 setting the

output impedance at 100 ohms. When the signal at the base of Q2 goes positive, current through Q2 increases and the emitter voltage rises. Q2 functions essentially as a high impedance emitter follower but the current increase also causes a drop in voltage at the junction of collector load resistors R8 and R9. The signal voltage tapped off at this point increases the forward bias of Q3. Q3 is connected as a common emitter amplifier with R7 as collector load resistor but it functions as a current switch and provides a much greater increase in current than the increase of current in Q2. Isolating resistor R11 connects the collector of Q3 to voltage check point E1.

*b.* The level detector is comprised of C6, CR1, CR2, C7, R12, and R13. Diodes CR1 and CR2 provide voltage doubling of the rectified cable received orderwire signal CROW. The detected voltage is used for system monitoring.

*c.* The transmit orderwire signal COWIN is developed across R14 and R15, and amplified by Q4. The gain of this amplifier is determined by the ratio of R16 to R17. The low frequency cutoff is determined by C8, R17, and R18. Dc bias is determined by R15, R17, and R18. The amplified output signal is coupled to power amplifier Q5 and Q6 through lowpass filter network C14, R18, and C13. This network has a cut-off frequency of approximately 2kHz. Stages Q5 and Q6 are connected as a power amplifier as described above in a above. The output signal is coupled through resistor R23 and capacitor C12 to the load. Isolating resistor R24 connects the collector of Q6 to voltage check point E8.

*d.* The level detector network C13, CR3, CR4, C14, R25 and R26 functions the same as the level detector network for the receive amplifier discussed in b above.

*e.* Voltage filtering components L1 through L4, and C15 through C22 limit the coupling of switching transients and other stray signals to the power supply circuits.

#### **2-46. Radio Amplifier-Detector 1A12A7 Circuit Functioning (fig. 5-35)**

The complete functional description of radio amplifier-detector 1A12A7 is provided in paragraph 2-f. Electrical operation of discrete piece parts is provided in a through j below.

*a. Agc Slicer and Buffer Amplifier.* The agc slicer is a dual transistor (Q4) emitter follower which reduces the amplitude of the reshaped



pcm signal 1RSPCM-1 to approximately the same amplitude as the pcm/orderwire signal FRPCM. It operates as a differential amplifier. Q4A conducts only when its base is more positive than the dc bias at the base of Q4B; when this occurs, Q4B is cut off. Thus, the signal is sliced or rectified because Q4A conducts only on the positive polarity of the pcm signal. The gain is controlled by the dc level at the base of Q4B, which is derived from the 1RSPCM-1 signal as modified by a feedback signal. This is explained in d, e, and below. The output signal from emitter load resistor R20 is coupled through a low pass filter, L7 and C8, which eliminates frequencies above 60 kHz. The signal is

then amplified in emitter follower buffer amplifier Q5. Resistors R21 and R22 determine the dc bias for Q5, and R22 is also the emitter load resistor. The output signal is coupled the radio simulation network.

b. Radio Simulation Network. The first section of the radio simulation network, C9, R23 and R24 provides for simulation of the low frequency phase shift characteristics of the radio receiver and for part of the attenuation. The signal is connected to the attenuation network, R25, R26

and R27 through capacitor C11. C11 provides some high frequency attenuation but it provides more low frequency than is desired. To compensate for this, part of the  $i_g$  (from R24) is coupled through low pass filter, C10 and R30.

c. *Subcontractor.* Amplifier A1 is a type MC131G integrated circuit (fig. 5-24) which operates as a unity gain differential amplifier. The input signal at pin 1 is the pcm signal. The input signal at pin 2 (inverting input) is the pcm plus orderwire signal. This signal, FRPCM, comes through low pass filter,  $I_f$ , C23 and R45 which eliminates frequencies above 50 kHz. The two pcm signals are as nearly equal as the circuits can make them. The result is that the output signal is the orderwire signal plus some residual pcm because the two pcm signals cancel (or the pcm at input pin 1 is subtracted from the pcm input at pin 2). The output signal (orderwire plus residual pcm) is fed back through capacitor CS3 and resistor R6 to the primary of transformer T1. It is also connected to the inverting input (pin 2) through resistor R31. Since the signal here is the pcm plus orderwire and the two orderwire signals are equal, the orderwire signal has no effect but the residual pcm signal provides negative feedback. Operating voltages are supplied to pin 1 through voltage divider resistors R28 and R29 and to pin 2 through R33 and zener diode CR2. Capacitors C14 and C15 filter the supply voltages.

d. *Buffer.* The reshaped pcm signal, 1RSPCM1, is passed through a low pass filter composed of L1, R2, R3 and C1 with a cutoff frequency of approximately 50 kHz. This passes the low frequency components of the pcm signal which is coupled through buffer amplifier Q1 to pin 3-5 of transformer T1 with no loss in signal. Q1 is an emitter follower; dc bias is determined by R3 and R4 and R4 is also the emitter load resistor. The output signal is coupled through capacitor C2 and isolating resistor R6 to the secondary of transformer T1.

e. *Product Detector.* The pcm signal inserted at the transformer center tap and the feedback residual pcm from the primary of transformer T1 are out of phase in the secondary; cancellation by an amount equal to the feedback pcm occurs. The resulting signal (reduced pcm plus orderwire) is rectified and filtered by C4, R5, R7, R8 and R9 and applied as positive dc pulses to the bases of Q2A and Q2B. Each half of the secondary of transformer T1 works into a half wave rectifier. Since their input signals are out of phase, the output pulses at Q2A and Q2B alternate.

f. *Differential Amplifier.* The differential amplifier operates as a class B push-pull amplifier. Resistors R10, R11, R47, and R11 set the dc bias level for Q2 stages. The voltage is filtered by O6. Resistors R12, R14, R16, R17, and R18 set the dc bias level for

Q3. Resistors R12, R14, R15, and R19 are collector load resistors. When the signal at the base of Q2B goes more positive, the collector voltage goes negative and drives the base of Q3B negative. Conduction through Q3B increases and charges capacitor C7. When the signal at the base of Q2A goes more positive, the collector voltage goes negative and drives the base of Q3A negative. The emitters of Q3A and Q3B are then driven negative to reduce the charging current into capacitor C7. The voltage across C7 is applied to Q4B and controls the gain of the age slicer.

g. *AF Amplifier.* The orderwire plus residual pcm output signal from subtractor A1 is developed across level adjustment potentiometer R34 and coupled to the base of audio amplifier Q6. Transistor Q6 is a common emitter amplifier; dc bias is determined by R36, R57 and R34. Resistor R37 is bypassed for ac by C16; R36 provides a small amount of degenerative feedback. Resistor R35 is the collector load resistor. The stage provides a gain of approximately 100. The output signal is coupled through low pass filter C17, C18, and R38. Transistor Q7 and Q8 are a power amplifier which provide current gain but no voltage gain; the circuit operates essentially as an emitter follower. When the signal at the base of Q7 goes positive, current flow through emitter load resistor R39 increases and the emitter voltage increases. Increased current flow in Q7 causes the voltage drop across the collector load, R41 and R40 to increase. This negative-going voltage, tapped off at the junction of R41 and R40, increases current flow in Q8. This is the main source of signal current flow. The output signal is coupled through R42 and C20. R42 provides an output impedance of 100 ohms. Isolating resistor R46 connects the collector of Q8 to voltage check point E9.

h. *Level Detector.* The orderwire signal detector, comprised of C21, CR3, CR4, C22, R43, and R44, is a voltage doubled-rectifier circuit used to monitor the peak amplitude of the radio recovered orderwire

i. *Voltage Filtering Components.* Voltage filtering components, I through L6 and C24 through CS1 limit the coupling of switching transients and other stray signals to the power supply circuits.

## 2-47. Radio Digital Regenerator 1A12A8 Circuit Functioning (fig. 536)

Radio digital regenerator 1A12A8 contains integrated circuits designated A1 and A3 through A11. Figure 5-24 provides a circuit diagram for each type of integrated circuit used. The complete functional description of radio digital regenerator 1A12A8 is provided in paragraph 2 Electrical operation of discrete piece parts is provided in subparagraphs below.

a. *Differential Amplifier.* The differential amplifier consists of a match pair of npn transistors, Q1A and Q1B, connected in a common emitter configuration with resistors R2, R3 and R4 in the emitter circuit. Resistor R1 is the 51 ohm termination for the pcm/orderwire input signal FRPCM. R6 and CR1 are the collector load for Q1A and R5 is the collector load for Q1B. The base of Q1B is grounded so Q1A turns on when the input voltage goes positive. When Q1A turns on there is a sharp drop in collector voltage (to approximately 0v). This is the voltage at the base of Q3; the voltage at the base of Q2 is 0.7v higher because of the voltage drop across CR1. Q3 turns on, Q2 is off. As the input voltage returns toward 0 volts, the voltage at the base of Q3 rises. When the voltage at the base of Q3 is 5.3 volts, Q3 starts to cut off and reaches cut-off when the base voltage is approximately +6 volts. When the voltage at the base of Q3 is + 5.3 volts, the voltage at the base of Q2 is +6 volts; Q2 is still off. When the voltage at the base of Q3 is +6 volts, the voltage at the base of Q2 +6.7 volts. At 6.2 volts and higher voltages Q2 conducts. The collector of Q1A will have about a 4 volt peak peak swing for a 1 volt peak-peak input signal at base of Q1A.

b. *Linear Buffer 1.* Linear buffer 1 consists of a pair of complementary transistors (npn and pnp) connected as emitter followers; Q2 conducts on the positive half cycle of the input signal and Q3 conducts on the negative half. When Q2 conducts, capacitor C1 charges through diode CR2 and capacitor C2. When Q3 conducts, capacitor C1 discharges through diode CR3 and capacitor C4. Thus, Q2 and Q3 are low impedance sources which rapidly charge and discharge capacitor C1 and couple the FRPCM signal into the peak detectors. R7 and R8 are current limiters to protect Q2 and Q3. The average dc voltage at the emitters of Q2 and Q3 is + 6 volt dc, so the ac signal at the bases is swinging positive and negative above and below this value. When it is +5.3 volts or less (0.7 volt negative with respect to +6 volt), Q3 is on; when it is +6.7 volts or higher (0.7 volt positive with respect to + 6 volts), Q2 is on.

c. *Peak Detectors.* The FRPCM signal is identified by diodes CR2 and CR3. The rectified voltage is developed across load resistors R9 and R11 and filtered by C2 and C4. C3 provides additional high frequency filtering. Under operation, C2 has an average positive voltage (E20) and C4 has an average negative voltage (E21). These voltages permit current to flow through C1 only on peaks of the signal voltage applied to Q2 and Q3. The algebraic sum of the voltages at E20 and E21 is present at E23. This voltage (E23) is always the dc average of the positive and negative peaks of the FRPCM signal.

d. *Linear Buffers 2 and 3.* Linear buffer 2 consists of npn and pnp emitter followers in series. R10 and R14 determine dc bias and R14 is the emitter load resistor. The pnp and npn transistors provide temperature compensation and cancellation of offsets, that is, the base to emitter voltage drop (positive to negative) of Q4A is cancelled by an opposite voltage change at the base-emitter junction of Q5A. Thus the voltage at the base of Q4A always equals the voltage at the emitter of Q5A. The circuit of linear buffer 3 is the same. The output signals are coupled through isolating resistors R19 and R20.

e. *Voltage Comparators.* Voltage comparator 1 (A11) receives the FRPCM signal at pin 3 (E13) and the dc reference signal developed from the FRPCM signal at pin 2 (F12). When the input signal at pin 3 goes more than 0.6 millivolt positive with respect to the signal at pin 2, the output goes to logic zero. When the input signal at pin 3 goes more than 0.6 millivolt negative with respect to the signal at pin 2, the output goes to logic one. Capacitor C5 is a supply voltage filter. When the output of A11 switches to logic zero (low), the negative voltage through R22 speeds up the transition at the input of A3A. Voltage comparator 2 (A8) is similar to voltage comparator 1 (A11). A fixed reference input of approximately +2v is supplied at pin 2 through voltage divider resistors R40 and R42. Feedback applied through R41 improves circuit stability. Under normal operation (pcm signal active), the output of A10 is low, so the input of A8 (pin 3) is low and the output is high. The output of A8 switches to low, when the input at pin 3 becomes more positive than +2 volts (pin 2). When the output of A10 switches to logic one (high),

current flow through R39 must charge capacitor C15 to +2 volts before the output of A8 switches to low. The time constant of R39, C15 is approximately 300 milliseconds, so a delay of 300 milliseconds occurs after the output of A10 switches before A8 switches. If the output of A10 returns to logic zero (low) before the output of A8 switches, capacitor C15 discharges and A8 does not switch. This delay action bridges over intervals in the pcm signal when many consecutive zeros occur and prevents a false indication of failure when the pcm signal is active.

*f. Transition Detectors.* Transition detectors 1 (A9) and 2 (A10) are similar in circuit and operation to alarm circuit 1 (A6) in cable digital processor 1A12A4 (para 243b). The time constant for transition detector 1 (A9) is determined by R23 and C6 and is 350 microseconds. The time constant for transition detector 2 (A10) is determined by R38 and C14 and is 420 nanoseconds.

*g. Slicers.* Slicer 1 (A7) has a fixed reference voltage at pin 2, supplied by voltage divider resistors R26 and R27. The supply voltages are filtered by C7 and C25. Feedback through R28 improves circuit stability. Resistor R25 isolates the input of A7 and prevents feedback from the input circuit of A7 to the low impedance input of Q1A. When the input signal (pin 3) is positive with respect to the reference signal (pin 2), the output is low (logic zero). When the input signal is negative with respect to the reference signal, the output is high (logic one). The reference voltage provided at pin 3 of slicer 2 by resistors R32 and R35 is adjustable. It is filtered by C12. When the input signal (pin 2) of slicer 2 is positive with respect to the reference voltage (pin 3), the output is high (logic one). When the input signal is negative with respect to the reference voltage, the output is low (logic zero).

*h. Tuned Circuit.* When the output of inverter A1 is low, the voltage drop across R31 is 12 volts and capacitor C10 charges to 12 volts through the primary of T1. When the output of A1 switches to high (+5 volts), the voltage drop across R31 is reduced by 5 volts. Capacitor C10 discharges through R31 and the transformer primary to the new voltage. The voltage pulse produced by this discharge is coupled to the tuned circuit in the transformer secondary. The secondary circuit is tuned to 2304 kHz by crystal Y1. Capacitor C11 is used to null the stray capacitance of the crystal circuit. As the tuned circuit oscillates, the voltage drop across R36 varies at the resonant frequency. The signal is applied to A6 through current limiting resistor R37.

*i. Leading Edge Pulse Generator.* Resistor R29 and capacitor C8 form a delay circuit. The operation of this circuit is similar to that described for delay circuit R39, C15 at the input of voltage comparator 2 (e above).

*j. Voltage Filtering Components.* Voltage filtering components L1 through L4 and C17 through C24 limit the coupling of switching transients and other stray signals to the power supply circuits.

## **2-48. Radio Control-Comparator 1A12A9 Circuit Functioning (fig 5-37)**

Radio control-comparator 1A12A9 contains integrated circuits designated A1 through A10. Figure 5-24 provides a circuit diagram for each type of integrated circuit used. The circuits of 1A12A9 that are comprised of discrete components are similar to corresponding circuits of cable control comparator 1A12A3 and the explanation of circuit operation is the same. Refer to paragraph 242. The complete functional description of radio control comparator 1A12A9 is provided in paragraph 2-6b.

## **2-49. Radio Digital Processor 1A12A10 and 1A12A16 Circuit Theory (fig. 5-38 and 5-38.1)**

The integrated circuits used in radio digital processor 1A12A10 and 1A12A16 are shown functionally in figure 5-38 for the synchronous mode and in figure 538.1 for the asynchronous mode. Figures 538 and 538.1 specify each integrated circuit type. Figure 5-24 provides a circuit diagram for each type of integrated circuit used. The complete functional description of radio digital processor 1A12A10 and 1A12A16 is provided in paragraph 2-6c and 2-6c.1. Electrical operation of discrete piece parts is provided below.

*a. Cable Output Amplifier.* Transistor Q1 has a fixed dc bias, determined by voltage divider L1, R2 and CR1, at the emitter. The primary of transformer T1 is to collect load impedance. Resistor R3 is a current limiter to protect Q1; R4 and CR2 clamp out inductive current when the signal changes from logic one to logic zero. When the output signal at A4C is logic one, transistor Q1 turns on and provides a current pulse through the primary of T1. This pulse is inductively coupled into both sections of the secondary. Positive-going transition of the input signal is speeded up by the +5 volt source through resistor R39 and capacitor C1.

Capacitor C1 charges with negative polarity on the side connected to the base of Q1. On negative-going input signal transitions, the negative charge on C1 speeds up switching time of Q1.

*b. Output Circuit.* The cable direct current path is shown in figure 5-29 which illustrates the complete current path through digital data modem 1A12. Diodes CR8 through CR15 provide protection against breakdown voltages in excess of 1300 volts. The cable current is set for a nominal 38 milliamperes. The cable simulation networks are 1/4-mile line sections which can be patched on-line for proper termination of the cable. These are selected to provide a 1-mile cable section for the remote cable repeater. Capacitor C4 provides signal ground for pcm.

*c. Traffic Detector.* The traffic detector circuit consists of transistor stages Q2 through Q4. The traffic signal from cable output amplifier Q1 is applied to traffic detector amplifier Q2, Q3 through transformer T1. The output of Q3 controls transistor switch Q4 in the traffic detector circuit and also transistor switch Q5 in the indicator circuit. When a traffic signal is detected Q4 and Q5 are turned on. With Q4 and Q5 turned on, the ONOR output is low and DS1 is on (normal condition). When a traffic signal is not detected, Q4 and Q5 are turned off. With Q4 and Q5 turned off, the ONOR output is high and DS1 is off (alarm condition). Positive pulses at the secondary (pins 5 and 6) of transformer T1 are applied through current limiting resistor R26 to the base of Q2. Q2 turns on and develops a negative-going voltage pulse across collector load impedance R27, R28 and R29. Part of this signal is connected to the base of Q3, which then develops a positive-going voltage pulse across collector impedance R34. The positive-going output signal of Q3 is coupled through current limiting R32 and R33 into the bases of Q4 and Q6. Q4 and Q5 turn on and signals ONOR and 1RP-FAIL are logic zero. Lamps DS1 is lighted. Diodes CR3, CR4, CR6 and CR7 are connected from base to emitter at their respective transistors. They protect the base emitter junction against excessive reverse voltage. Resistors R31 and R35 speed up turn off time of Q4 and Q5. Resistor R36 keeps lamp DS1 warm during off time. CR5 and R30 limit current (to external relay 1A12A12A2TB1K1) for logic one (Q4 off).

*d. Voltage Filtering Components.* In figure 5-38, voltage filtering components L1, L5, L6, L7, C2, C3, and C14 through C19 limit the coupling of switching transients and other stray signals to the power supply

circuits. In figure 538.1, the voltage filtering components are L3, L4, and capacitors C6 through C10.

## 2-50. Orderwire Assembly 1A13 Circuit Functioning

Orderwire assembly 1A13 provides party line communication on a single orderwire channel by amplifying and interconnecting signals between Handset H-156/U, remote phone, the radio equipment, and the through orderwire. The internal orderwire connections are such that sidetone is only provided for Handset H-1656/U. The orderwire assembly also provides central alarm monitoring circuits, an input to a speaker monitor, inband signaling at 1.6 kHz, a 1.1 kHz test tone, and orderwire fault detection circuits. Five daughter board assemblies 1A13A1 through 1A13A5 plug into orderwire chassis 1A13A7 to provide the functions mentioned above. The interconnections between the five daughter board assemblies and chassis mounted components of the orderwire assembly are shown in figure 5-39. Paragraphs 2-51 through 2-55 describe each board in reference designation order (1A13A1, 1A13A2, etc). The descriptions are at the circuit level and are based on the schematic diagram of the associated board.

### 2-51. Daughter Board No. 1 Assembly 1A13A1 Circuit Functioning (fig. 5-40)

Daughter board No. 1 assembly 1A13A1 provides the orderwire fault detection circuits. The circuits consist of a 4.02 kHz oscillator circuit, monitor circuit, MODULE TEST selector switch, and TEST TONE switch. The MODULE TEST selector switch (1A13A1S1) connects a test input signal (4.02 kHz or ground) to the orderwire circuit under test. The output of the orderwire circuit under test is connected through the MODULE TEST selector switch to the monitor circuit. The TEST TONE switch (1A13A1S3) is used to control the 1.1 kHz oscillator circuit on daughter board No. 2 assembly 1A13A2. When depressed, the TEST TONE switch turns on the 1.1 kHz oscillator and the 1.1 kHz test tone signal is routed to the orderwire circuits. The following subparagraphs describe the 4.02 kHz oscillator and monitor circuits on daughter board No. 1 assembly 1A13A2.

*a. 4.02 kHz Oscillator Circuit.* The 4.02 kHz oscillator circuit generates a test signal for amplifier circuits on daughter board assemblies

1A18A3 through 1A1S3A, peak limiter circuits on 1A18A5, and the speaker amplifier circuit on 1A13A2.

The 4.02 kHz oscillator circuit is comprised of transistor circuit Q1, tuned circuit Z1,

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and output amplifier A1. Output amplifier A1 is a buffer stage which isolates the oscillator output. The 4.02 kHz output of amplifier A1 is applied to S1C-1 and S1E-1 of the MODULE TEST selector switch and the transformer 1A13A1T1. The transformer inverts the 4.02 kHz output for application to S1D-1 of the MODULE TEST selector switch. The two 4.02 kHz signals are applied to S1C-1 and S1D-1 because two inputs are required to test the amplifier circuits on daughter board assemblies 1A13A3 through 1A13A5 and the peak limiter circuits on 1A13A5. The 4.02 kHz signal applied to S1E-1 is used to test the 4.02 kHz oscillator and monitoring circuits. With the MODULE TEST selector switch set to position 1, the 4.02 kHz test signal is routed through S1E-1 and suet the monitoring circuit Q2, IC A2, and switch assembly S2. An analysis of the 4.02 kHz oscillator circuit follows:

(1) Transistor circuit Q1 and tuned circuit Z1 form a modified Colpitts oscillator. Tuned circuit Z1 is a parallel tank circuit with a frequency of 4.02 kHz. When power is initially applied, the tank circuit oscillates and the 4.02 kHz signal is coupled from pin 2 of the tank circuit to the emitter of Q1. The amplifier signal developed at the collector of Q1 is applied to the tank circuit and sustains oscillation because the initial loop gain is greater than unity. Resistors R1 and R2 provide the bias at the base of Q1 and resistors R3 and R6 are bias resistors at the emitter of Q1. Potentiometer R4, in the emitter bias circuit provides a means of adjusting the signal level into amplifier A1.

(2) Two 4.02 kHz oscillator output signals are coupled to amplifier A1 which provides level control. One 4.02 kHz oscillator output is coupled through capacitor C2 and voltage divider R8, R9 to the inverting input of A1 and the other 4.02 kHz oscillator output is coupled through capacitor C1 and voltage divider R6, R7 to the noninverting input of A1. This configuration (inverting and noninverting inputs) provides minimum distortion. C3 and C4 are stabilizing capacitors and resistor R10 provides a negative feedback path to stabilize the voltage gain. A zero dc offset voltage is obtained by supplying -6 volts bias through R11. Capacitor C5 blocks dc from the output circuit. Resistors R12 and R13 are impedance matching resistors in the output circuit. A diagram of amplifier A1 (integrated circuit U5B770231X) is provided in figure 6-24.

b. Monitor Circuit. The monitor circuit determines the status of the orderwire circuit under test. If the circuit under test is operating properly, MODULE TEST indicator DS1 is extinguished. If the circuit under test is not operating properly, the MODULE TEST indicator lights red. The monitor circuit is comprised of emitter follower Q2, tuned circuit (4.02 kHz) Z2, amplifier A2, and switch assembly S2. The 1.6 kHz oscillator, 1.1 kHz oscillator, or alternating 1.1/1.6 kHz alarm signals are applied to the monitor circuit through S1-A of the MODULE TEST selector switch.

(1) The 4.02 kHz test signal is applied through the voltage divider network consisting of .R,16 and R17 through SIB of the MODULE TEST selector switch. Potentiometer R17 is used to adjust the sensitivity of the 4.02 kHz test signal which is coupled to the base of emitter follower Q2 through closed contacts of switch S2 and capacitor C8. Emitter follower Q2 provides a low input impedance to tuned circuit Z2. Resistor R19 stabilizes the input impedance at the base of Q2 and resistor R20 establishes the bias at the emitter of A2. Tuned circuit Z2 provides a very narrow bandwidth and peaked output at 4.02 kHz which is applied to amplifier A2 through capacitor C9. A diagram of amplifier A2 (integrated circuit CA3035) is provided in figure 5-24.

(2) Amplifier A2 provides an output across resistor R26 which is applied through pin 6 of switch assembly S2 to the MODULE TEST indicator lamp driver. When the 4.02 kHz test signal is amplified and properly detected, the output at pin 7 of amplifier A2 is approximately 0 volt causing the MODULE TEST indicator lamp to remain extinguished. If the 4.02 kHz test signal is not amplified and properly detected, the output of amplifier A2 is approximately + 10 volts causing the MODULE TEST indicator lamp to light red. Resistor R18 and diode CR1 provide the voltage necessary to operate MODULE TEST indicator DS1.

(3) The 1.6 kHz oscillator, 1.1 kHz oscillator, or 1.1/16 kHz alternating alarm signal is applied to three stage amplifier A2 through S1A, resistors R33 and R21, and capacitor C9. If the test signal applied is of the proper amplitude, amplifier A2 will provide an output that causes the MODULE TEST indicator to remain extinguished. The positive signal output from the first stage of amplifier A2 is coupled through C10 and is detected by diodes CR2 and CR3. Capacitor C11 filters the detected signal. Resistor R22 is a feedback resistor for the first stage and resistors R23 and R24 are input resistors for the the

second and third stages of amplifier A2. Resistor R25 provides positive bias to operate the MODULE TEST indicator DS1 under zero output conditions. Capacitors C6 and C7 are decoupling capacitors for the + 12v and - 6v supplies. Resistors R14, R15, and R26 through R32 are voltage dividing resistors to provide proper monitoring levels.

## 2-52. Daughter Board No. 2 Assembly 1A13A2 Circuit Functioning (fig. 5-41)

Daughter board No. 2 assembly contains the central alarm monitor, the 1.1 kHz test tone oscillator, and the speaker amplifier circuits. The following subparagraphs describe each circuit on daughter board No. 2 assembly.

*a. Central Alarm Monitor Circuit.* The central alarm monitor circuit monitors the alarm input signals, RCVR ALM, XMTR ALM, and PCM ALM. If an alarm condition is present at any of the inputs, the central alarm monitor circuit will cause the CNTRL ALARM indicator on meter panel assembly 1A15A8 to change from green to red and the 1.1/1.6 kHz audible alarm to sound. The alarm inputs are applied to two OR gates: OR gate A controls the 1.1/1.6 kHz audible alarm and OR gate B controls the CNTRL ALARM indicator on meter panel assembly 1A15A8.

(1) With ground applied to any of the alarm inputs, OR gate A (diodes CR6-CR9, resistors R18-R21, and capacitors C5-C8) detects an alarm condition and controls the audible alarm circuits. Assume that ground is applied to pin 6 (PCM ALM) causing capacitor C5 to discharge through resistor R18. The negative pulse developed across R18 is coupled through diode CR6 to the cathode of silicon controlled switch Q3 causing Q3 to operate. With Q3 operating, a ground return is connected to the emitters of multivibrator transistors Q1 and Q2 permitting the multivibrator to operate. R4 and C2 determine one time constant of the multivibrator and R3 and C1 determine the other time constant. R2 and R5 are collector bias resistors of the multivibrator. When pin 4 of Q3 is connected to + 12v through pins E and A and R6, the current to turn on Q3 is from +12v through R1 and R7 to ground. CR1 is used as a bias diode. With the multivibrator operating, the 1.1 kHz and 1.6 kHz oscillators are alternately turned on and off. The multivibrator output at the collector of Q1 is applied to the emitter of Q7 (part 2-90 of 1.1 kHz oscillator circuit) through diode CR10.

When Q1 conducts, its collector voltage is low and triggers the 1.1 kHz oscillator into oscillation. When Q1 is not conducting, its collector voltage is high and the 1.1 kHz oscillator cannot oscillate because a high voltage is applied through CR10 to the emitter of Q7. The multivibrator output at the collector of Q2 is applied to the 1.6 kHz oscillator circuit on 1A13A5 and alternately turns the oscillator on and off. The alternating 1.1/1.6 kHz oscillator outputs are applied through external circuits and pin M to emitter followers Q4 and Q5. Resistors RS through R12 are used to bias emitter followers Q4 and Q5. The output of Q5 is applied to speaker amplifier A2 through resistors R13, R83, and R34. Capacitor C16 couples the signal to amplifier A2. C16 is a high frequency bypass. Stabilization of the amplifier is accomplished with C18 and C19. The output of A2 is connected through C20, C21 and R36 to speaker amplifier monitor. The output of Q4 is applied to the remote signal alarm through the hybrid transformer mounted on orderwire assembly 1A13. The 1.1/1.6 kHz audible alarm signal can be removed by depressing the RESET pushbutton on meter panel assembly 1A15A8. This removes the path through Q3 causing Q3 and the multivibrator to turn off.

(2) Speaker amplifier A2 receives additional order-wire inputs through pin 8, speaker volume control No. 1 input. The signals are amplified for application to the speaker on meter panel assembly 1A15A8. A circuit diagram of amplifier A2 (integrated circuit MC1554G) is provided in figure 24.

(3) With ground applied to any of the alarm inputs, OR gate B (diodes CR2-CR5 and resistors R14-R17) detects the summary alarm condition and causes the CNTRL ALARM indicator on meter panel assembly 1A15A8 to change from green to red. Assume that ground is applied to pin 6 (PCM ALM) causing diode CR2 to conduct. With CR2 conducting, transistor switch Q6 is turned-off. For this condition, the operating voltage for the green lamp, CNTRL ALM-NORMAL, is removed from pin P, and the ground return for the red lamp, CNTRL ALARM, is applied to pin N through CR2. Thus, the CNTRL ALARM indication on meter panel assembly 1A15A8 changes from green to red (alarm condition).

*b. 1.1 kHz Oscillator Circuit.* The 1.1 kHz oscillator circuit generates the 1.1 kHz signal which is used for test tone and part of the audible



alarm signal (1.1/1.6 kHz). The oscillator circuit is comprised of transistor circuit Q7, 1.1 kHz tuned circuit Z1, and amplifier A1. Transistor circuit Q7 and 1.1 kHz tuned circuit Z1 form a modified Colpitts oscillator. Resistors R22 and R33 are a voltage divider and develop the bias on the base of Q7. R24, R25, and R26 are the Q7 emitter resistors and provide dc bias and ac impedance. Potentiometer R25 controls the ac input level to amplifier A1. The oscillating frequency is determined by the 1.1 kHz tuned circuit. The oscillator turn-on signal is coupled through diode CR10 from the multivibrator circuit Q1 and Q2, the MODULE TEST switch on 1A13A1, or the TEST TONE switch on 1A13A1. When the oscillator is turned on, the 1.1 kHz output of Z1 is fed back to the emitter circuit of Q7. The amplified signal developed at the collector of Q7 sustains oscillation. Capacitors C9 and C10 and R27 and R24 couple the 1.1 kHz output to operational amplifier A1. R28 and R31 provide input loading for amplifier A1. In addition, R31 and R128 form the feedback path which determines the amplifier gain. R32 is a bias load resistor. The A1 output is coupled through resistor R35. C13 and C14 are stabilizing capacitors preventing high frequency oscillations. Amplifier A1 is a general purpose operational amplifier which provides minimum distortion and isolates the oscillator from the output circuits. A circuit diagram of amplifier A1 (integrated circuit U5B770231X) is provided in figure 5-24.

*c. Filtering Components.* C11, C12, and C17 are filter capacitors for the power supply circuits. C3 and C4 are spike suppression capacitors for high frequency.

### **2-53. Daughter Board No. 3 Assembly 1A13A3 Circuit Functioning (fig. 5-42)**

Daughter board No. 3 assembly 1A13A3 contains the pcm alarm circuit and amplifier circuits A1 and A2. Each circuit is described in the following paragraphs.

#### **NOTE.**

**Amplifiers A1 and A2 are integrated circuits (type MC1533G). A circuit diagram is provided for these circuits in figure 5-24.**

*a. PCM Alarm Circuit.* The pcm alarm circuit (relay K1) connects either the recovered orderwire signal (pins N and S) or the receiver traffic signal (OW-PCM BYPASS, pin D) to the orderwire circuits. For normal conditions, a ground return is present at pin H causing relay K1 to be energized. With K1 energized,

the recovered orderwire signal is coupled to the orderwire circuits by transformer T2, resistors R10 and R9, and contacts 4 and 6 of relay K1. When a pan alarm condition occurs, the ground return is removed from pin H and relay K1 becomes deenergized. R11 is a dropping resistor in the relay coil circuit. With K1 deenergized, the ow-pcm bypass signal (pin D) is applied to the orderwire circuits by contacts 8 and 6 of relay K1. Since the orderwire signal is part of the receiver traffic signal, orderwire communication is maintained when a pcm failure occurs.

*b. Amplifier A1.* Amplifier A1 (o.w. ampl 3) amplifies orderwire signals for application to the through orderwire transmit terminals (pins 11 and 12). The recovered order wire 4 kHz input (orderwire test signal), or the ow-pcm bypass signals are applied to the noninverting input (pin 2) of amplifier A1 through capacitor C2. Resistor R2 provides symmetrical loading to the noninverting input of A1. The ow ampl 3 input signals are applied to the inverting input (pin 1) of amplifier A1 through capacitor C1. Amplifier A1 has an input impedance of approximately 1 megohm and an output impedance of approximately 100 ohms. The amplifier gain is approximately 100 which is determined by resistor R1 and resistor R3. Capacitors C3, C4, and C5, and resistor R6 provide stabilization. The output (pin 5) is coupled to the through orderwire transmit terminals by capacitor C6, resistor R5, 3 kHz low pass filter FL1, and transformer T1. Filter FL1 sharply attenuates signals above 3kHz, consequently, the 4 kHz test signal cannot appear at the through orderwire transmit terminals. The 4kHz is routed to orderwire amplifier No. 3 monitor circuits through pin E. Resistors R6, R7, and R8 provide an impedance match between the filter and transformer T1.

*c. Amplifier A2.* Amplifier A2 amplifies orderwire amplifier No. 2 input signals for application to the orderwire hybrid terminal (pin 8). Orderwire signals (through orderwire receive and recovered orderwire) are applied to the inverting input (pin 1) of amplifier A2 through capacitor C7 and resistor R12. The noninverting input (pin 2) receives the orderwire amplifier No. 2 inputs (pin 9) through capacitor C8. Resistors R14 and R12 determine the gain of A2 and R13 provides a symmetrical input into the non-inverting input (pin 2). Capacitors C12 and C13 provide stabilization. The output of A2 is applied to filter FL2 through C14 and R16. R17, R18 and R19 provide an output T pad for filter FL2.

R20 couples the output signal to the remote signal/alarm circuits.

*d. Filtering Components.* Capacitors C9 and C10 are filter components for the power supply circuits.

#### **2-54. Daughter Board No. 4 Assembly 1A13A4 Circuit Functioning (fig. 5-43)**

Daughter board No. 4 assembly 1A13A4 contains amplifier circuits and the 1.6 kHz monitor circuit. Each circuit is described in the following paragraphs.

#### **NOTE.**

**Amplifiers A1 and A2 are type MC1533G integrated circuits and amplifiers A3 and A4 are type CA3035 integrated circuits. A circuit diagram for each of these circuits is provided in figure 5-24.**

*a. Amplifier Circuits.* Amplifiers A1 and A2 amplify signals for application to the speaker amplifier 6 monitor circuit, and orderwire amplifier 4 monitor circuit. Through orderwire receive oz 4.02 kHz test signals are applied to the inverting input (pin 1) of amplifier A1 (ow ampl 4). The through orderwire receive signal is applied through pins 6 and H, transformer T1, resistors R13, R7, and R1 and capacitor C1. The 4.02 kHz test signal is applied through pin F, resistors R7 and R1, and capacitor C1. The orderwire amplifier inputs, are applied to the noninverting input (pin 2) of amplifier A1 through pin M and capacitor C2. The amplifier provides a gain of approximately 100. Circuit operation and component function is the same as described in paragraph 2-53 for amplifier A1 on 1A13A3. The output (pin 5) of amplifier A1 is coupled through capacitor C8 and resistor R5, appears across potentiometer R6, and is applied through pin 1 to orderwire amplifier No. 2. The output of A1 is also applied to the inverting input (pin 1) of amplifier A2 through coupling capacitor C9. Also the 4.02 kHz test signal is applied to the inverting input of A2 through pin E, resistors R6 and R9, and capacitor C9. The orderwire amplifier 6 remote input signals are applied to the noninverting input (across R10) of amplifier A2 through pin N and coupling capacitor C10. Amplifier A2 provides a gain of 100 and operates the same as amplifier 1A13A3A1 (para 253). The output of amplifier A2 is coupled through capacitor C14 and 3 kHz low pass filter FL1 to Handset H-156/U by the handset rev -terminal (pin L) Filter FL1 sharply attenuates signals above 3 kHz, consequently, the 4.02

kHz test signal is not applied to Handset H-156/U. Resistor R14 matches the output impedance of the amplifier to the filter circuit. Resistors R15-R17 form an impedance matching network in the output of filter FL1. The output of amplifier A2 is also applied to the speaker amplifier circuit through resistor R18 and pin 12 and to the 1.6 kHz monitor through resistor R20.

*b. 1.6 kHz Monitor Circuit.* The 1.6 kHz monitor circuit detects the orderwire amplifier 6 input (1.6 kHz ringing signal). The circuit is comprised of tuned circuit Z1, amplifiers A3 and A4, a level discriminator circuit, and relay K1. When the 1.6 kHz ringing signal is detected, relay K1 becomes energized causing the 1.6 kHz ringing signal to be applied to the speaker volume control circuit No. 1 through pin 13. Also, the RING indicator on the meter panel assembly 1A15A8 changes from green to amber.

(1) A 1.6 kHz signal at the output of amplifier A2 is passed by means of voltage dividing resistors R20 through R25, through the 1.6 kHz tuned circuit, and capacitor C16 to amplifier A3. A3 is comprised of three amplifier stages. Pin 1 is the input and pin 3 is the output of the first stage of A3. The first stage is a frequency reject circuit in that a level will appear at pin 3 only when a 1.6 kHz signal is present. R27 provides negative feedback for gain stabilization. Pin 3 is connected to the input (pin 4) of the second stage through resistor R26 and capacitor C15. The output of the second stage is pin 5. (The third stage of amplifier A3 is not used.) The output of the first and second stages are coupled to the level discriminator circuit (diodes CR1 through CR5 and resistor R28) through capacitor C17 and C18.

(2) The output of the level discriminator circuit is applied to the input (pin 1) of amplifier A4 through filter network R29, R30, and C19. Amplifier A4 is the same type of circuit as amplifier A3; however, the third stage of A4 is used (input-pin 6, output-pin 7). Resistors R32 and R31 are input resistors for the second and third stages. When no signal or a signal other than 1.6 kHz  $\pm$  40 Hz is applied to amplifier 3, the amplitude-phase detector circuit causes the output of A4 to be high (+12v). For this condition, relay K1 is deenergized. When the ringing signal (1.6 KHz  $\pm$  40 Hz) is applied to amplifier A3, the level discriminator causes the output of A4 to be low (0 volt). For this condition, relay K1 is energized causing the RING indicator on the meter panel assembly 1A15A8

to change from green to amber and ringing tone to be applied to the speaker. Diode CR6 protects against transient voltages when relay K1 is deenergized.

(3) Capacitors C3 and C4 are used to decouple the power supply inputs to 1A13A4. Resistor R8 provides the proper output level from A2 for monitoring purposes. Resistor R19 couples the 1.6 kHz tone to the speaker volume control No. 1 when relay K1 is energized.

## 2-55. Daughter Board No. 5 Assembly 1A13A5 Circuit Functioning (fig. 5-44)

Daughter board No. 5 assembly contains the 1.6 kHz oscillator circuit, peak limiter circuits, and amplifier circuits. Each circuit is described in the following paragraphs.

### NOTE

**Amplifiers A1 through A5 and voltage regulator VR1 on board 1A13A5 are integrated circuits: A1 (type U5B 770231X), A2 and A3 (type CA3001), A4 and A5 (type MC1533G), and VR1 (type MC1560G). A circuit diagram of each circuit is provided in figure 5-24.**

a. *1.6 kHz Oscillator Circuit.* The 1.6 kHz oscillator generates a 1.6 kHz signal which is used for ringing and also for part of the 1.1/1.6 kHz alternating alarm signal. The circuit is comprised of transistor circuit Q1, 1.6 kHz tuned circuit Z1, and amplifier A1 (osc amplifier). Transistor circuit Q1 and 1.6kHz tuned circuit Z1 form a modified Colpitts oscillator circuit. The oscillator control signal is coupled to the emitter of Q1 through diode CR1 and pin C. The oscillator can be turned on by the RING switch on meter panel assembly 1A15A8, the MODULE TEST selector switch on 1A13A1 or the central alarm circuits on 1A13A2. The 1.6 KHz oscillator output is applied to amplifier A1 via capacitors C1 and C2. Amplifier A1 is a general purpose operational amplifier which provides minimum distortion and isolates the oscillator from the output circuits. The 1.6 kHz oscillator and amplifier circuit and component function is identical with that of the 4 32 kHz oscillator described in paragraph 2-51a.

b. *Peak Limiters and Amplifier Circuits.* Linear amplifiers A2 and A3 are used as peak limiter circuits. The purpose of the peak limiter circuits is to prevent the input signals from exceeding a predetermined level. Peak limiting is accomplished by utilizing the diode

characteristic of the linear amplifier. Above a predetermined value the output of the amplifier follows the limiting action of the silicon diode. Voltage regulator VR1 provides a regulated supply voltage for the peak limiter circuits. Handset H-156/U orderwire, 1.1 kHz test tone, or the 4 kHz oscillator test signal is applied to amplifier A2 (peak limiter A) through capacitor C7 and resistor network R19 and R24. The proper handset level is obtained through voltage divider network R16 and R17. Resistors R14 and R15 provide proper input levels for the 4 kHz and 11 kHz signals. Resistor R23 minimizes input offset voltage and R25 sets the operating point of amplifier A2 to provide the proper peak limiting. Minimum output offset voltage is obtained with R26. The output of peak limiter A is coupled through capacitor C6 and resistor R27 to potentiometer R28. The remote phone orderwire hybrid input, ring input 1.6 kHz, or the 4 kHz test signal is applied to amplifier A3 (peak limiter B) through resistor divider networks R29 through R33. These inputs are coupled to peak limiter B through capacitor C9 and resistors R34 and R37. Operation and component function for peak limiter B is identical to that for peak limiter A above. The +6 volts required for the peak limiters is established in VR1 by resistors R35 and R36. Resistor R38 is a current limiting resistor and capacitor C10 reduces output noise. The 6 volt output of VR1 is filtered by capacitor C11 and is applied to peak limiters A and B through blocking diode CR2. The output of peak limiter A appears across potentiometer R28 and is coupled to amplifier AS (pin 1) through capacitor C13. Peak limiter A output is also applied to orderwire amplifier No. 2 through pin F. The output of peak limiter B appears across potentiometer R43 and is coupled to amplifier A5 (pin 2) through capacitor C14 and to orderwire amplifier No. 6 through pin 6. Amplifier AS provides a gain of 100. Operation and component function of amplifier A5 is identical to amplifier 1A13A3A1 (para 2-53b). The output of amplifier A5 appears across potentiometer R50 and is coupled to amplifier A4 (pin 1) through capacitor C21 and to orderwire amplifier No. 3 through orderwire amplifier No. 5 inputs are supplied to amplifier A4 (pin 2) through capacitor C22. Amplifier A4 provides a gain of 100 and is identical to amplifier A6. The output of A4 is applied to the transmitters orderwire circuits (TO RADIO OW) through capacitor C26, impedance matching resistor R6, 3kHz low pass filter FL1, transformer T1, and output pins 13 and 14. Filter FL1 sharply attenuates signals above 3kHz; consequently, the 4 kHz test signal is not applied to the transmitter

orderwire circuits. Transistor circuit Q2 is used as a sidetone amplifier and is connected between the transmit and receive elements of Handset H156/U. The transmitted signal from Handset H156/U is applied to the base of Q2 by pin R and capacitor C8. The output of Q2 (emitter follower configuration) is applied to the receive element of Handset H-156/U through resistor R22 and pin S. Resistors R20 and R21 provide the proper bias for transistor Q2. Dc power is supplied to the microphone of Handset H-156/U through dropping resistor R18.

**2-56. Electrical Frequency Synthesizer 1A14 Circuit Functioning**

Electrical frequency synthesizer 1A14 provides an rf output frequency in the range of 284.275 MHz to 303.125 MHz. The 1A14 output is applied to transmitter amplifier-frequency multiplier 1A11 in the T1054/GRC-144 and to amplifier-frequency multiplier 2A10 in the R-1467/GRC-144. Figure 5-45, electrical frequency synthesizer 1A14 interconnecting diagram, shows the chassis mounted components and plug-in component connections. The circuit theory for the plug-in components is given in paragraphs 2-57 through 2-64. All circuit theory and associated illustrations also apply to electrical frequency synthesizer 2A14 in Receiver, Radio R1467/GRC-144.

*a. Thumbwheel Switches.* Four thumbwheel switches: S1-I (S1-II dummy), S1-III, S1-IV, and S1-V (fig. 5-45(1)) provide +6 vdc return (ground) connections to the switch gate inputs of variable frequency dividers and 1A14A5 in accordance with their settings; the contact configurations for each thumbwheel switch setting are indicated below. An X indicates the switch closed position which applied a +5 vdc return (ground) line to the associated switch gated input.

(1) S1-I.

Contact	Setting						
	44	45	46	47	48	49	50
B		X		X	X		
C	X		X		X		

(2) S1-III.

Contact	Setting									
	0	1	2	3	4	5	6	7	8	9
A	X						X	X	X	X
B	X	X						X	X	X
C	X	X	X						X	X
D	X	X	X	X						X
E	X	X	X	X	X					

(3) S1-IV or S1-V.

Contact	Setting									
	0	1	2	3	4	5	6	7	8	9
1		X		X		X		X		X
2			X	X			X	X		
4					X	X	X	X		
8									X	X

*b. Indicator Lamps.* Two power indicator lamps on electrical equipment chassis 1A14A10 indicate the presence of the +28 volt and +6 volt power from power supply 1A14A8. Operational indicator lamps are provided on plug-in components 1A14A1-1A14A6. A lighted (red) lamp indicates a failure in the associated plug-in components.

*c. Integrated Circuit Z1.* Integrated circuit Z1 (type 933) provides a diode distribution network for the +5 volt lamp test signal. Pressing TEST pushbutton S2 applies 5 volts dc to this network which, in turn distributes it to the individual operational indicator lamp bias circuits.

*d. Relay Circuit.* Relay K1 is controlled by application of power to the crystal oven in standard rf oscillator 1A14A7. Relay K1 is shown in the deenergized position which indicates that the crystal oven has reached its operating temperature.

When the crystal oven is not at its operating temperature, 28 volts dc is applied to the relay coil from pins 4 and 6 of plug XA7. This energizes relay K1 and provides an open circuit at pins A3, B3, causing the SYNTH OVEN indicator on meter panel assembly 1A15A8 to go out.

**2-57. Radio Frequency Oscillator 1A14A1 Circuit Functioning (fig. 5-46)**

*a.* Power (+28 volts dc) from power supply 1A14A8 is applied through pins 1 and 5 of connector P1 to terminal E12 on board A3 and to the input of voltage regulator VR1. This regulator produces 21 volts + 1 percent which is applied to radio frequency oscillator (vco) Y1 through rf choke L13, to board A4 through rf choke L4 and to board A2. RF feedthroughs FL1, FL2, and FL3 filter rf currents which might adversely affect the circuit operation.

*b.* The rf output frequency generated by the radio frequency oscillator Y1 is determined by the vco bias voltage produced in audio frequency phase error detector 1A14A3 and applied through coaxial connector P1-A3 and terminal E1. The

vco bias voltage is between 5.0 and 16.0 volts dc. The rf output is applied to board A4 (buffer amplifier) through terminal E18 and to board A2 (digital amplifier) through terminal E3 and R8.

c. The rf signal applied to board A4 is applied to the base of transistor Q4 through the isolating network consisting of resistors R19, R20, and R21, and coupling capacitor C14. The level of this signal is set by selecting the value of R20, the nominal value of which is 270 ohms. The amplified rf signal is direct coupled from the collector of Q4 to the base of transistor Q5 where it is further amplified to the required level (20 milliwatts). The output of Q5 is developed across autotransformer T2 and coupled through capacitor C19 to the isolating network consisting of resistors R29, R31, and R32. The rf output (high) to the main chassis is developed across R32 and routed through terminals E21 and E22 and coaxial connector P1-A1. The nominal rf output into a 50 ohm load is 20 milliwatts. The sinusoidal rf signal frequency is between 284.3750 and 303.1250 MHz. Part of the rf output developed by Q5 is rectified by diode CR3 and filtered by capacitor C20 to supply the meter current which is applied to meter panel assembly 1A15A8 through the main chassis. The nominal meter current is 25 microamperes for 20 milliwatts into 50 ohms. The value of resistor R33 is also determined during final test and its nominal value is 62K ohms.

d. The rf signal applied to board A2 is routed to the base of transistor Q1 through resistor R8, transformer T1, and capacitor C8. Transformer T1, and capacitor C7 comprise a bandpass filter so that signals outside the 284.375 to 303.125 MHz range are excluded. The signal is amplified by Q1 and is capacitively coupled by C4 to the base of emitter follower Q2. An emitter follower output, rf output (low), is developed across resistor R12 and routed through capacitor C10, terminal E7 and E8, and coaxial connector P1-A2 to electronic frequency converter 1A14A2. The nominal sinusoidal rf output from the emitter follower is 225 millivolts rms into 50 ohms. The collector signal of Q2 is rectified by lamp detector diode CR1 and filtered by capacitor C6. Resistor R7 provides the operational indicator lamp bias at terminal E6 which is applied to board A3.

e. The normal lamp bias voltage applied to terminal E13 is negative, keeping transistor Q8 nonconducting. Likewise, the transistor in lamp

assembly DS1 is non-conducting. Bias diode CR2 is a temperature-compensating diode cluster which varies the base voltage on QS in accordance with the voltage variations between the base emitter junctions in DS1 and Q8 caused by temperature variations. For example, if the temperature decreases, the base voltage of Q3 could become positive and Q3 may then conduct, which could cause the transistor in assembly DS1 to conduct, and light the lamp. If the rf output signal from board A2 is decreased, the bias on Q8 becomes positive and it conducts, causing the transistor in assembly DS1 to conduct and light the indicator lamp. When the TEST pushbutton on the main chassis is pressed, a 5 volt lamp test signal is applied via pin P1-4, terminal E16, and resistor R16, to base of the transistor in DS1, causing it to conduct and light the indicator lamp.

### **2-58. Electronic Frequency Converter 1 A14A2 Circuit Functioning (fig. 547 and 5-48)**

Electronic frequency converter 1A14A2 is comprised of printed wiring board assemblies (1A14A2A1 and 1A14A2A2). Board 1A14A2A1 contains the if amplifier-mixer circuits and is shown in figure 5-47. Board 1A14A2A2 contains the amplifier-multiplier circuits (fig. 5-48) and provides a 128 MHz signal to 1A14A2A1.

a. The rf output (low) frequency from radio frequency oscillator 1A14A1 is applied to board 1A14A2A1 (fig 547) through coaxial connector P1-A1, terminals E7 and ES, capacitor C2, and steering diodes CR1 and CR2 to a high-speed divide-by-two circuit consisting of transistors Q1, Q2, and Q3. The divide-by-two circuit operates as an astable multivibrator. The free running frequency of the astable multivibrator is locked to the first subharmonic of the rf input frequency. The switching is performed by Q1 and Q2; transistor Q3 provides a constant current input to the emitters of the switching transistors. The output frequency from the divide-by-two circuit Q1 through Q3 is amplified by rf amplifiers Q4 and Q5. Diode CR3 provides temperature compensation for the base-emitter junction of rf amplifier Q4. The output from rf amplifier Q5 is coupled through capacitor C17 to the local oscillator input port (terminals) of mixer Z1. A 128 MHz signal from board 1A14A2A2 is also applied

to Z1 signal input port (terminal 1) through terminal E4 and resistor R22. The value of R22 is selected to provide a minimum if output level. The nominal value of R22 is 390 ohms. The mixer output is an intermediate frequency in the range from 14.1875 to 23.5625 MHz which is amplified by video amplifiers Q6 and Q7 and routed to variable 1 frequency divider 1A14A4 through transformer T2 and coaxial connector P1-A2 (if output).

b. The signal in the secondary of T2 is also monitored to provide lamp bias. The signal is rectified by diode CR6 and the resultant negative voltage keeps transistor Q8 nonconducting which holds the transistor in assembly DS1 nonconducting, causing the failure lamp DS1 to go off. When the rf output signal amplitude falls below 1.8 volts peak-to-peak, the positive bias causes lamp driver Q8 to conduct which in turn causes the transistor in DS1 to conduct and light the indicator lamp DS1 (red). Pressing the TEST pushbutton on the main chassis applies a 5 volt lamp test signal through pin P1-3, terminal E9, and resistor R33, to the base of lampdriver Q8 causing it to conduct and test that the lamp circuit is functional.

c. Regulator diode CR5 and resistor R17 reduce the 28 volt power input to a regulated 6.2 volts for the divide-by-two circuit Q1 through Q3 rf amplifiers Q4, Q5, and lampdriver Q8.

d. The 8MHz signal from standard radio frequency oscillator 1A14A7 is applied to board 1A14A2A2 (fig. 5-48) through coaxial connector P1-A3, terminals E1 and E2, an isolation pad consisting of resistors R1, R3, and R16, and capacitor C1 to the base of multiply by two transistor Q1. The output from Q1 is doubled to 16 MHz and doubled again in second stage multiply by two Q2 to 32 MHz. The output from Q2 is quadrupled by multiply by four stage Q3 from 32 MHz to 128 MHz. The 128 MHz output from Q3 is applied through emitter follower Q4 and capacitor C23 to the signal input of the mixer on board 1A14A2A1. The 128 MHz output is developed across resistor R15. Rf is filtered from the +28 volt input by rf choke L5 and rf bypass capacitors C11, C16, and C17.

## 2-59. Audio Frequency Phase Error Detector 1A14A3 Circuit Functioning (fig. 5-49)

a. The 1.5625 kHz reference signal from fixed frequency divider 1A14A6 is applied through pins P1-2 and P1-8. terminals E9 and E10, and resistor R17 to transformer T1. Diode CR7 prevents spurious signals from being applied to T1. The 1.5625 kHz reference signal consists of one microsecond positive-going pulses which cause sawtooth generator Q4 to conduct and discharge capacitor C9. The voltage across C9 is the fundamental sawtooth waveform. A constant current generator comprised of transistor Q3, resistors R5, R6, and R7, capacitor C4, and temperature compensating diode CR3, charge C9. The value of R7 is selected at final test to correctly set the peak amplitude of the sawtooth and its nominal value is 120k ohms. The threshold voltage from which C9 starts charging is the voltage developed across capacitor C8 which is determined by the  $2^0$  and  $2^1$  correction code input signals from the fixed frequency divider which are applied through pins P1-6 and P1-16, terminals E8 and E7, and resistors R12 and R11 to digital to analog converter Q9 and Q8, respectively. The voltage developed across C8 is determined by the voltage divider consisting of diodes CR4, CR5, and CR6 and resistors R13 through R16. In addition, diode CR4 provides temperature compensation. The voltage developed across C8 is the voltage across CR4 and R13; these form one part of the parallel voltage divider. The parallel combination of resistor R14 and R15 in series with diode CR5 form the second part, and resistor R16 in series with diode CR6 form the third part of the voltage divider. When both transistors Q8 and Q9 of digital to analog converter are nonconducting ( $2^0$  and  $2^1$  are both logic zeros), current flows through the three parallel parts of the voltage divider and is maximum. When  $2^1$  is a one level. Q8 is conducting and CR5 is reverse biased. For this condition, no current flows from R15 into R13 causing the voltage across CR4 and R13 to be reduced. When  $2^0$  is a one level, Q9 is conducting and CR6 is reversed biased. For this condition, no current flows from R16 into R18 causing

the voltage across CR4 and R13 to be further reduced. The lowest voltage is developed across CR4 and R13 when both Q8 and Q9 are conducting (2 and 2° are both a one level); then, the only path for current is through R14. Since R16 is twice R15, the voltage charge with Q9 conducting is half the voltage change when Q8 conducts. The correction code can be 00, 01, 10 or 11; a logic zero corresponds to zero volt (transistor nonconducting;) a logic one corresponds to 5 volts (transistor conducting). The maximum, sawtooth starting voltage corresponds to an input code of 00; it gets progressively lower from 01 to 10 and is minimum for code 11. Varying the starting voltage of the sawtooth waveform step changes the vco bias voltage. The vco bias voltage is applied to the radio frequency oscillator 1A14A1. This results in a faster return to the phase locked condition or faster frequency capture. The voltage developed across C8 and C9 is applied to the input of buffer stage Q5 and Q6 which buffer the step level and sawtooth to the input of the sample and hold circuit.

b. The sample and hold circuit consists of transistor Q7, which gates the composite signal, and capacitor C14, which stores (or holds) the gated voltage level. Transistor .Q7 is a dual emitter gate which has a low resistance bi-directional conduction path between the two emitters when a positive voltage is applied between the collector and base. The gate is opened by the divide-by-N pulses which are applied through pins P1-13 and P1-14, terminals E11 and E12, and resistor R19 to transformer T2. Diode CR8 prevents spurious signals from being applied to T2. During normal phase-locked operation, the divide-by-N and the 1.5625 kHz reference are both the same frequency; therefore. the gate will open at the same ramp point of the sawtooth, thus keeping the charge on C14 constant and the vco bias voltage steady. Capacitor C14 charges or discharges through Q7 to the incoming sawtooth voltage while the gate is open and stores the voltage. Transistors Q10 and Q11 are a unity gain buffer amplifier and Q18 and Q18 act as complementary pair dc amplifier. The resulting vco bias voltage is filtered by the network consisting of resistors R28 through R31 capacitors C12, C18, C16, and C17. This network is a parallel-Tee filter with maximum rejection at 1.5625 kHz. The output is coupled to radio frequency oscillator 1A14A1 through terminals E14 and E16 and coaxial connector P1-A1. The range of dc control is set at final

test by selecting the value of resistor R32. The nominal value of resistor R32 is 470k ohms.

c. The sawtooth waveform at the output of buffer Q5 and Q6 produces a bias for lamp DS1. The positive sawtooth signal keeps ac detector Q1 conducting which keeps the transistor in the DS1 assembly nonconducting. If the sawtooth signal is not present the base of ac detector Q1 becomes zero and is turned off. This will cause the transistor in assembly DS1 to conduct and light the failure indicator DS1 lamp red. Pressing the TEST pushbutton on the main chassis applies a 5-volt lamp test signal to pin P1-8, to terminal EI through resistor R3, and to the base of the transistor in DS1 which lights the lamp.

d. Diodes CR2 and CR10 and transistor Q2 form a voltage regulator which converts the 28 volt input to 20 volts. Only the transistors in the lamp circuits operate directly from the 28-volt supply in order to isolate the vco bias voltage from any spurious variations.

## 2-60. Variable 1 Frequency Divider 1A14A4 Circuit Functioning (fig. 5-0)

### NOTE

**Variable 1 frequency divider 1A14A4 contains integrated circuits designated Z1 through Z18. Integrated circuit types M(C932, 949, 950, 983, 9002, and MSC6847L are used. These circuits are shown functionally in figure 5-0. A circuit diagram for each of these circuits is provided in figure 5-24.**

a. Variable 1 frequency divider 1A14A4 contains two printed wiring boards A11 and A2 which provide the following circuits: clamp circuit CR1, driver Q1, divide-by-two circuit Z1, two 0.1 MHz and 1 MHz cascaded divide-by-ten counter registers, control flip-flops and gates. The if output frequency from 1A14A2 is applied to divide-by-two Z1, through clamp circuit diode CR1 and driver Q1. The output from terminal 11 of divide-by-two circuit Z1 is applied to input inverter Z2 with the final inverted output from Z2 applied to the first stage (Z6) of the divide by-ten counter registers. The output pulsed from input inverter 72B are the clock pulses for the cascaded divide-by-ten counter registers. The

registers count down the clock pulses until the reset enable signal from variable 2 frequency divider 1A14A6 is received and the registers contain the unique number (1 MHz register contains 0100-decimal 4, 0.1 MHz register contains 0100-decimal 6). After the unique number count, the initialize, inhibit, and preload sequence (8 counts) takes place. During the initialize, inhibit, and preload periods, the clock pulses are prevented from being counted. The 0.1 MHz and 1 MHz register stages are set to all ones during the initialize period, the count (all ones) in the counter registers is modified in accordance with the 1 MHz and 0.1 MHz thumbwheel switch settings. After the preload period, the clock pulse are no longer inhibited and the count (determined by thumbwheel switch settings) in the registers is decremented by the incoming clock pulses. The counter registers count down through zero until the reset enable signal is received from 1A14A6 and the unique number again appears in the registers. The cycle then repeats as described above.

b. The 0.1 MHz and 1 MHz divide-by-ten counter registers on board A2 are binary coded decimal (BCD) counters. The 0.1 MHz divide by-ten counter register is comprised of integrated circuits Z6 (least significant bit) Z8, Z710, and Z12 (most significant bit). The 1 MHz divide by-ten counter register is comprised of integrated circuits Z18 (least significant bit), Z16, Z17, and Z18 (most significant bit). The registers are cascaded: the clock pulses are applied to the first stage D6 -of the 0.1 MHz register; the output stage 112 of the 0.1 MHz register triggers the first stage Z13 of the 1 MHz register; the output stage Z18 of the 1 MHz register is inverted through count inverter Z14C and the output .(count) is applied to the first stage of the 10 MHz register in variable 2 frequency divider 1A14A5. The 0.1 MHz and the 1 MHz divide-by ten counter registers in 1A14A4 count down in accordance with the following chart. It should be noted the chart lists the state of each register stage for 99 through 90. For 89 through 00 the standard binary logic regression applies.

1MHz divide-by-ten register stages				0.1 MHz divide-by-ten register stages				Decimal equivalent
Z18	Z17	Z15	Z14	Z13	Z10	Z8	Z6	
0	0	0	0	0	0	0	0	00
1	0	0	1	1	0	0	1	99
1	0	0	1	1	0	0	0	98
1	0	0	1	0	1	1	1	97
1	0	0	1	0	1	1	0	96
1	0	0	1	0	1	0	1	95

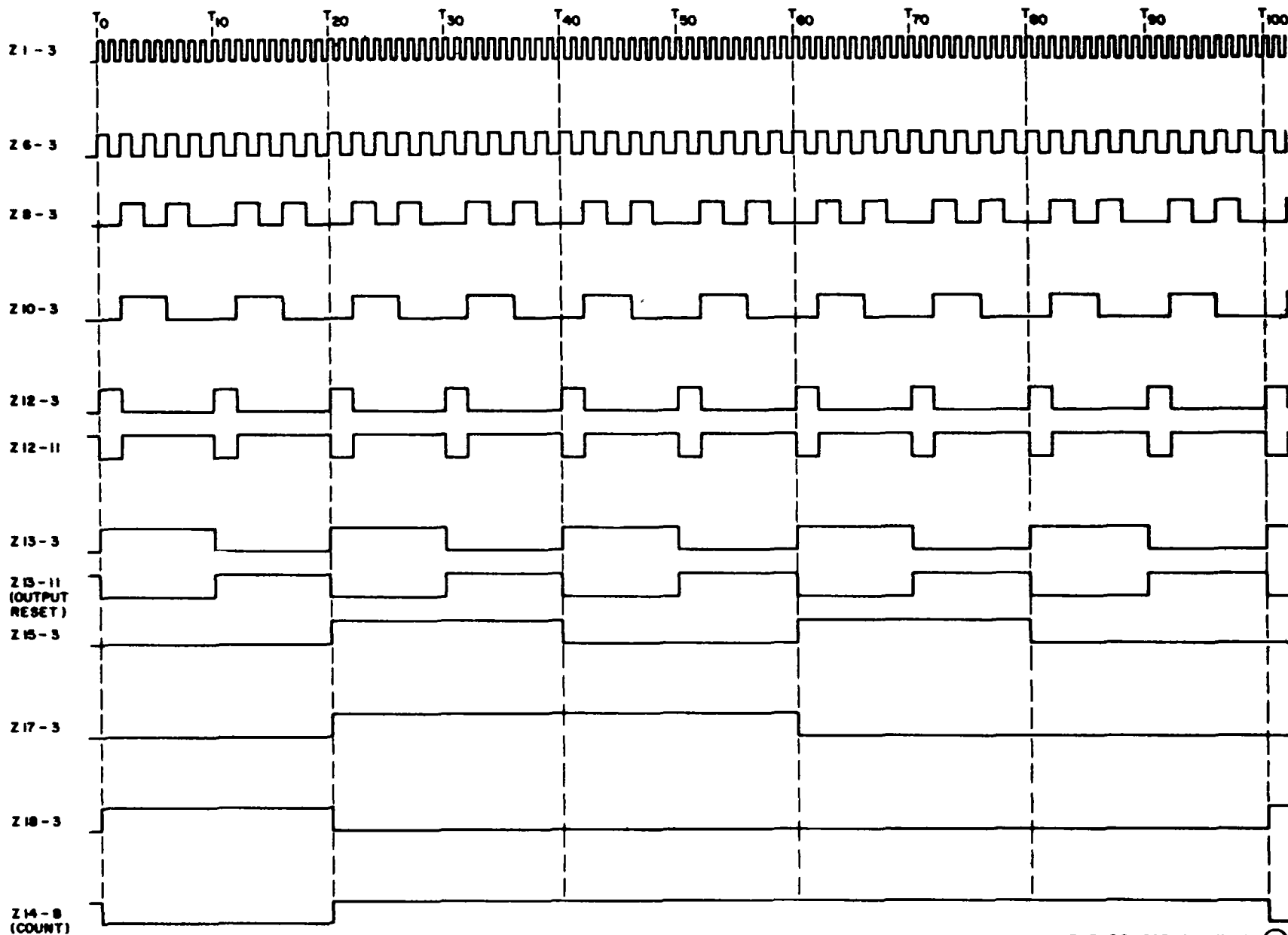
1MHz divide-by-ten register stages				0.1 MHz divide-by-ten register stages				Decimal equivalent
Z18	Z17	Z15	Z14	Z13	Z10	Z8	Z6	
1	0	0	1	0	1	0	0	94
1	0	0	1	0	0	1	1	93
1	0	0	1	0	0	1	0	92
1	0	0	1	0	0	0	1	91
1	0	0	1	0	0	0	0	90
0	0	0	0	0	0	0	0	00

c. The following is a description of the divide by-ten registers (BCD down counters). As stated previously, the output from stage Z12 of the 0.1 MHz divide-by-ten counter register triggers the first stage of Z18 of the 1.0 MHz divide-by-ten counter registers. Assume that integrated circuits Z18, Z15, Z17, and Z18 are all reset (0000). The first negative going transition from Z12 sets Z1 and Z18 (1001: ). To set a flop-flop type 950 pin 4 must be at a 0 volt level; to reset the flip-flop, pin 10 must be at a 0 volt level. If the count is 0000, only Z13, Z17, Z18 are conditioned to be set; however, since Z15 does not change, no transition will be applied to Z17. The second negative-going transition from Z12 resets Z18 (1000). At this time, the input to pin 9 of NAND gate Z11B is a low (0 volt) level and pin 8 is a high (5 volt) level; this now satisfies the two ones requirement of NAND gate Z16D, since pins Z16D-12 and 13 are both high. The third negative-going transition from Z12 sets D18, Z16, and Z.17 and resets Z1 (0111). The fourth negative-going transition from Z12 resets Z13 (0110). The fifth negative-going transition from Z12 sets Z13 and resets 715 (0101). The sixth negative-going transition from Z12 sets Z13 and Z15 and resets Z17 (0100). The eighth negative-going transition from Z12 resets Z13 (0010). The ninth negative-going transition from Z12 sets Z13 and resets Z15 (0001). The tenth negative-going transition from Z12 resets Z13 (0000).

d. Variable 1 frequency divider 1A14A4 divides the if output frequency from 1A14A2 by 200 (one divide-by-two flip-flop, and two divide by-ten counter registers). Thing for the divide by-200 operation is shown in figure 2-18, part 1.

The clock pulses from Z1 are the if output frequency from 1A14A2 divided by two. The waveform at pin 8 (set output) of each register stage is shown from the time T. through T. (T is the period of the clock pulse). Pin 11 of Z12 is also shown since the negative-going transition of this output causes Z12 (input stage of the second divide-by-ten counter) to trigger. The width of the count signal at pin 8 of output inverter Z14C





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Figure 2-18(1). Variable 1 frequency divider 1A14A4, timing diagram (part 1 of 2).

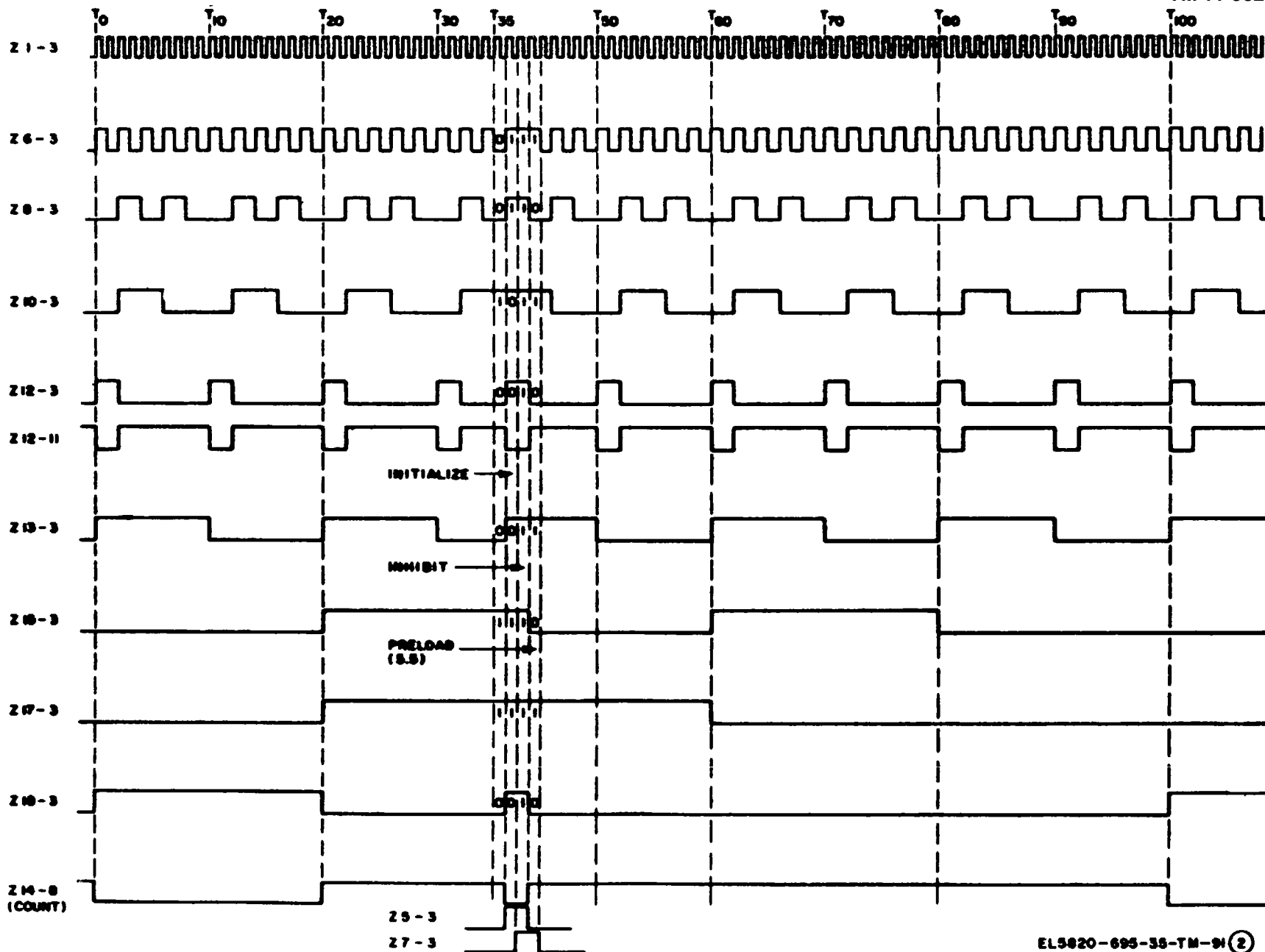


Figure 2-18(2). Variable 1 frequency divider 1A14A4, timing diagram (part 2 of 2).  
2-100

is equal to 20 periods of the incoming clock pulses (40 periods of the if output frequency from 1A14A2). The repetition rate of the count signal at Z14C-8 is equal to 100 periods of the clock pulses (200 periods of the if output frequency from 1A14A2). The time from T<sub>1</sub> to T<sub>2</sub> is the width of the count pulse applied to variable frequency divider 1A14A6. Z18 pin 11 provides the output reset signal which is used in 1A14A5 to control the width.

e. The registers in 1A14A5 contain the most significant bits and will reach their unique number before the registers in 1A14A4 have reached their unique number. When the registers in 1A14A5 count down to the two most significant digits of the unique number, the reset enable signal is decoded in 1A14A5 and is applied to 1A14A4. The reset enable signal is applied as a low (0-volt) level to NAND gate Z14A in 1A14A4. It is inverted to high (-volt) level and applied as one input to NAND gates Z3A and Z3B. At time R85 (fig. 2-18(2)) the count in registers Z18 (most significant bit), Z17, Z16, Z18, Z12, Z10, Z8, and Z6 (least significant) bit is 011100100. Since control gate Z3 has been provided by the reset enable signal from 1A14A5, this count, which is the unique number (decimal 64), will be decoded by gates Z3A, Z3B and provide a logic zero level to Sea-. The following positive going transition from Z1-11 will set Z5, causing gate Z2A to produce a zero level initialize signal. The initialize signal sets all register states to all "ones" and is sent to 1A14A5. The next count applied to Z6 by Z2B is inhibited by the one level applied to pin ten of Z6 by the output of NAND gate Z4B. However, the count transition from Z2B is applied to flip-flop Z7 which sets it. The inhibit signal becomes a zero level that is applied to pin 3 of NAND-gate Z4B. The next count transition applied to Z6 from gate Z2B is, therefore, also inhibited, but it resets flip-flop Z5 and produces a zero level output from NAND gate Z2C which is inverted by gate Z2D to produce a one level preload signal. The preload signal is applied to the switch gates in this module and in 1A14A6 causing the thumbwheel switch settings to be gated into the registers. This is illustrated in figure 2-18(2), where the assumption is made that the 1 MHz and 0.1 MHz thumbwheel switch sections on the main chassis are each set at position 5. With the switches in this position, the 4 and 1 inputs to the switch gates Z9B, Z16B and Z4C, Z9D are a zero level (grounded through the switch sections). The 8 and 2 inputs are not TM 11-5820-6955 grounded and are a one level (5 volt); these input levels

are inverted in their associated gates and set the state of associated flip-flops; for this example, the count becomes 01010101. The next incoming clock pulse will reset control flip-flop Z7 and remove the inhibit signal on gate Z4B. Starting with the next clock pulse from Z2B, stage Z6 will start counting down. This operation continues until all the register stages again reach zero.

f. The start of the count down for stage Z6 can be delayed by one clock period depending upon the setting of the least significant bit (1) of the 0.1 MHz switch. The timing associated with this operation is shown in figure 2-19. As Z6-11 goes to a logic one state at time 35, it raises Z3B-10 to logic one forcing Z5-4 to a logic zero. This conditions Z5 to be set on the next clock pulse. Therefore, the next clock pulse (time 36) from Z2B-6 sets Z5-3 to a one. Since Z5-11 is zero, Z4B-4 is also zero. For this condition, stage Z6 is stopped from counting and Z-8 remains a logic one. Z74-3 is forced to a one on the next clock pulse. This places a one on Z4C-9. The next clock pulse from Z2B-6 raises Z-11 to a one causing Z4B-4 to also be a logic one. This imposes the following levels on Z4C; pin 10 is one, pin 9 is one. The output at Z4C-8 now depends on whether a one or a zero condition is programmed in on Z4C-11-1 from the least significant bit (1) from the 0.1 MHz thumbwheel switch. If a logic one is programmed in, Z4C-8 will go to a zero allowing Z6-3 to switch off (logic zero) at the next clock pulse. If a zero is programmed in, Z4C-8 will go to a one, thereby keeping Z6-3 at a high level when the next clock pulse occurs, and not changing state until the following clock pulse (T<sub>2</sub>). The effect of the delay is to change the total count by the addition of two counts.

g. The count output pulses at output pin 11 of flip-flop Z18 are monitored by a lamp bias circuit. A negative voltage is developed at the base of the transistor in lamp assembly DS1 by diodes CR2 and CR8 which keeps the transistor nonconducting and the failure lamp extinguished. The negative bias voltage is produced by capacitor C11 discharging through diode CR8 and charging capacitor C12 in a negative direction with respect to ground (+5V RET). If the count signal is not present, the base of the transistor in lamp assembly DS1 becomes positive through resistor R12 and the transistor conducts, lighting the failure indicator lamp DS1 red.

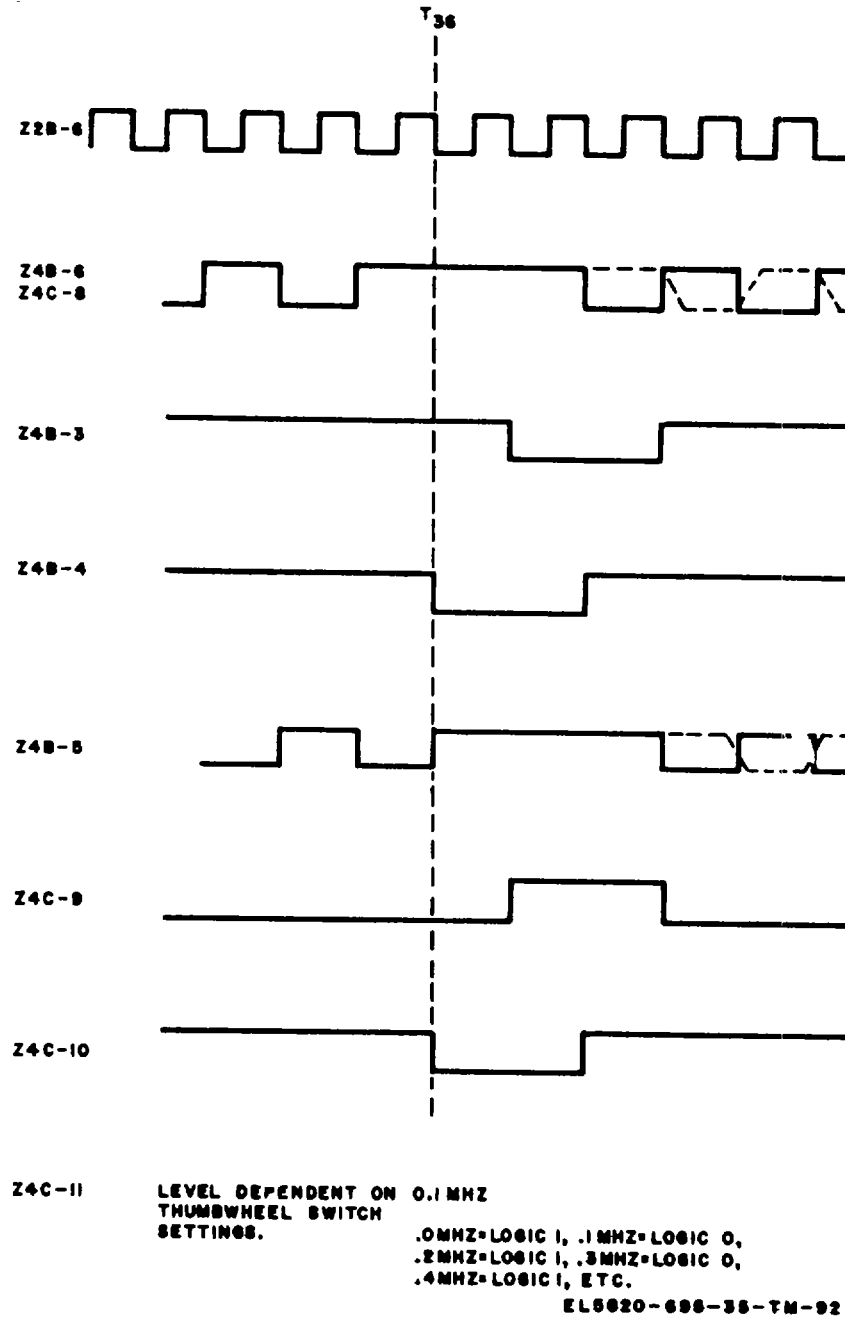


Figure 2-19. 1A14 timing diagram, 0.1 MHz thumbwheel switch.

Pressing the TEST pushbutton on the main chassis applies a +5 volt lamp test signal to pin P1-1, terminal E19, and resistor R18 to the base of transistor in DS1, lighting the lamp red.

**2-61. Variable 2 Frequency Divider 1A14A5 Circuit Functioning (fig. 641)**

**NOTE**

Variable 2 frequency divider 1A14A5 contains integrated circuits designated Z1 through Z10 and Z12 through Z14. Integrated circuit types MC932, 946, and 960 are used. A

circuit diagram for 2-102 each of these circuits is shown in figure 6-24.

a. Variable 2 frequency divider contains one printed wiring board A1 which provides the following circuits: 10 MHz divide-by-ten counter registers Z2 through Z6, 100/1000 MHz divide by-eight ripple through counter registers Z7 through Z9, an output register Z10, and switch and control gates. The count signal from variable 2 frequency divider 1A14A4 is applied to the divide-by-ten counter registers Z2 through Z6. The output from the divide-by ten counter registers Z2 triggers the divide-by-eight counter register

The output (divide-by-N pulses) from stage Z10 of the divide-by-eight registers is applied through output inverter stage Z18 to fixed frequency divider 1A14A6 and to af phase error detector 1A14A3. If the count in the 1A14A5 registers was not programmed by the thumbwheel switch settings (10 MHz, 100 MHz, and 1000 MHz) and the control logic in variable 2 frequency divider 1A14A4, they would divide the count pulses by 80 (10 x 8). Both variable frequency dividers 1A14A4 and 1A14A5 would divide the if output frequency from 1A14A2 by 16,000 (200 x 80) if they were not programmed. The registers in 1A14A5 count down the count pulses from 1A14A4 until the registers contain the unique number (divide-by-eight register contains 111-decimal 7 and divide-by-ten register contains 11110-decimal 4). The binary to decimal relationships are described later in this paragraph. Once the registers contain the unique numbers, the reset enable signal is applied to 1A14A4 to produce the initialize, inhibit, and preload sequence (3 counts). The initialize signal from 1A14A4 insures that registers are at the required count for setting in a number from the thumbwheel switches. The inhibit signal from 1A14A4 prevents the divide-by-eight register from accumulating a false count. The preload signal modifies the count ((11111110) in the registers in accordance with the 10 MHz, 100 MHz, 1000 MHz thumbwheel switch settings. The modified count in the registers reduces the time between the divide-by-N output pulses. After the preload period, the count (determined by thumbwheel switch settings) in the registers is decremented by the incoming count pulses from 1A14A4. The registers count down through zero until the unique number appears again in the registers. The cycle then repeats as described above.

b. The 10 MHz divide-by-ten register stages Z2 through Z6 operate as a Johnson Counter (shift register). The 100/1000 MHz divide-by eight ripple-through register stages Z7 through Z9 operate as a standard three stage nonsynchronous binary counter. These register stages count down in accordance with the following chart. It should be noted the chart lists the state of each register stage for 79 through 70. For 69 through 00 the standard binary logic regression applies.

c. The following describes the operation of the divide-by-ten register (Johnson Counter). The count pulses from 1A14A4 are applied to the divide-by-ten register. It is assumed that register stages Z2 through Z6 are reset (00000). The first negative-going count transition sets register stage Z2 (00001). To set a flip-

flop type 950, pin 4 must be at a low (0-volt) level. When the registers state is 00000, only Z2 is conditioned by Z6 to be set; stages Z3 through Z6 are conditioned to be reset, but, since they are already reset, their status is not changed. After Z2 has been set its outputs condition Z3 to be set. The second incoming negative-going count transition sets Z3 (00011); the third negative-going count sets Z4 (00111); the fourth negative-going count sets Z5 (011(11); and the fifth negative going count sets Z6 (11111).

100/1000 MHz divide-by-eight register stages			10 MHz divide-by-ten register stages (Johnson Counter)					Decimal equivalent
Z9	Z8	Z7	Z6	Z5	Z4	Z3	Z2	
0	0	0	0	0	0	0	0	00
1	1	1	0	0	0	0	1	79
1	1	1	0	0	0	1	1	78
1	1	1	0	0	1	1	1	77
1	1	1	0	1	1	1	1	76
1	1	1	1	1	1	1	1	75
1	1	1	1	1	1	1	0	74
1	1	1	1	1	1	0	0	73
1	1	1	1	1	0	0	0	72
1	1	1	1	0	0	0	0	71
1	1	1	0	0	0	0	0	70
0	0	0	0	0	0	0	0	00

Setting Z6 primes the reset input pin 10 of stage Z2. The next five negative-going counts will advance the one through the reset side of register stages Z2 through Z6 and eventually return the registers to 00000.

d. The 10 MHz divide-by-ten counter Z2 through Z6 is a Johnson Counter or shift register. Stages Z6, 05, Z4, Z5, and Z2 are programmed by the A, B, C, D, and E inputs respectively from the 10 MHz thumbwheel switch. The divide-by-eight ripple-through counter Z7 through Z9 is a three stage nonsynchronous binary counter. Stages Z8 and Z7 are programmed by the B and C inputs respectively from the 100/1000 MHz thumbwheel switch. Stage Z9 (most significant bit) is not programmed; the programmed input (reset) is connected permanently to logic 1 (+5 vdc). Because the reset input to Z9 is permanently connected to a logic one, the lowest number that can be programmed into the divide-by-eight register is decimal 4 or 100 binary.

e. If the count was not programmed by the control logic in variable 1 frequency divider 1A14A4

and the thumbwheel settings, the registers in 1A14A5 would divide the count pulses from 1A14A4 by 80 as illustrated in figure 552. The count pulses are shown across the top of the diagram from time  $T_0$  through  $T_{8000}$  ( $T$  is the period of the clock pulses applied to the registers in 1A14A4). Note that the repetition rate of the count pulses is equal to 100 periods of the clock pulses. The waveform at pin 8 (set output) of each register stage is shown from time  $T_0$  through  $T_{8000}$ . Immediately preceding time  $T_0$  all register stages Z2 through Z10 are zero; at  $T_0$  the negative-going count transition sets Z2 which, in turn, sets Z7 through Z10. When Z10 is set the divide-by-N output pulse starts. When Z2 is set it conditions Z10 to be reset, and, when the output reset signal from variable 1 frequency divider 1A14A4 is applied to Z10 (40 time periods of the incoming if frequency; time  $T_{20}$ ), Z10 is reset and terminates the divide-by-N pulse. The count continues (assuming registers are not programmed) through time  $T_{8000}$  and the cycle is repeated.

f. The following describes how the count in the 1A14A5 registers is modified by the control signals from variable 1 frequency divider 1A14A4 and the 10 MHz, 100 MHz, and 1000 MHz thumbwheel switch settings. The timing for the modified (jump) count is illustrated in figure 2-20. The count pulses are shown across the top of the diagram. The count from time  $T_0$  until  $T_{500}$  is the same as described in the previous paragraph. At the time  $T_{500}$ , the count in the registers Z9 through Z2 is 11111110 which is the unique count (decimal 74). For this condition, the inputs to the reset enable gate Z1A and diode CRS are all at a high (65 volt) level. Gate Z1A produces a low (0 volt) level which is the reset enable signal applied to variable 1 frequency divider 1A14A4. Variable 1 frequency divider 1A14A4 will produce the initialize signal (a low (0-volt) level) which resets Z2 and sets Z5 through Z6 and Z9. One clock pulse later variable 1 frequency divider 1A14A4 will produce the inhibit signal (a low (0-volt) level) which is inverted by gate Z14C and prevents Z7 from being reset when Z2 changes state. The next clock pulse causes variable 1 frequency divider 1A14A4 to produce the preload signal (a high (5-volt) level) which is applied to the switch gates. The thumbwheel switch settings are gated into the registers. This is shown in figure 2-20 where it is assumed that the 1000 MHz, 100 MHz and 10 MHz thumbwheel switch sections are set at 45 and 6, respectively. The 1000 MHz and 100 MHz setting of 45 preloads decimal number 5 (binary 101) into stages Z9, Z8, and Z7. The 10 MHz setting of 6 preloads decimal number 6 (01111) into Johnson Counter stages Z6, Z6,

Z4, Z3, and Z2. With the 1000 MHz and 100 MHz switches in these positions, signal B is a high (5-volt) level and signal A is a low (0-volt) level (grounded through the switch section). With the 10 MHz switch set at 6, signal A is a low (0-volt) level (grounded through the switch section) and signals B, C, D, and E are at a high (6-volt) level. The preload signal sets the count into register stage Z9 through Z2; the registers assume the state 10101111. Assuming that the 1 MHz and 0.1 MHz thumbwheel switches are both set to 5, causing the registers in 1A14A4 to contain decimal 55, the count is jumped from time  $T$ , to time  $T$ . The clock pulses applied to the registers in 1A14A4 and the count pulses applied to the register in 1A14A5 -will now decrement the count until all registers are zero producing the divide-by-N pulses from output inverter Z13 in 1A14A5. The width of these pulses is determined by the conditioning of pin 10 of Z10 from Z211, thereby allowing it to be reset by the output reset signal from 1A14A4.

g. The divide-by-N -pulses are monitored at the output register Z10 to provide lamp bias. These pulses develop a positive voltage through diode CR1 keeping lamp driver Q1 conducting. With lamp driver Q1 conducting, the transistor in lamp assembly DS1 is held nonconducting. When the divided-by-N signal is not present, lamp driver Q1 becomes nonconducting and the transistor in DS1 conducts, lighting the failure indicator DS1 lamp red. Pressing the TEST pushbutton on the main chassis applies a 5 volt lamp test signal through terminal E23 and resistor R12 to the base of the transistor in DS1, causing the failure lamp DS1 to light red.

## 2-62. Fixed Frequency Divider 1A14A6 Circuit Functioning (fig. 5-53)

### NOTE

**Fixed frequency divider 1A14A6 contains integrated circuits designated Z1 through Z24. Integrated circuit types MC932, 946, 950, and 9002 are used. Circuit diagrams for each of these circuits are shown on figure --24.**

a. The 8 MHz sinusoidal signal from the standard rf oscillator (1A14A7) is applied through pins P1-8 and P1-6 and terminals E1

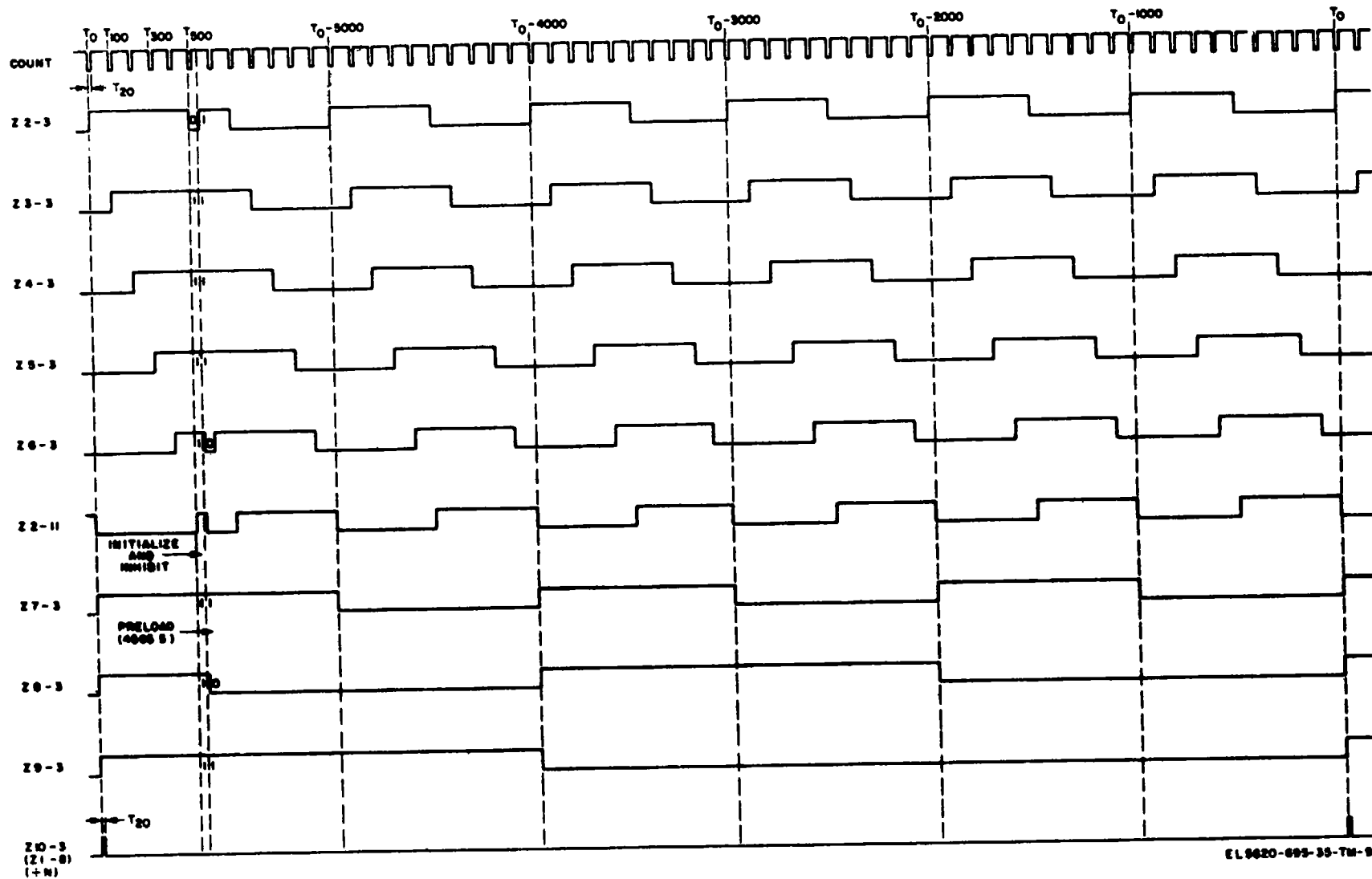


Figure 2-20. Variable 2 frequency divider 1A14A5, timing with jump count.  
2-105

and E2 to transformer T1 on board 1A14A6A2. Clamp diode CR2 across the secondary of transformer T1 clamps the signal which is then applied to divider Z1 through inverter Z15D. Divider stages Z1 through Z10 divide the incoming 8 MHz signal by 1024, each stage provides divide-by-two. The flip-flops, type 950, are set or reset from the previous circuit by a negative-going transition at pins 5 and 6; it is set when pin 4 is a low (0-volt) level and reset when pin 10 is a low (0-volt) level. The 7.8125 kHz output from Z10 is divided by five divider stages Z11 through Z13 (total divide 5120 by stages Z1 through Z13) to produce the 1.6625 kHz reference signal. Figure 2-1 shows the countdown in stages Z1 through Z15. A, figure 2-21 shows the timing for stages Z1 through Z5; B, figure 221 shows the timing for stages Z5 through Z10; and C, figure 1-33 shows the timing for stages Z10 through Z15. The pulse width of the 1.5625 kHz output of Z13 is changed to a 1 microsecond pulse width by output register Z14. The output frequency of Z14 is still 1.5625 kHz since only the pulse duration has been changed. The 1.6626 kHz signal is then routed through inverter Z24A to the af phase error detector 1A14A6A1 and to board 1A14A6A1.

b. The 1.6625 kHz reference signal is applied through pin P1-4 and terminal E20 to input gate Z16A and counter gate Z18A. The divide-by-N signal is applied through pin P1-7 and terminal E21 to input gate Z16B and counter gate Z18B. Both signals are shown in A, figure 2-22. Two timing conditions are shown in A, figure 2-22; both are phase-locked loop conditions. The waveforms on the left side of A, figure 122 show the leading edges of the 1.5625 kHz reference and divide-by-N (N) pulses occurring at the same time. The waveforms on the right side of A, figure 222 show a slight time lag between the 1.6255 kHz reference and the divide-by-N pulses, corresponding to a different rf output frequency from the rf oscillator (1A14A1). In either case; the repetition rate of the divide-by-N pulses is 1.5625 kHz. The two incoming signals (1.5625 kHz reference and divide-by-N pulses) alternately set and reset flip-flop Z17 with their pulse trailing edges. As shown in A, figure 2-22, the output of counter gates Z18A and Z18B are unchanged by the input signals. However when the divide-by-N signal is interrupted (or its frequency is not exactly 1.6625 kHz) as shown in B, figure 2-22, the next 1.5625 kHz reference pulse sets flip-flop Z17 which remains set; the next pulse develops an output from counter gate 2-106 I, Z18A which trigger

flip-flop Z19. Each succeeding pulse triggers flip-flop Z19 which then begins the counting in flip-flops Z20 through Z23 as shown in figure 2-23. The output from flip-flop Z22 becomes the 20 correction code that is applied to audio frequency phase error detector 1A14A3, the output from flip-flop Z23 becomes the 2 correction code. These signals will only change after a significant change in either input. When the 1.5625 kHz signal is interrupted, the output of audio frequency phase error detector 1A14A3, radio frequency oscillator 1A14A1, electronic frequency converter 1A14A2, and variable 1 and 2 frequency dividers 1A14A4 and 1A114A6 are all affected; the overall electrical frequency synthesizer 1A.14 operation for this case is considered nonoperating.

c. When the 1.662 kHz and divide by signals are phase locked, the input and output of flip-flop Z19 are unchanged and no signals are applied to inverter Z24B. In this state, alarm driver Q2 is nonconducting and the collector voltage is 8.6 volts dc (normal condition). This voltage is applied to alarm monitor 1A6 in the transmitter cabinet as the phase lock alarm through the main chassis. If the two signals are not in proper phase, flip-flop Z19 generates a square wave which biases alarm driver Q2, causing it to conduct and reduces the phase-lock alarm voltage to 0 volt (alarm condition). If the 1.5625 kHz signal is interrupted, flip-flop Z19 would not generate bias for alarm driver Q2 due to lack of signal; however, diode CR5 would bias alarm driver Q2 and change the phase lock alarm voltage to 0 volt (alarm condition).

d. The 1.5625 kHz output from flip-flop Z13 is monitored to produce a lamp bias for lamp driver Q1 through diode CR3. Lamp driver Q1 is normally conducting, and the transistor in lamp assembly DS1 is nonconducting causing the failure lamp DS1 to be extinguished. When the 1.5626 kHz signal is interrupted, lamp driver Q1 becomes nonconducting and drives the transistor in lamp assembly DS1 into conduction, lighting the failure lamp DS1 red. Pressing the TEST pushbutton on the main chassis applies a 5 volt lamp test signal through pin P1-9 terminal E12, and resistor R4 to the base of the transistor in lamp assembly DS1 to conduct and the failure lamp DS1 to light red.



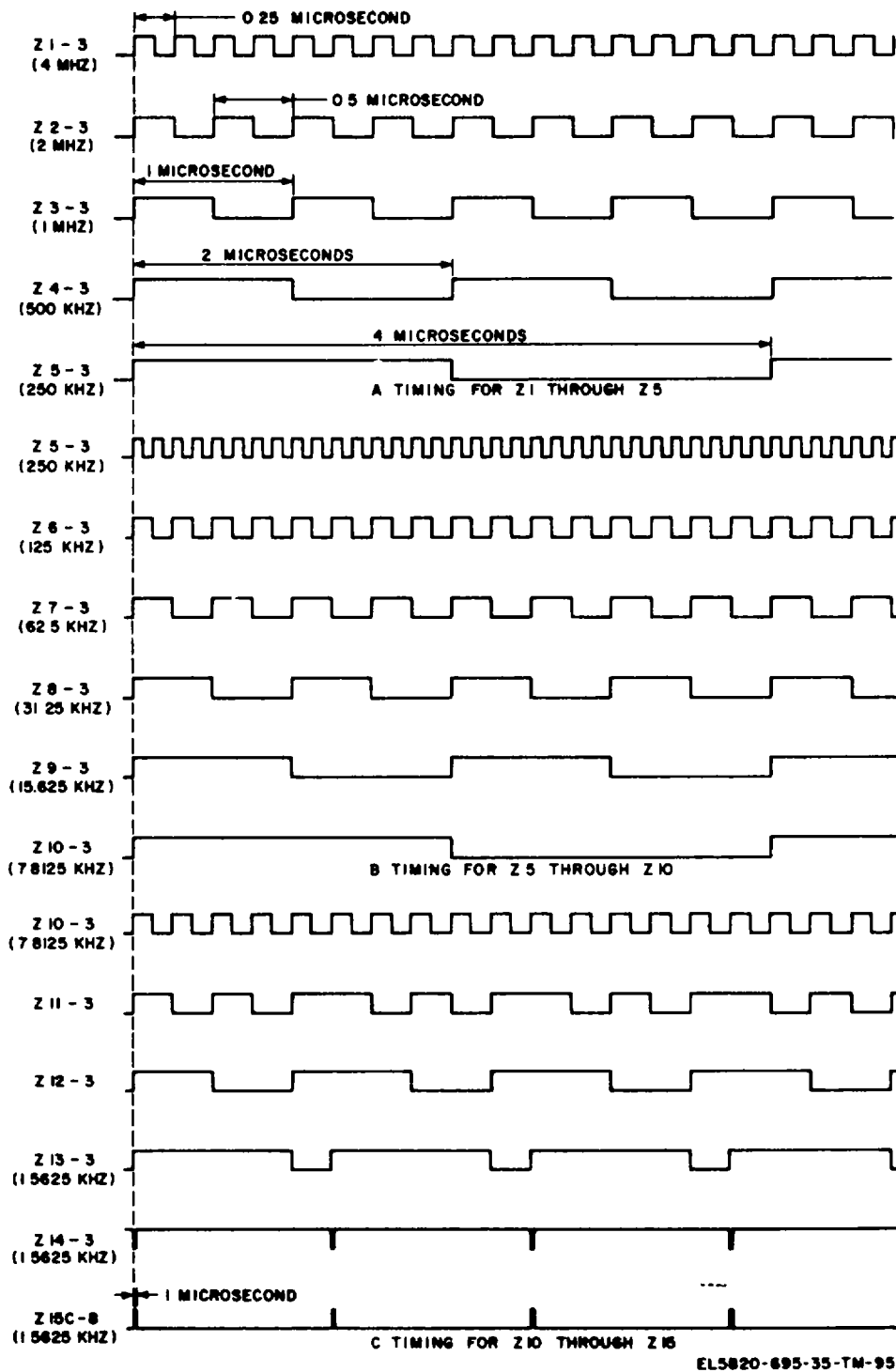


Figure 2-21. Fixed frequency divider 1A14A6, timing diagram.

**2-63. Standard Radio Frequency Oscillator 1A14A7 Functioning (fig. 5-45(1))**

The standard radio frequency oscillator 1A14A7 consists of a sealed module which contains a stable quartz crystal oscillator which is fully transistorized and uses integrated circuits and proportional oven control for maximum stability and reliability. The oscillator produces an 8.0 MHz sine-wave signal with an rf output

of 0.7vrms  $\pm$ 2db. It has a built-in oven with a temperature sensor which indicates when the oven is above 76°C. The temperature sensor contacts remain closed when the oven temperature is below 79° C. A frequency adjustment control is

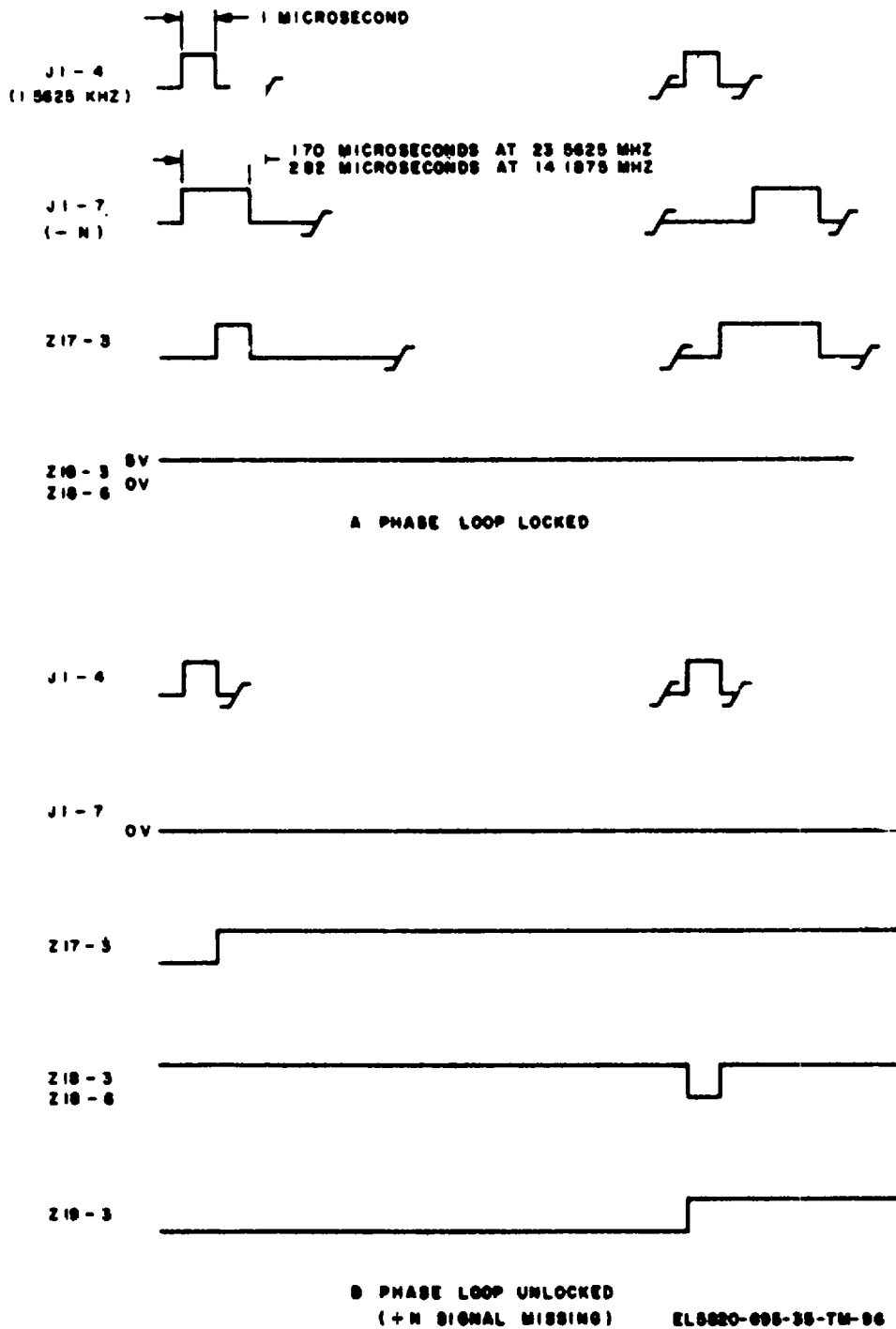


Figure 2-22. Fixed frequency divider 1A14A6 phase detector, timing diagram.

provided to compensate for aging and to allow the oscillator to be set within  $5 \times 10^8$ .

**2-64. Power Supply 1A14A8 Functioning (fig. 5-45(1))**

Power supply 1A14A8 consists of a sealed module which contains transistorized circuits that rectify 115

volts ac and produce two separate dc outputs: 28 volts and 5 volts. The input ac voltage may vary from 108.5 to 126.5 volts and from 50 to 400 Hz and the dc outputs will remain constant. The 28-volt output is rated for a full-load current of 450 milliamperes. The minimum full-load current for the 5-volt output is 760 milliamperes.

**2-64.1 Functioning of Relay Assembly 1A15A18**

Relay assembly 1A15A18 monitors summary alarm signals from Transmitter, Radio T-1054(P)A/GRC-144(V), Receiver, Radio R-1467 (P) A/GRC-144 (V) and Converter-Multiplier Assembly CV-3633/GRC-144 (V) . The summary alarm signals are applied to relays 1A15A18K1, K2 and K3 and output signals from these relays are routed to the OCU and to alarm monitor circuits in orderwire assembly 1A13. Relay 1A18K4 monitors status signals from the waveguide switches. Output signals from K4 are routed to WAVEGUIDE SW indicator at meter panel 1A15A8. The input connectors are shown in figure 2-29 for AN/GRC-144(V) 3 and in figures 2-30 and 2-31 for AN/GRC-144(V)4. These are simplified schematic diagrams; for the complete schematic diagram of relay assembly 1A15A18 see figure 5-15.1 (sheet 1).

a. Operating voltage (+28 Vdc from 1A15TB3-13) is applied to relays K1, K2 and K3 through 1A15A18E1. The status of the monitored signals at 1A15A18E2, E5 and E11 then determines whether a relay is energized or not. The sources of these signals are indicated in the figures. Refer to paragraph 2-87 for the signal at 3A7J2-C in figure 2-35. The chart below lists the three inputs and shows the corresponding status of each relay for normal and for fault condition. The relay output signal are routed to the OCU and to orderwire assembly k13. The chart shows output signal status for normal and fault conditions and signal routing. Chart data is applicable to both AN/GRC-144(V) 3 and AN/GRC-144(V)4, except for relay K1. In AN/GRC-144(V)3, there is no input at 1A15A18E2, K1 is always deenergized and the output signals at 1A15A18E3 is always open circuit.

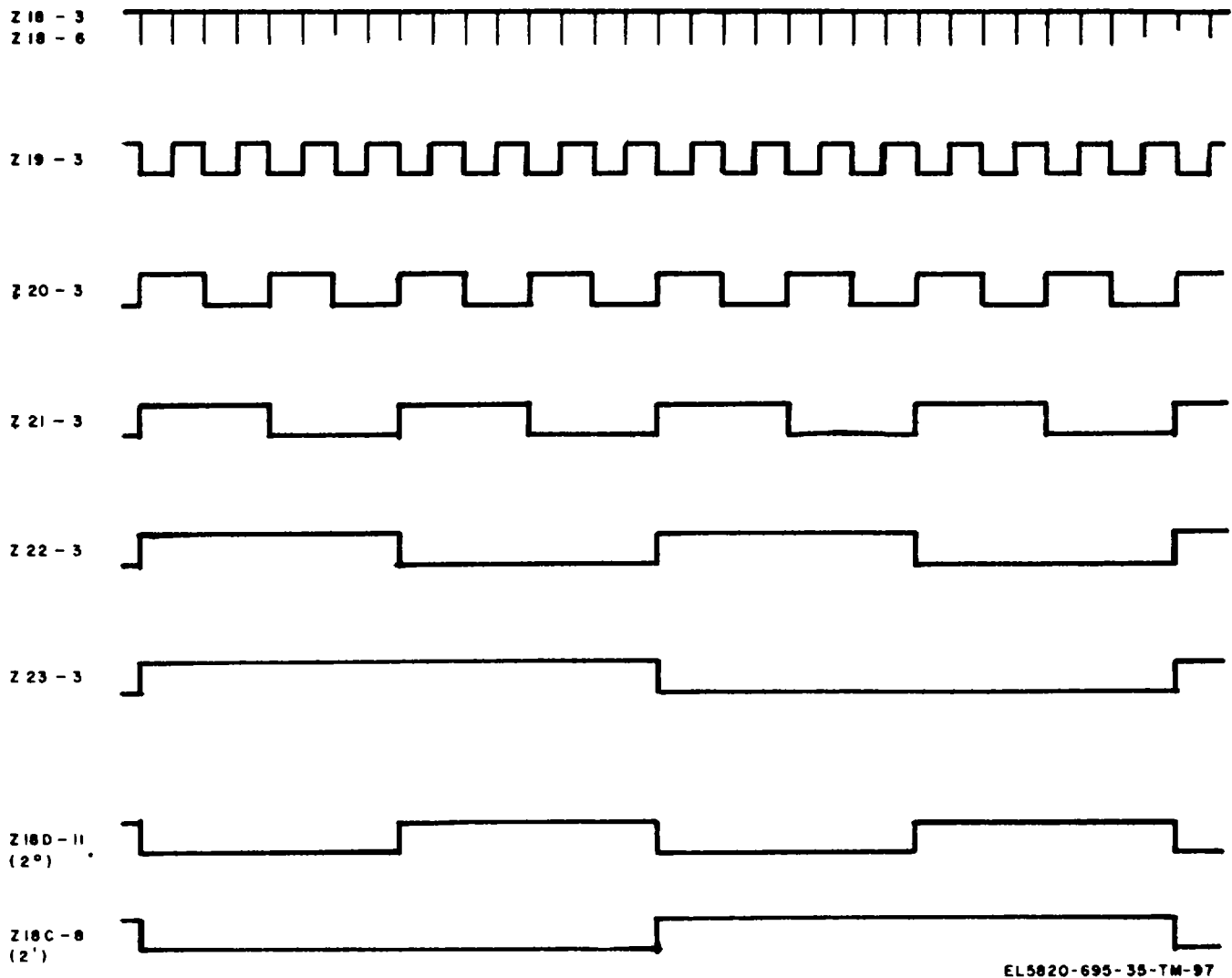
**Relay Assembly 1A15A18 Alarm Signal Data**

Inputs			Outputs			
Status			To OCU		To Orderwire Assembly 1A13	
Terminal	Signal	Relay	Terminal	Status	Terminal	Status
1A15A18E2 (conv)	Normal	K1 Not Energized	1A15A18E6/E7 via 1A15J22 -S and -T	Open Circuit	1A15A18E3 to 1A15XA13B-25	Open Circuit
	Fault	K1 Energized		Shorted		gnd
1A15A18E5 (xmtr)	Normal	K2 Not Energized	1A15A18E8/E9 via 1A15J22 -U and -V	Open Circuit	1A15A18E10 to 1A15XA13B-25	Open Circuit
	Fault	K2 Energized		Shorted		gnd
1A15A18E11 (rcvr)	Normal	K3 Not Energized	1A15A18E12/E13 via 1A15J22 -W and -X	Open Circuit	1A15A18E18 to 1A15XA13B-	Open Circuit
	Fault	K3 Energized		Shorted		gnd

b. Signals from the waveguide switches are applied to K4; these signals indicate the positions of the waveguide switches (para 2-80). Output signals from K4 are routed through 1A15A18E27 and E28 to WAVEGUIDE SW indicator (DS10 green and DS11 red) at meter panel 1A15A8. For AN/GRC-144(V)3 and the K-band only operating mode of AN/GRC-144(V)4, relay

K4 is energized for the antenna position and DS10 is off and DS11 is on. For the C-band/K-band operating mode of AN/GRC-144(V)4, when both waveguide switches are in the same band position, relay K4 is energized and DS10 is lighted and DS11 is off. If both switches are not in the same band position, relay K4 is not energized, DS10 is off and DS11 is on.

#### 2-108.2 Change 6



EL5820-695-35-TM-97

Figure 2-23. Fixed frequency divider 1A14A6 phase detector, timing diagram with phase loop unlocked.

### Section III. FUNCTIONING OF RECEIVER, RADIO R-1467(P)/GRC-144(V) and R-1467(P)A/GRC-144(V) CIRCUITS

#### 2-65. General

This section covers the functioning of circuits used in the R-1467(P)/GRC-144(V) and R-1467(P)A/GRC-144(V). The coverage is presented in sequential reference designation order and is at the schematic diagram level. Circuit functioning and schematic diagrams are not provided for nonrepairable assemblies such as tunnel diode amplifier 2A2 and preselector bandpass filter 2FL4. Circuit descriptions for cabinet mounted components (metering circuits, indicators, etc.) and the nonrepairable assemblies are covered in

the block diagram descriptions for the R-1467(P)/GRC-144(V) and R-1467(P)A/GRC-144(V) (para 2-19 through 2-26). Also, for circuits which are identical to those in Transmitter, Radio T-1054(P)/GRC-144(v) and T-1054(P)A/GRC-144(V) reference is made to circuit functioning coverage in section II. All cabinet mounted components circuits and all interconnections in the R-1467(P)/GRC-144(V) are shown in figure 5-21. (The R-1467(P)A/GRC-144(V) circuits are shown

in figure 5-21.1). All references to the R-1467(P)/GRC-144(V) also apply to the R-1467 (P) /GRC-144 (V) unless otherwise specified.

### 2-66. Power Supply 2A1 Circuit Functioning

Power supply 2A1 contains voltage regulators 2A1A1 through 2A1A4 which provide the dc supply and control voltages for the R-1467(P)/GRC-144(V). Power supply chassis assembly 2A1A5 provides the following: (1) a connector for each voltage regulator, (2) an ac fuse at the input of each voltage regulator, and (3) a failure lamp and a test point at the output of each voltage regulator. The interconnecting diagram for power supply 2A1 is shown in figure 6-22.

### 2-67. Low Pass Filter 2A3 and 2A17 Circuit Theory (fig. 2-24 and 2-24.1, 2-24.2, and 2-24.3)

The low pass filter is connected in the pcm orderwire signal path, between demodulator 2A4 and af-rf amplifier A11 and contributes to the overall required shaping the pacm signal pulses. In the synchronous mode, 1.0 MHz low pass filter 2A3 is used. In the asynchronous mode, 3.8 MHz low pass filter 2A17 is used. Both filters consist of a five-pole low pass filter tuned to approximate Gaussian shaping. The 1.0 MHz filter has a nominal 3 dB bandwidth of 1 MHz, and at 1.4, 2, and 2.8 MHz it provides 6, 12, and 20 dB of attenuation, respectively. The 3.8 MHz filter has a nominal 3 dB bandwidth of 3.8 MHz and it provides attenuation of 1.5 dB at 2.687 MHz, 6 dB at 5.374 MHz, 12 dB at 7.676 MHz and 20 dB at 10.526 MHz. The source impedance for both filters is 50 ohms and the load impedance is 150 ohms. The filtering components consist of variable inductors L1 and L2 and capacitors C1 through C6 (C1 through C3 for the 3.8 MHz filter). Resistor R1 provides the input impedance matching. For Receiver, Radio R-1467 (P)A-GRC-144 (V), 5.3 MHz low pass filter assembly 956419 (fig. 2-24.2) is used for 9 MB/s data rate and 13 MHz low pass filter

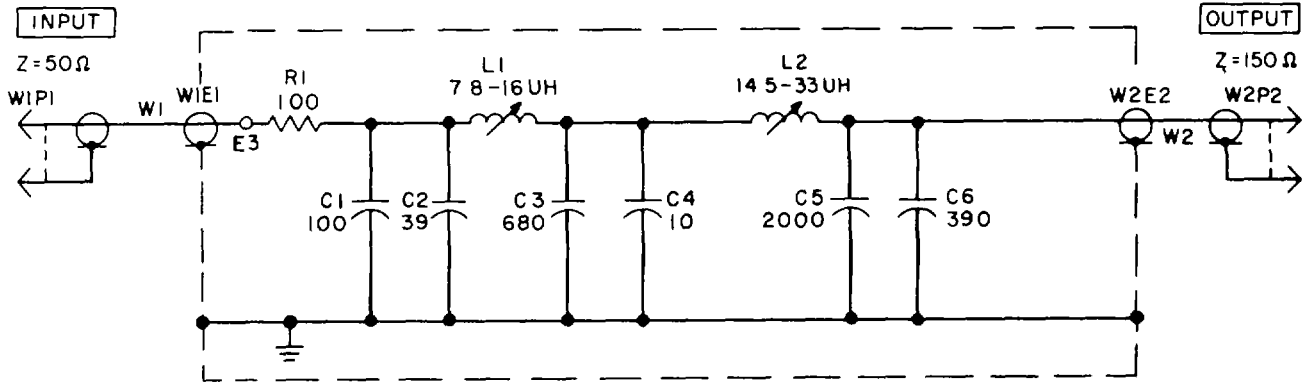
assembly 956421 (fig. 2-42.3) is used for 18 MB/s data rate.

### 2-68. Demodulator 2A4 Circuit Functioning (fig. 5-54)

Demodulator 2A4 converts the 70 MHz if signal to the baseband signal (composite pcm and orderwire signal). The demodulator consists of input amplifier Q1 limiter stages Q2 through Q5 a two stage discriminator driver Q6 and Q7, a frequency discriminator, and video output amplifier Q8 and Q9.

*a. Input Amplifier.* The 70 MHz if input from 2A5 is applied to J1 IF input connector and through coupling capacitor C1 to input amplifier Q1. This stage matches the input impedance to the impedance of first limiter stage Q2. Q1 is biased by resistors R2, R4 and R6, while R5 is the input load resistor. C3 and C5 are bypass capacitors. The output is taken off at the Q1 emitter and fed through coupling capacitor C8 to first limiter stage Q2. A diode detector CR1 connected to the input of Q1 through coupling capacitor C2, monitors the if input. The detector circuit consists of CR1 and R1. When the signal goes negative, diode CR1 conducts grounding the signal; diode CR1 is nonconducting during positive half cycles. This produces a rectified signal which is filtered by RC circuit R3 and C4. The resultant dc is available at J2 (front panel test point TP2 INPUT LEVEL.)

*b. Limiter Stages.* The purpose of limiter stages Q2 through Q5 is to prevent amplitude variations (amplitude modulation) from appearing at the frequency discriminator input. The limiter stages operate in the common base configuration. Since the four limiter stages are identical, except for minor variations in biasing and tuning, only first limiter stage Q2 is described in detail. The input is applied to the junction of resistors R10 and R11. R10 and R11, together with voltage divider R7 and R8 establish the transistor bias. The bias is bypassed by capacitors C7 and C11, which serve as a ground return for

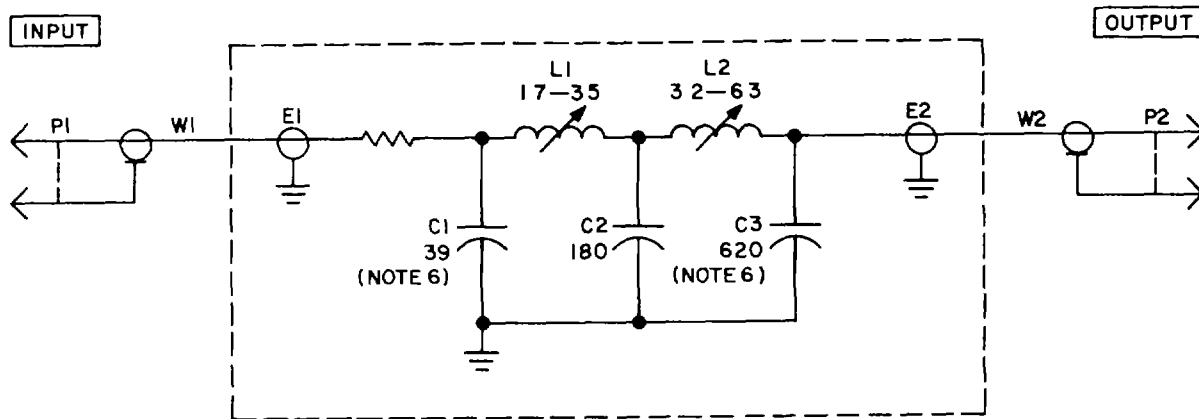


NOTES

EL5820-695-35-TM-79

- 1 UNLESS OTHERWISE SPECIFIED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN PICOFARADS, ALL INDUCTANCES ARE IN MICROHENRIES
- 2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, PREFIX ALL REFERENCE DESIGNATIONS WITH 2A3
3.  INDICATES MARKING ON EQUIPMENT.

Figure 2-24. 1.0 MHz low pass filter 2A3, schematic diagram.

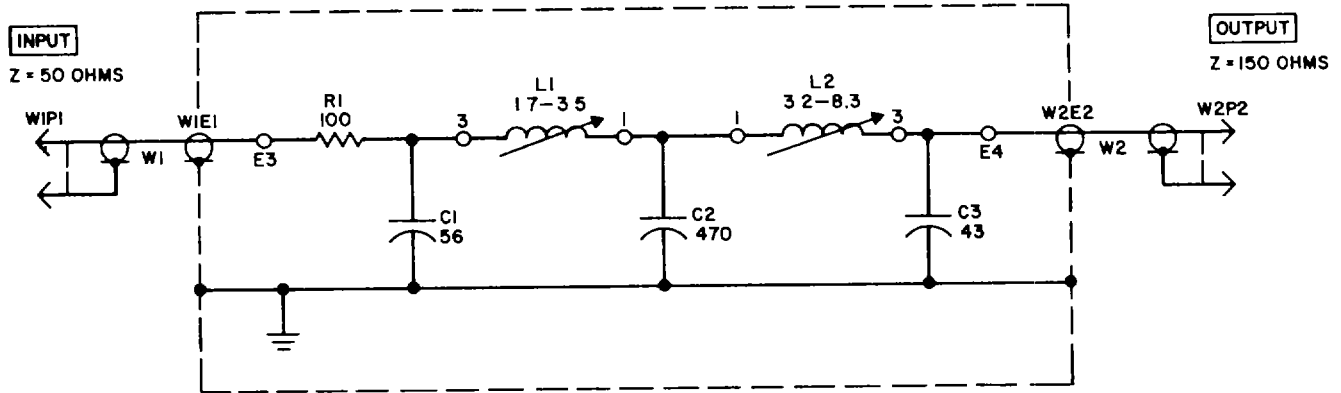


NOTES

EL218007

- 1 AT P1 SOURCE IMPEDANCE: 50 OHMS RESISTIVE.
- 2 AT P2 LOAD IMPEDANCE: 150 OHMS RESISTIVE
- 3 UNLESS OTHERWISE SPECIFIED  
CAPACITANCE VALUES ARE IN PICOFARADS  
RESISTANCE VALUES ARE IN OHMS  
INDUCTANCE VALUES ARE IN MICROHENRIES
- 4 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.
- 5  INDICATES MARKING ON EQUIPMENT
- 6 ON CONTRACT DA A B05-72-C-5507, C1 IS 30 AND C3 IS 560

Figure 2-24.1. 3.8 MHz low pass filter 2A3, schematic diagram.

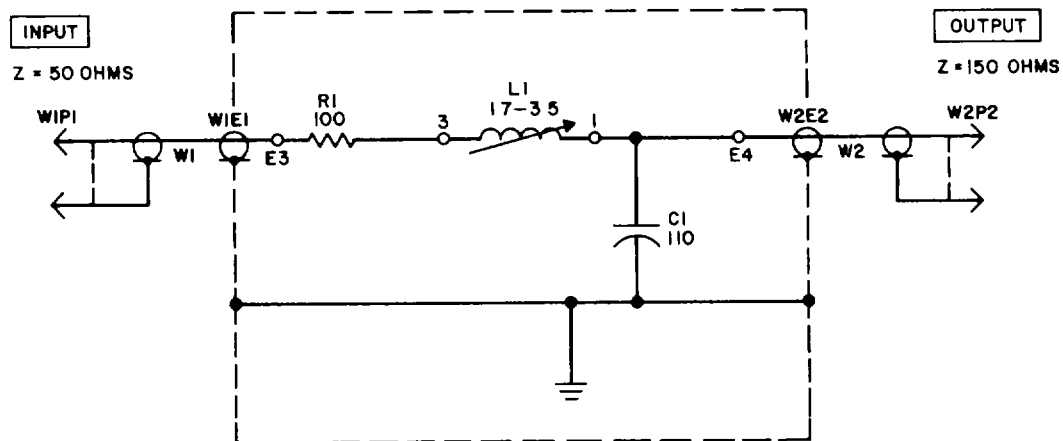


NOTES

- 1 AT P1 SOURCE IMPEDANCE, 50 OHMS RESISTIVE
- 2 AT P2 LOAD IMPEDANCE, 150 OHMS RESISTIVE
- 3 UNLESS OTHERWISE SPECIFIED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN PICOFRADS, ALL INDUCTANCES ARE IN MICROHENRIES
- 4 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, PREFIX ALL REFERENCE DESIGNATIONS WITH 2A3.
- 5  INDICATES MARKING ON EQUIPMENT

EL2IB028

Figure 2-24.2. 5.3 MHz low pass filter 2A3, schematic diagram.



NOTES

- 1 AT P1 SOURCE IMPEDANCE, 50 OHMS RESISTIVE
- 2 AT P2 LOAD IMPEDANCE, 150 OHMS RESISTIVE
- 3 UNLESS OTHERWISE SPECIFIED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN PICOFRADS, ALL INDUCTANCES ARE IN MICROHENRIES
- 4 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; PREFIX ALL REFERENCE DESIGNATIONS WITH 2A3.
- 5  INDICATES MARKING ON EQUIPMENT

EL2IB029

Figure 2-24.3. 13 MHz low pass filter 2A3, schematic diagram.



the rf signal. Variable inductor LI tunes the collector circuit of Q2 and resistor R9, connected across L5, loads the collector circuit thereby providing stability. The stage output is tapped from inductor L5. The limiting action is obtained by operating Q2 near saturation. The base is biased at +13.5 volts dc. A resistance of 1015 ohms (R11 plus R10) in the emitter circuit results in highly stable operation near the saturation region. Under these conditions, the collector to emitter voltage of Q2 is in the order of 1.0 volt. A negative signal swing tends to further increase the current of Q2 but, because of the near saturation, the swing at the collector is limited. With a positive signal swing, the emitter voltage tends to become more positive, thereby reducing the base emitter voltage. This, in turn, causes the emitter voltage to decrease, due to the reduced emitter current through resistors R10 and R11. Because of these counteracting effects the output voltage swing due to positive signal excursions is also limited. The second, third, and fourth limiter stages operate in an identical manner. The output of fourth limiter stage Q5 is tapped from variable inductor L14 and applied to the first stage of discriminator driver Q6 through capacitor C33. The output of Q6 is also fed to a metering circuit consisting of diode detector CR2, resistor R30, and associated RC circuit R27 and C81. The metering circuit produces a dc signal proportional to the limiter output level. The resultant dc level is made available for monitoring at Jo (front panel test point TP3 LIM. LEVEL).

*c. Discriminator Driver.* The discriminator driver consists of two transistor stages Q6 and Q7. The first stage Q6, is an emitter follower. The signal enters at the base, and the output is taken off at the junction of resistors R81 and R32. Biasing is provided by voltage divider R28, R29, and emitter resistors R31 and R32. Capacitors C35 and C37 are bypass capacitors. The input to second stage Q7 is through coupling capacitor C38 to the junction of resistors R36 and R37. This stage is configured common base, and, unlike the limiter stages, is biased in the linear region. Base bias voltage of +6.76 volts is derived from voltage divider R83 and R84 and emitter bias from resistors R36 and R37. The base is bypassed by C39 and the emitter by capacitor C44.

*d. Frequency Discriminator.* The frequency discriminator recovers the video signal (composite pcm and orderwire) from the modulated 70 MHz if signal. It operates on the phase shift principle, and consists of transformer T1, diodes CRS and CR4, and associated parts.

(1) Both the primary and secondary of transformer T1 are tuned to the 70 MHz. center frequency. Tuning is accomplished by variable capacitors C43 and C45, respectively. The signal from Q7 is connected across the primary winding of transformer T1, and also to the center tap of the secondary winding of T1 through capacitor C41. With a 70 MHz signal applied, the voltages across each half of the secondary windings are in quadrature with the voltage across the primary. They are of equal amplitude and are 180 degrees out of phase. When the signal is above resonance, the phase angle between one half of the secondary and the primary is greater than 90 degrees, and that for the other half of the secondary is less than 90 degrees. Below resonance, these phase relationships are reversed, the phase angle for the first half of the secondary being less than 90 degrees, and that for the second, greater than 90 degrees.

(2) The signals at the cathodes of diodes CR3 and CR4 are the vector sums of the primary and associated secondary voltages. At resonance these signals are of equal amplitude; while off resonance, the signal associated with the half secondary having the greater phase difference is the larger. The difference between the two voltages is proportional to the frequency excursion from the resonant frequency. The modulation (video) is recovered by the rectifying action of diodes CR3 and CR4. Since the voltages across these diodes are in opposition, the current through load resistors R40 and R41 is produced by the difference between the impressed voltages. The signal developed across the load resistors has, as its fundamental frequency, the recovered video. Ripple at the if frequency is bypassed by capacitor C46.

(3) Two positive coefficient thermistors, R85 and R41, are used in the discriminator to compensate for thermal effects in discriminator driver Q7 and Q8. The thermistors have a temperature coefficient of approximately +0.7 percent degree centigrade. The resistance of R85 in the collector circuit of Q7 increases with increasing ambient temperature. This action compensates for the thermal effects in Q7. Similarly, resistor R41 increases the output signal at capacitor C48, with increasing ambient temperature, compensating for thermal effects in diodes CRS and CR4, and the video output amplifier, Q8 and Q9.

(4) A metering circuit is provided at the output of frequency discriminator, consisting of R42, C47, and J4. When the mean if frequency at the input of the frequency discriminator differs

from the resonant frequency of transformer T1, a dc component is present in the output of the frequency of transformer T1, a dc component is present in the output of the frequency discriminator at the junction of R40 and R41. The dc level/ depends on the frequency offset, and the polarity on whether the if frequency is above or below the resonant frequency of transformer T1. This dc component is extracted by RC low pass filter R42 and C47, and can be monitored at J4 (TP4 DISCR), thus determining whether the frequency discriminator is properly tuned, or conversely, whether the if frequency is properly centered.

*e. Video Output Amplifier.* The frequency discriminator output is applied through capacitor C48 to the base of Q8, which together with Q9 comprises the video output amplifier. This circuit provides isolation between the frequency discriminator and 1.0 MHz low pass filter 2A3. Resistors R43 and R44 set the base bias for Q8, while R45 limits the collector current of video output amplifier Q8 and Q9. Capacitor C51 bypasses the collectors of video output amplifier Q8 and Q9. The output is developed across resistor RH5 and applied to the 1.0 MHz low pass filter 2A3 through capacitor C52, resistors R47 and R48 and connector J6 VIDEO OUTPUT.

### **2.68.1 Receiver, Radio R-1467(P)/GRC-144 (V) Demodulator 2A4 Circuit Functioning (fig. 5-54.1)**

Demodulator 2A4 converts the 70 MHz IF signal (from 2A5) to the baseband (composite data/orderwire) signal.

*a.* The amplifier-low pass filter stage Q1-Q2 includes an input matching section (R1, R2, R3, L1) required to meet a 26 dB return loss limit. Buffer amplifiers Q1 and Q2 provide isolation between the input section and the low pass filter. Variable inductors L4 and L5 in the low pass filter are adjusted for frequency response flatness. The cutoff frequency of the filter is 90 MHz and it rejects harmonics of the 70 MHz IF signal. A rectifier-filter network monitors the input signal and supplies a test point voltage at J2 (TP2 INPUT LEVEL) .

*b.* Limiter input matching circuitry, consisting of inductor L6, resistor R20 and common emitter amplifier Q3, provides impedance matching between the low pass filter and the limiter stages. Test point E8 serves as a matched impedance point for alignment checking. Transistors Q3, Q4 and Q5 are common emitter limiter-amplifiers. Diodes CR2 through CR7 serve as low impedance shunt limiters. Emitter follower stage Q6 provides low impedance (75 ohms) coupling into the low pass filter L11, L12 and L13. These variable inductors are adjusted for amplitude flatness and group delay characteristics. A 3 dB resistive pad (R44 through R46) is used to improve the 75-ohm impedance match.

*c.* Discriminator driver amplifiers Q7 and Q8 use emitter by-passing to produce a flat amplitude response (+0.2 dB) and a differential group delay of less than 1 nanosecond over the 60 to 80 MHz frequency range. Capacitor C42 in the emitter circuit of Q7 is adjusted for flat response in the 63 to 77 MHz range. Capacitor C49 in the emitter circuit of Q8 is adjusted for 13 dB minimum gain. The discriminator is a standard Crosby type. Tank circuit L19/C51 is tuned to 93 MHz and L20/C52 is tuned to 47 MHz. Capacitors C53 and C54 are charged with opposite polarities through discriminator/rectifier diodes CR8 and CR9. The charging time constants are short and the voltages across C53 and C54 track frequency variations. The algebraic sum of these voltages is developed across R66, R67 and R68. R67 is adjusted for average (center frequency) level and the signal is fed through low pass filter L21/L22 are adjusted for flat response (+1 dB) below 30 MHz. The low pass filter rejects harmonics of the video signal. Common emitter video amplifier stages Q9 and Q10 use inverse feedback and provide a gain of 25 dB. Emitter follower stage Q11 provides low impedance coupling of the video signal to low pass filter 2A3.

### **2.69 70 MHz Intermediate Frequency Amplifier 2A5 Circuit Functioning (figs. 5-55 and 5-55.1)**

The 70 MHz intermediate frequency amplifier 2A5 amplifies the low level 70 MHz signal to a sufficient level to drive the demodulator circuits.

The gain of 2A5 is controlled by an internal age circuit.

*a. IF Amplifier.* The incoming 70 MHz if signal is applied from connector P1, IF INPUT, to the base of transistor Q1 through R GAIN potentiometer R2 and capacitor C2. Cascaded if amplifiers Q1 through Q5 amplify the incoming if signal under the control of an age level. The age level is applied to diodes CR1 through CR4 which are connected in the interstage networks of the cascaded if amplifiers. These diodes present a minimum ac impedance at high dc currents and low dc, currents the diodes present maximum ac impedance. This provides automatic gain control under the influence of the amplified agc voltage level established at the emitter of emitter follower Q10. A high level of age voltage at the emitter of emitter follower Q10 will cause a high dc current flow through the diodes CR1 through CR4 producing minimum attenuation of the incoming if signal. The rf signal is detected by diodes CR5 and CR6 and the resulting detected dc voltage is amplified by dc amplifiers Q8 and Q9 which controls the agc voltage applied to emitter follower Q10. Each cascaded if amplifier is forward biased by a resistive divider network in the base circuits; the cascaded if amplifiers are tuned by variable capacitors C4, C8, C12, C16, and C21 in the emitter circuits. Additional degenerative feedback is provided by unbypassed resistor R57 in the emitter circuit of the input transistor Q1. The amplified if signal is coupled through buffer Q6 to the base of output amplifier Q7 through capacitor C24. The if output signal is taken from a center tap on autotransformer T1 to provide an output impedance of 75 ohms.

*b. AGC Circuits.* Full wave detection of the amplified if signal is provided by peak detector diodes CR5 and CR6 in conjunction with capacitors C28 and C31. The detected agc level is developed across series resistors R32 and R37. AGC SEL switch S1 allows selection of the source of age applied to the base of dc amplifier stage Q8. When AGC SEL switch is in the DIV OFF position, the detected agc level is applied to the base of Q8 through contact 3 of section SIA. Placing the AGC SEL switch in the TEST position disables the age function and places the if gain A1 a constant maximum value by grounding the base of Q8 through contact 1 of section SIA. The DIV ON position is not used because the R1467/GRC-144 is a single channed

receiver. Dc amplifiers Q8 and Q9 are connected as a differential amplifier and the age level is coupled from the wiper of AGC GAIN potentiometer R40 to the base of emitter follower Q10. The operation of Q10 was described in paragraph 2-69a.

*c. Metering Circuits.* The metering circuits provide agc signal level outputs to the meter selector switch on meter panel assembly 2A15A2, to alarm monitor 2A12, and to Indicator, Antenna Alignment ID-1708/GRC. The age output derived from peak detector diodes CR5 and CR6 is applied to the carrier if meter circuit on 2A15A2 through the voltage divider consisting of R32 and R37 and pin P3-10. The age output of emitter follower Q10 is applied to the agc meter circuit on 2A15A2 through R43 and P3-9, and to the ID-1708/GRC through R52 and P3-11. The references for age metering and antenna alignment indicator outputs are applied through the meter adjust circuit of R46, R47, and R48. METER ZERO control R47 is used to set the meter on 2A15A2 to electrical zero. The age output of emitter follower Q10 is also applied to the carrier if monitor circuit in alarm monitor 2A12 through R55 and R56 and P3-12. The reference for the carrier if monitor signal is applied through the carrier level alarm adjust circuit, R49, R50, CR8 and CR9. The alarm adjust circuit produces a 1.5 to 7 vdc reference for the alarm circuit in 2A12.

## **2-70. 70 MHz Bandpass Filter 2A6 Circuit Functioning (figs. 2-25, 2-25.1 and 2-25.2)**

The 70 MHz bandpass filter 2A6 is used in the signal path between amplifier-mixer 2A7 and 70 MHz if amplifier 2A5 to reduce if noise components, to reject undesired signals and to aid in shaping of the pcm pulses. The 70 MHz bandpass filter 2A6 is a five pole bandpass filter with a center frequency of 70 MHz, a bandwidth of 5.0 MHz is tuned to approximately Gaussian shaping. The source and load impedances of the filter are 75 ohms, respectively. The maximum insertion loss at 70 MHz is 2.5 dB. The frequency response of 2A6 (reference 0 dB at 70 MHz) is as follows:

Frequency (MHz)	Attenuation (db)
68.20 and 71.81.....	1.2 to 1.6
67.64 and 72.54.....	2.6 to 3.4
66.58 and 73.59.....	6.4 to 6.6
65.15 and 75.19.....	10.8 to 13.2
63.52 and 77.10.....	17.0 to 23.0

For Receiver, Radio R-1467(P)/A/GRC-144(V), 10.6 MHz bandpass filter assembly 956417 (fig. 2-25.1) is used for 9 Mb/s data rate and equalizer-filter assembly 956462 (fig. 2-25.2) is used for 18 Mb/s data rate.

**2-71 Amplifier-Mixer 2A7 Circuit Functioning (figs. 2-26 and 2-26.1)**

Amplifier-mixer 2A7 converts the 4.4-5.0 GHz rf input signal to the 70 MHz if signal. This conversion is made by mixing the 4.4-5.0 GHz rf input signal with the 4.33 to 5.07 GHz local oscillator signal. The B+ supply (15 vdc) is provided by decoupling capacitors C5, C10, C14, and C20. Inductors L5, L8, and L10 block the if signal from the B+ input. Test point TP2, + 15v, can be connected to the meter on meter panel assembly 2A15A2 with a test lead and resistor R21 is a meter decoupling resistor.

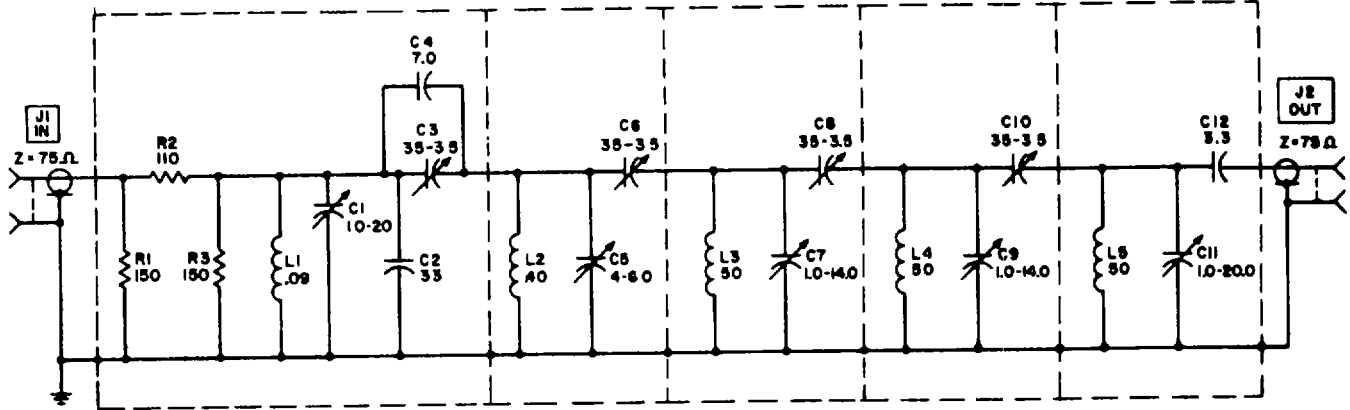
a. *Crystal Mixer 2A7Z1.* The 4.4 to 5.0 GHz rf input signal is applied to input of 2A7Z1 through connector J1 RF IN and the 4.33 to 5.07 GHz local oscillator signal is applied to input jack J2 LO IN. Crystal mixer 2A7Z1 consists of a matched pair of IN23 WEMR crystal diodes CR1 and CR2 which mix the rf input signal with the local oscillator signal. Mixing the two signals produces numerous frequencies, of which, the four predominant frequencies are: (1) the original carrier frequency, (2) the original local oscillator frequency, (3) the sum of the two frequencies, and (4) the difference between the two frequencies (70 MHz). Only the 70 MHz difference frequency is applied to the input circuit of first preamplifier Q1, through coupling capacitors C2, C3, and C7. All other frequencies produced by the mixing process are rf bypassed to ground in crystal mixer 2A7Z1. Additional outputs are provided which permit monitoring the dc current through

crystal diodes CR1 and CR2. A positive dc voltage is developed across resistor R1 which is proportional to the dc current through crystal diode CR1. This positive dc voltage is sent to the meter selector switch through pin 8 of plug P1. Similarly, a negative dc voltage is developed across resistor R2 which is proportional to the dc current through crystal diode CR2. This negative dc voltage is also sent to the meter selector switch via pin 9 of plug P1. Inductors L1 and L2 are used to block the if signal from the diode monitoring circuits, and capacitors C1 and C4 provide filtering. A filter in each circuit (C6, L4, C9, and C8, L6, C13) provides additional filtering of the if signal. Resistors R3, R23, and R4, R22 and meter decoupling resistors. Resistors R22 and R23 are variable and are used to adjust meter deflection.

b. *First Preamplifier.* The input circuit for first preamplifier stage Q1 is a parallel resonant circuit. Therefore, the resonant frequency and bandwidth of the parallel resonant circuit determines the band of frequencies coupled to the base of first preamplifier stage Q1. The parallel resonant circuit is formed by L3, C7, the input capacitance of Q1, and the output if capacitance of crystal mixer 2A7Z1. The resonant frequency is set at 70 MHz by adjusting IF ADJ control L3. Q1 amplifies the 70 MHz if signal passes by the input circuit, and the amplified 70 MHz if signal is coupled by C11 to the base of second preamplifier stage Q2 through capacitor C11. Resistors R5 and R6 provide fixed dc basis for Q2, and resistor R7 is its collector load. Emitter resistor R8 provides negative dc feedback to temperature stabilize first preamplifier stage Q1, and capacitor C12 provides the if bypass and tuning.

c. *Second Preamplifier.* Second preamplifier stage Q2 also amplifies the 70 MHz if signal, and the output is coupled by C15 to the base of third preamplifier Q3. Resistors R9 and R10 provide fixed dc bias for this stage and inductor L7 is its collector load. Resistor R11 provides negative ac feedback to stabilize second preamplifier

**5-POLE GAUSSIAN FILTER**  
 $f_0 = 70 \text{ MHz}$   
**3DB BANDWIDTH=5MHZ**



**NOTES**

1. UNLESS OTHERWISE SPECIFIED  
 CAPACITANCES ARE IN PICOFARADS  
 INDUCTANCES ARE IN MICROMHENRIES  
 RESISTANCES ARE IN OHMS
2. PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN, FOR COMPLETE  
 DESIGNATION, PREFIX WITH 2A6.
3.   INDICATES MARKING ON EQUIPMENT

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Figure 2-25. 70 MHz band pass filter (B=5.0 MHz) 2A6 (684447), schematic diagram.

stage Q2, and capacitor C16 is the if signal bypass for RT1 and potentiometer R12. Thermistor RT1 also provides temperature compensation for the gain of this stage over a wide temperature range. Potentiometer R12 sets the operating current through second preamplifier stage Q2, and, therefore, sets the gain of second preamplifier stage Q2.

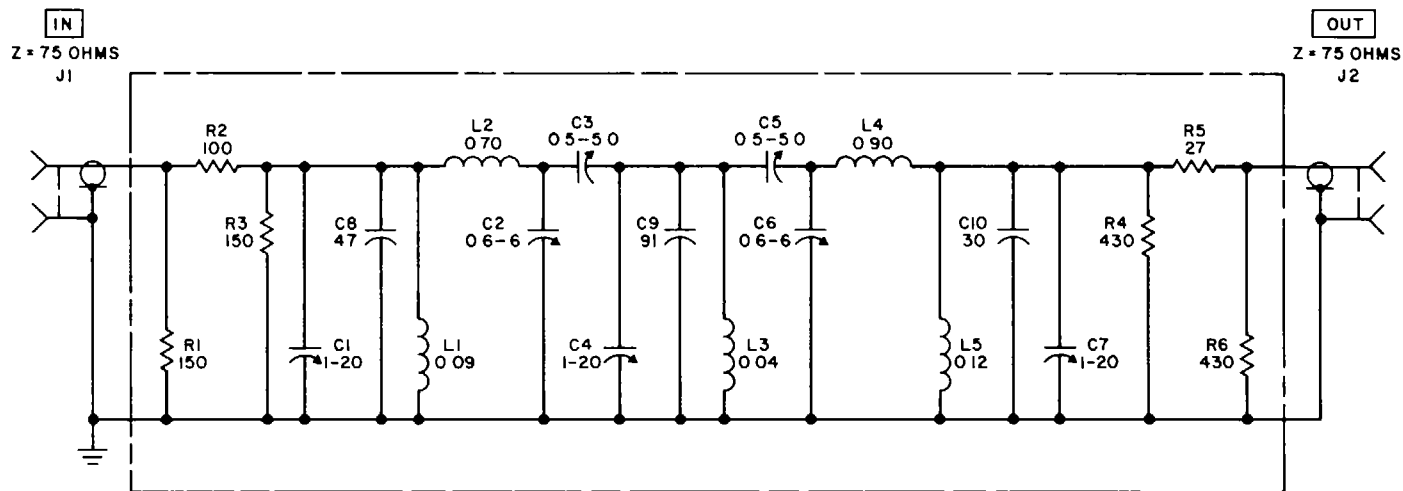
d. *Third Preamplifier.* Third preamplifier Q3 also amplifies the 70 MHz if signal. Its output is coupled by C17 to 70 MHz bandpass filter 2A6 through output plug P2 designated IF OUT. Resistors R17, R19, R20, and capacitor C22, form an impedance matching network to provide a 75 ohm output impedance. Capacitor C22 is variable in this network to permit matching the load. Resistors R13 and R14 provide fixed dc bias for third preamplifier stage Q3, and inductor L9 is its collector load. Emitter resistor R15 provides negative ac feedback to stabilize this stage, and capacitor C19 is the ac bypass. Resistors R15 and R16 determine the current through third preamplifier stage Q3. The 70 MHz if signal out of third preamplifier stage Q3 is also coupled by C18 to a diode detector circuit formed by CR3, R18, and C21. This provides a positive dc voltage which is proportional to the level of the detected if signal at jack J4 designated TP1 IF MON. Test point TP1 IF MON can be connected to the meter on meter panel assembly 2A15A2 with a test lead.

**2-72. Receiver Frequency Mixer Stage 2A8 Circuit Functioning (fig. S:6)**

Receiver frequency mixer stage 2A8 produces the 4.33 to 5.07 GHz local oscillator signal by mixing the 220 MHz signal from the 220 MHz frequency multiplier-osc 2A13 with the 4.55 to 4.85 GHz signal from bandpass filter 2FL21. Receiver frequency mixer stage 2A8 consists of 220 MHz bandpass filter FL1, crystal mixer Z1, a crystal current metering circuit, and coaxial circulator HY1.

a. *220 MHz Bandpass Filter 2A8FL1.* 220 MHz bandpass filter 2A8FL1 is a three-pole Chebyshev type bandpass filter. Maximum insertion loss is 8 db; bandwidth is 11.5 MHz at the 3 db reference points. The input is filtered by 2A8FL1 for application to crystal mixer 2A8Z1.

b. *Crystal Mixer 2A8Z1.* Crystal mixer 2A8Z1 is similar to a conventional balanced coaxial mixer but uses two forward diodes CR1 and CR2. The unit accepts a 220 MHz input signal at a level of +11 dbm to +13 dbm and an input signal in the frequency range 4550 to 4850 MHz at a level of + 16 dbm to +22 dbm. The resultant rf output



NOTES

- 1 UNLESS OTHERWISE SPECIFIED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN PICOFRADS, ALL INDUCTANCES ARE IN MICROHENRIES
  - 2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN,
  - 3 PREFIX ALL REFERENCE DESIGNATIONS WITH 2A6
- ▭ INDICATES MARKING ON EQUIPMENT

EL2IB030

Figure 2-25.1. 70 MHz band pass filter (B=10.6 MHz) 2A6, (956417) schematic diagram.

Change 6 2-114.1

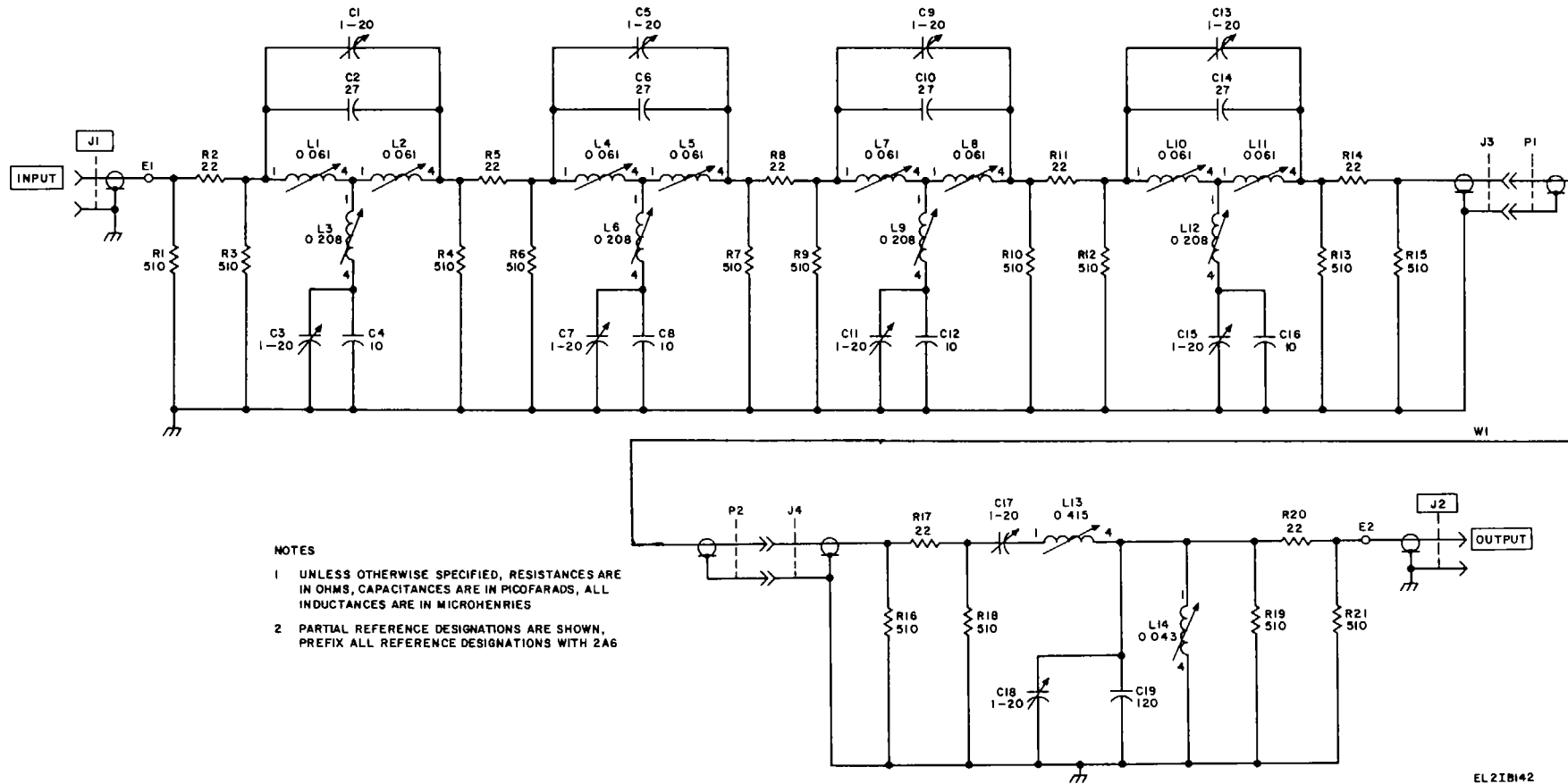


Figure 2-25.2. Equalizer filter 2A6, (956462), schematic diagram.

2-114.2 Change 6

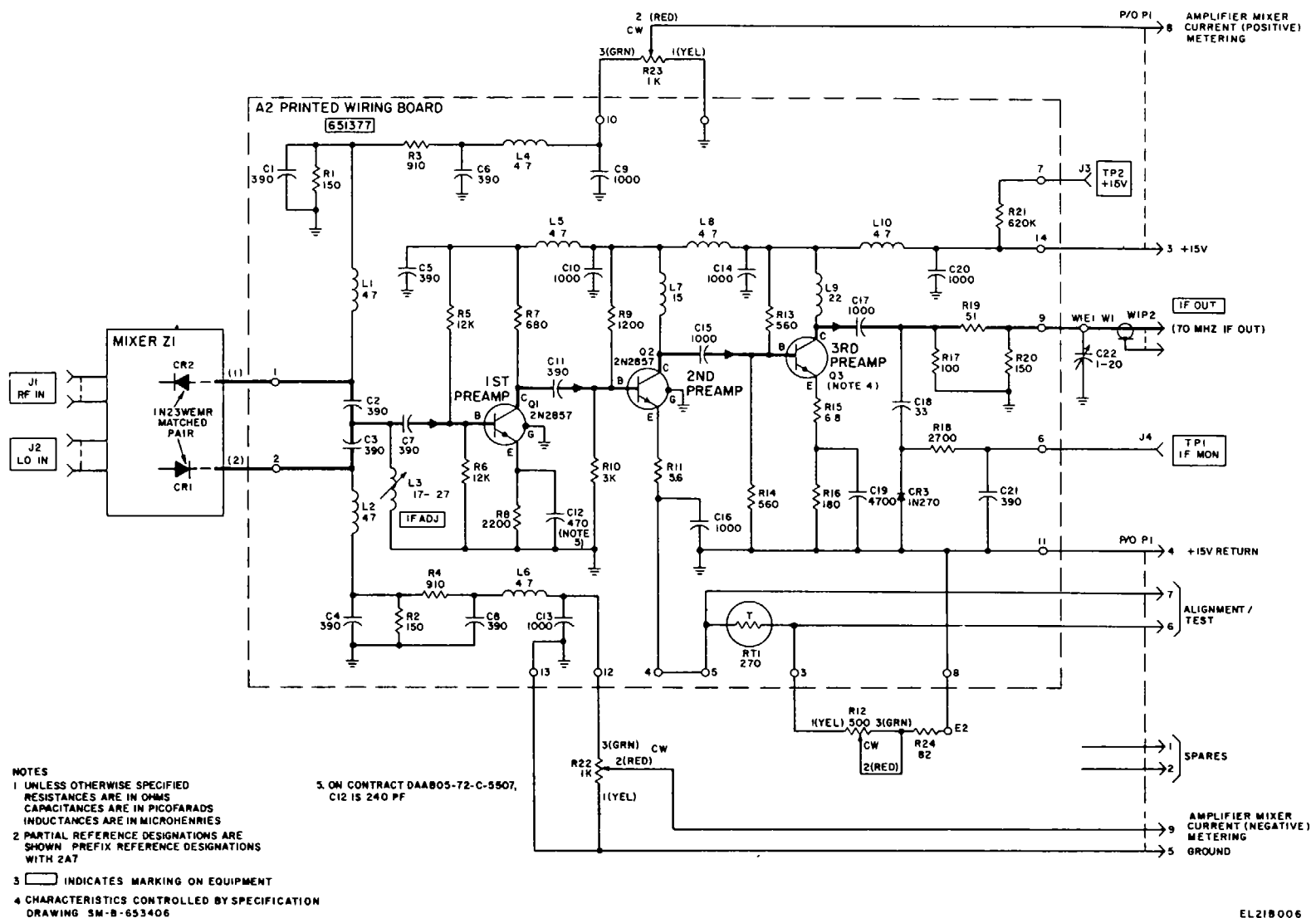


Figure 2-26. Amplifier-Mixer 2A7, (650520) schematic diagram.



frequency is in the range of 4.33 to 5.07 GHz; conversion loss does not exceed 12db relative to the 220 MHz signal input level thereby producing an output level of above 0 dbm nominal at connector J2 RF OUTPUT.

*c. Crystal Current Metering Circuit.* The crystal current metering circuit consists of L1, C1, R1, R2, C3, L2 and FL2 in one mixer diode metering branch and L3, C5, R3, R4, C6, L4 and FL3 in the other mixer diode branch. Capacitors C2 and C4 provide coupling of the 220 MHz signal into crystal mixer 2A8Z1.

*d Crystal Circulator 2A8HY1.* Coaxial circulator 2A8HY1 has a bandpass of 4.33 to 5.07 GHz with a maximum insertion loss of 0.8 db. The 2A8HY1 provides 18db isolation from port J2 output to port J1 input. A resistive termination is incorporated at port 3 to dissipate the rejected sideband from local oscillator bandpass filter 2FL6.

### **2-73. Amplifier-Frequency Multiplier 2A10 Circuit Functioning (fig. 5-7)**

Amplifier-frequency multiplier 2A10 amplifies and multiplies (times 16) the 284.375 to 303.125 MHz (20 milliwatts, nominal) input signal to a 4.55 to 4.85 GHz (70 milliwatts, nominal) output signal. Amplifier-frequency multiplier 2A10 is comprised of a 300 to 600 MHz frequency doubler, a 600 MHz amplifier, and a 600 to 4800 MHz frequency octupler.

*a. 300 to 600 MHz Frequent Doubler.* The 284.375 to 303.125 MHz signal from electrical frequency synthesizer 2A14 is applied to the primary of transformer T1 through connector designated J1 INPUT. The secondary of T1 is connected to the anodes of diodes CR1 and CR2. This circuit is, in effect, a full-wave rectifier, in which CR1 and CR2 alternately pass a half cycle of the input signal. The fundamental output (568.750 to 606.250 MHz) is twice the input frequency and is coupled to the base of Q1 in the 600 MHz amplifier circuit through variable capacitor C1.

*b. 600 MHz Amplifier.* The 600 MHz amplifier consists of transistor stages Q1 and Q2 which operates as low level class A amplifiers in the common emitter configuration. Transistor stage Q3 is a power amplifier and operates class C. Capacitors C3, C4, C10 and C11 are emitter bypass capacitors and adjustable resistor R7 in the emitter circuit of Q2 permits adjusting the gain. The output of Q2 is coupled to the base of Q3 through capacitors C13 and C14. The output of

Q4 is applied to the 600 to 3800 MHz octupler stage via cable W1. Matching is accomplished by C17, L12, C18, and C19.

#### *c. 600 to 4800 MHz Frequency Octupler.*

This stage multiplies (times 8) the amplified 568.750 to 606.250 MHz signal up to 4.55 to 4.85 GHz. The frequency multiplying (times 8) action is achieved by varactor diode CR3. The input circuit consists of capacitors C20, C21, C23, C28, and inductor plates L13 and L14. Resistor R13 provides bias for varactor diode CR3. The input circuit is tuned to the 568.750 to 606.250 MHz input signal. The output circuit (C22, C29, L15) is tuned to the eighth harmonic of the input frequency. The 4.55 to 4.85 GHz. output signal (70 milliwatts, nominal) is fed through circulator HY1 to the HY1J2 OUTPUT connector. Circulator HY1 provides isolation between the 600 to 4800 MHz frequency octupler circuit in 2A10 and the receiver frequency mixer stage 2A8.

### **2-74. AF-RF Amplifier 2A11 Circuit Functioning (fig. 2-13)**

Af-rf amplifier 2A11 is a wide band video amplifier and is identical to af-rf amplifier 1A4 used in the T-1054/GRC-144. The circuit theory description provided in paragraph 2-31 for af-rf amplifier 1A4 also covers af-rf amplifier 2A11 with the following exceptions: (1) The composite pcm and orderwire signal from 1.0 MHz low pass filter 2A3 is applied to J1 IN and is amplified; (2) the orderwire input (P1-8) is not used; (3) the amplified output (composite pcm and orderwire signal) is applied to digital data (modem 1A12 via J2 OUT; and (4) the alarm output (P1-9) is used (the amplified pcm and orderwire signal is routed to alarm monitor 2A12 via P1-9).

### **2-75. Alarm-Monitor 2A12 Circuit Functioning (fig. 2-14)**

*a.* Alarm monitor 2A12 is identical to alarm monitor 1A5 used in the T-1054/GRC-144; however, the jumper connections on the associated plate assembly connectors for each assembly are different. The circuit functions of alarm monitor 1A5 are described in paragraph 2-32. The following paragraphs describe the circuit functions of alarm monitor 2A12.

*b.* The low level traffic monitor input signal is amplified by integrated circuit operational amplifier AR1 (fig. 2-14, part 3). The inverting

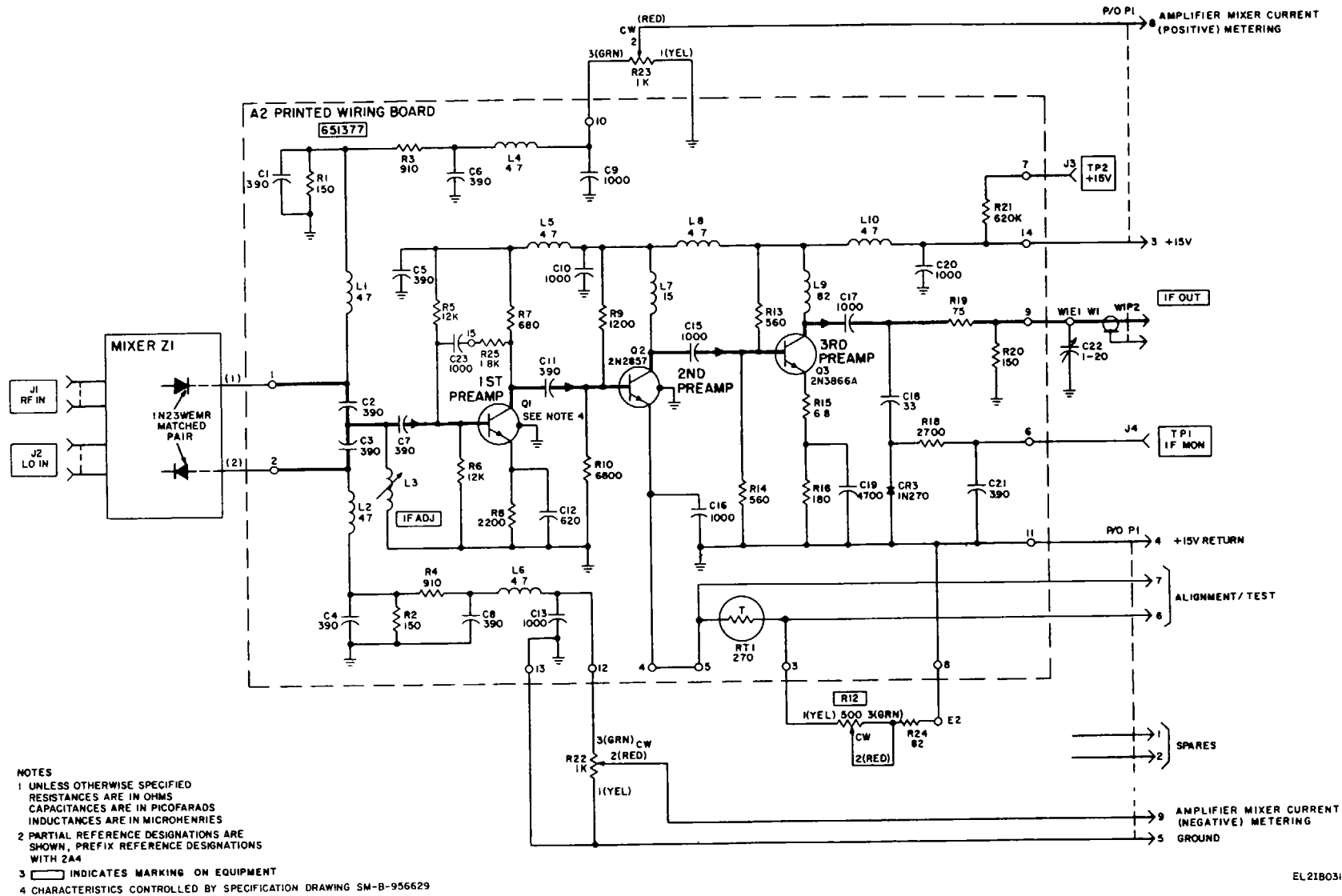


Figure 2-26.1 Amplifier-Mixer 2A7, (956425) schematic diagram.

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input of operational amplifier AR1 is pin 2 and the noninverting input is pin 5. The output signal is taken from pin 7 with a feedback resistance connected from the output pin 7 to the inverting input pin 2 to establish the gain of the amplifier AR1.

c. The traffic monitor signal is coupled in pin 13 through attenuator R1-R3 to the inverting input pin 2 of amplifier AR1. The network consisting of C1 and R4 connected across the differential inputs (pin 2 and 3) provides lag compensation which increases the high frequency response. The amplified traffic signal is applied through the peak detector circuit consisting of capacitor C4, diodes CR1 and CR2 and capacitor C5 to the meter selector switch on 2A15A2 through variable resistor R8 and also to the base of emitter follower stage Q1. The positive peak-detected dc voltage is applied to Q1 which couples the signal through attenuator network, R10, R11, and R12, to its associated Schmitt trigger circuit on board AS. The Schmitt trigger circuit for the traffic signal consists of transistors Q5 and Q6 (fig. 2-14(2)). When no signal is present, transistor Q6 conducts and holds transistor Q5 off due to the voltage developed across common emitter resistor R48. The incoming peak-detected traffic signal will forward bias transistor Q5 when the magnitude of the peak-detected traffic signal exceeds the magnitude of the voltage developed across common emitter resistor R48. When this occurs transistor Q5 conducts and transistor Q6 cuts off until the peak-detected signal again drops below the voltage level of the common emitter resistor R48. The output of the Schmitt trigger circuit is a positive voltage which is developed at the collector of transistor Q6. This voltage is applied to the base of transistor Q7 to forward bias it into conduction. When transistor Q7 is conducting its collector is at a low level; this provides a low impedance path to ground to light the normal (green) TRAF indicator lamp on meter panel assembly 2A15A2. The inverted output level at the collector of transistor Q6 is applied to the alarm (red) TRAF indicator lamp on 2A15A2. Transistor (Q7) provides a low impedance path to ground for the alarm lamp when no traffic signal is detected (quiescent state of the Schmitt trigger circuit).

d. A synthesizer monitor signal, developed in electrical frequency synthesizer 2A14, is applied to Schmitt trigger circuit Q14 and Q15 through pin P2-17 (fig. 2-14(2)). This signal indicates when the electrical frequency synthesizer 2A14 is not phase locked and is in a search mode attempting to correct the oscillator frequency. When electrical frequency synthesizer 2A14 is phase locked, a +2 volt level is applied to input pin 17 to forward bias transistor Q14. This in turn, cuts off

transistor Q15 and turns on transistor Q16 providing the normal (green) indication. When electrical frequency synthesizer 2A14 is not phase locked, the input signal drops to zero volts which turns on transistor Q15 producing the alarm (red) indication.

e. The carrier (if) monitor signal is applied to the base of transistor Q4 and the carrier (if) monitor reference signal (a predetermined level) is applied to the base of Q3. Transistors Q3 and Q4 on board A5 (fig. 2-14(1)) form a differential amplifier. As the 70 MHz if carrier input to 2A5 increases, the age signal decreases, consequently, the carrier (if) monitor input to Q4 decreases. With the input to Q4 lower than the input to Q3, Q3 will conduct more heavily and Q4 turns off. With Q4 turned off, its output dc voltage is high. The high output of Q4 is applied through potentiometer R35 on board A1 (fig. 214(3)) to Schmitt trigger (Q17, Q18) on board A5 (fig. 2-14(3)). Potentiometer R35 is used to set the input level to Q17. The high output from Q4 causes Q17 to turn on, which in turn, causes Q18 to turn off and Q19 to turn on. With Q19 turned on, its collector is at a low level which provides a low impedance path to ground to light the normal (green) if carrier indicator lamp on 2A15A2. The inverted output level at the collector of Q18 is applied to the alarm (red) carrier (if) indicator on 2A15A2 which provides a low impedance path to ground for the alarm indicator when the carrier (if) monitor input (derived from the age signal) is at a higher level than the predetermined carrier (if) monitor reference signal.

f. A three input diode OR-gate and inverting transistor provides the summary alarm function. This circuit consists of diodes CR12, CR15, and CR16, transistor Q23 and resistors R102 and R103 (fig. 2-14(2)). When the anode of any input diode has a positive voltage level applied to it, it conducts and forward biases transistor Q23 into conduction producing a summary alarm condition. When all of the diodes have a low (or zero) voltage applied to their anodes, they are nonconducting and transistor Q23 is turned off producing a normal indication.

g. Zener diodes C5 and CR6 are incorporated on board A1 to provide regulated plus and minus voltages for the integrated circuits. Zener diode CR5 (fig. 214(8)), in conjunction with resistor

R31, provides a regulated plus 10 volts while zener diode CR6 (fig. 2-14(3)) in conjunction with resistor R33 provides a regulated minus 8.2 volts.

## **2-76. 220 MHz Frequency Multiplier-OSC 2A13 Circuit Functioning (fig. 5-58 and 2-27)**

The 220 MHz frequency multiplier-osc (fig. 5-58) generates a 220 MHz (70 milliwatts, nominal) output signal which is applied to receiver frequency mixer stage 2A8. The 220 MHz frequency multiplier-osc consists of 110 MHz rf oscillator 2A13Y1 and amplifier-frequency multiplier 2A13A1.

### *a. 110 MHz RF Oscillator 2A13Y1 (fig. 2-27).*

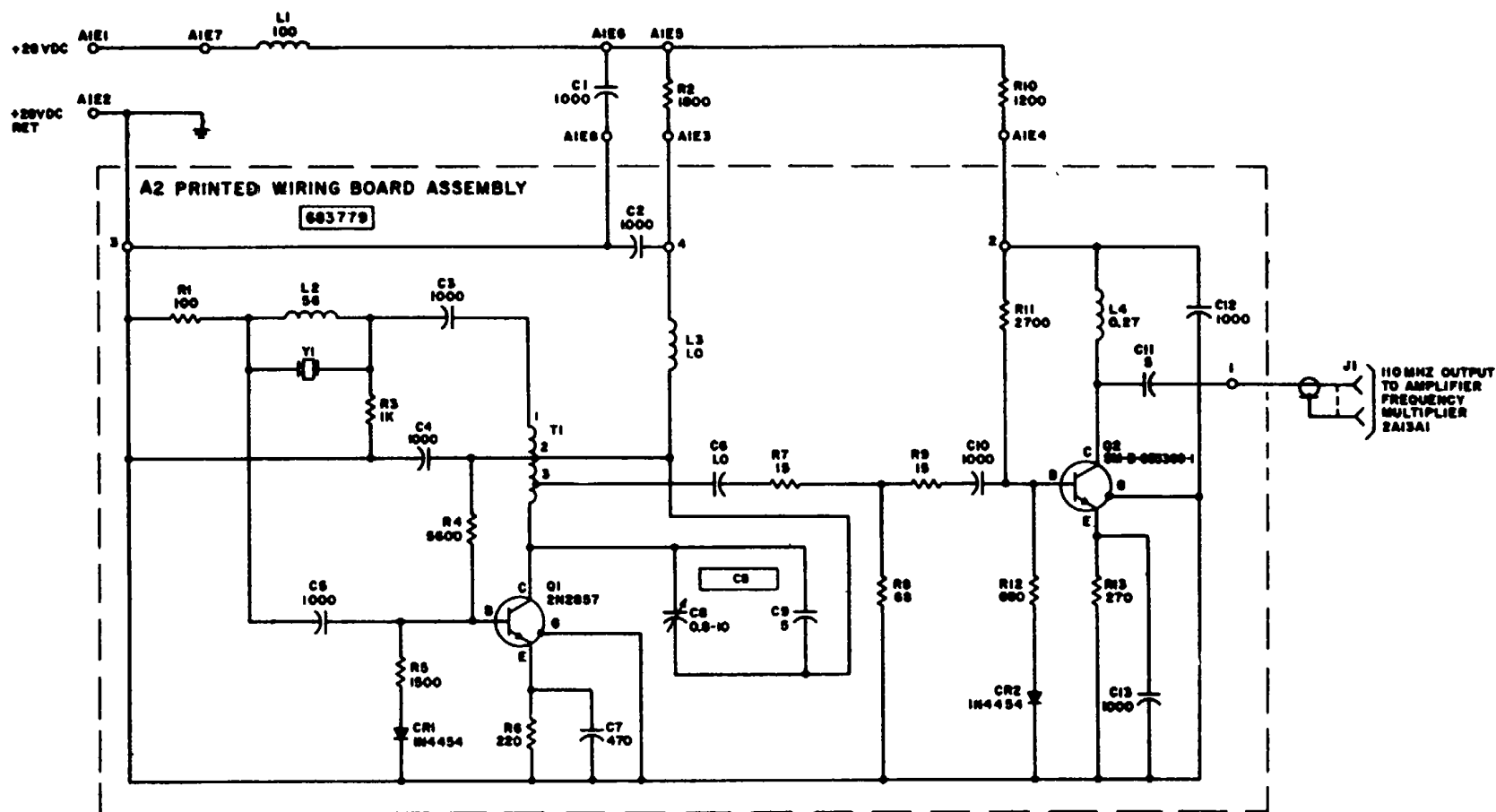
The 110 MHz rf oscillator is a crystal oscillator which produces a 110 MHz (Z 1600 Hz) output signal at a nominal power level of 16 milliwatts (across 50 ohms). The 110 MHz output is applied to amplifier-frequency multiplier 2A13A1 through connector 2A13Y1J1 and coaxial cable A1W1. The oscillator consists of transistor Q1, 110 MHz crystal Y1, coupling capacitors C5 and C6, bias resistors R4, R5, and R6, and a tank circuit comprised of transformer T1 and capacitors C8 and C9. Variable capacitor C8 provides a means of tuning the crystal oscillator to the correct stable output power level. When the +28 vdc supply voltage is applied, the initial surge will cause oscillations to start. The crystal signal is amplified by Q1 and fed back to the crystal to sustain oscillations. The 110 MHz output is taken at terminal 3 of T1 and coupled through capacitors C6 and C10 to amplifier stage C2. Resistors R7, R8, and R9 provide attenuation and impedance matching between the 110 MHz oscillator stage and amplifier stage Q2. CR1 and CR2 are temperature compensating diodes in the base circuits of Q1 and Q2. The amplified 110 MHz signal appears at the collector of Q2 and is coupled to output connector J1.

*b. Amplifier-Frequency Multiplier 2A13A1 (fig. 5-58).* Amplifier-frequency multiplier 2A13A1 doubles the frequency of the incoming 110 MHz oscillator signal and

amplifies the doubled frequency (220 MHz) to a level of 70 milliwatts (across 60 ohms). The 110 MHz oscillator signal is applied through cable A1W1 to the base of input amplifier stage Q1 through attenuator pad R1, R2 and RS and base biasing network C8, R4 and R5. The amplified 110 MHz signal is capacitance coupled by C4 to the primary winding (pins 1 and 2) of transformer T1. Frequency doubler stage Q2 and Q3 is connected to the secondary windings and conduct on alternate half cycles of the incoming 110 MHz signal thus, the common collector signal will be twice the frequency as the input signal. Inductor LB, in parallel with the output capacitance of the frequency doubler stage, resonates at 220 MHz and variable capacitor C9 tunes LS to 220 MHz and also controls the drive to the base of output amplifier stage Q4. Zener diode CR1 in conjunction with resistor R11 provides a regulated 16 volts for application to the collectors of Q2 and QS of the frequency doubler stage and to the base biasing network, CR2, R12, R18, and R14 of output amplifier stage Q4. This stage amplifies the incoming 220 MHz signal and the output is taken from the tuned resonant circuit consisting of autotransformer L4 and capacitor C14. The output signal is coupled to the receiver frequency mixer stage 2A8 through a pad consisting of R16, R17, R18, R19 and R21. The output is adjusted by variable capacitor C14 to provide 70 milliwatts drive across a 50 ohm load at connector P2. A sample of the output is detected by diode CRS and is applied to the meter selector switch on 2A15A2 through resistor R21 and rf filter FL1. Test points designated TP1 + 28V and TP2 CR1 are used for monitoring the +28 vdc and regulated 15 volts.

## **2-77. Electrical Frequency Synthesizer 2A14 Circuit Functioning**

Electrical frequency synthesizer 2A14 is identical to electrical frequency synthesizer 1A14 used in Transmitter, Radio T-1054/GRC-144 (para 2-56 through 2-64).



NOTES

1. UNLESS OTHERWISE SPECIFIED. RESISTANCES ARE IN OHMS. CAPACITANCES ARE IN PICOFARADS. INDUCTANCES ARE IN MICROMHENS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; PREFIX REFERENCE DESIGNATIONS WITH ZA13Y1.
3.    INDICATES MARKING ON EQUIPMENT.

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Figure 2-27 .110 MHz rf oscillator 2A13Y1, schematic diagram.

Section IV. FUNCTIONING OF INDICATOR, ANTENNA ALIGNMENT ID-1708/GRC CIRCUITS

2-78. General

Indicator, Antenna Alignment ID-1708/GRC is used to measure the relative signal strength of the 70 MHz if carrier signal in Receiver, Radio R-1467/GRC-144. The agc level, derived from the 70 MHz If carrier signal, is applied to the ID-1708/GRC to provide a relative signal strength indication and facilitate antenna alignment.

from 70 MHz intermediate frequency am plifier 2A5 in the R1467/GRC-144 is applied to meter M1 through connector P1, cable W1, and switch 91 (ON position). Capacitor C1 averages out the fluctuations of the incoming agc signal to provide a peak reading on the meter. In the OFF(TRANSIT) position, switch S1 provides a short across the meter. Terminals E1 and E2 are provided for connecting a telephone handset to permit communication over the link and also with shelter personnel. Terminals E1 and E2 are connected to the remote phone circuit through P1-F and P1-G.

2-79. Indicator, Antenna Alignment ID-1708/GRC Circuit Functioning (fig. 2-28)

The agc signal level and the agc meter reference level

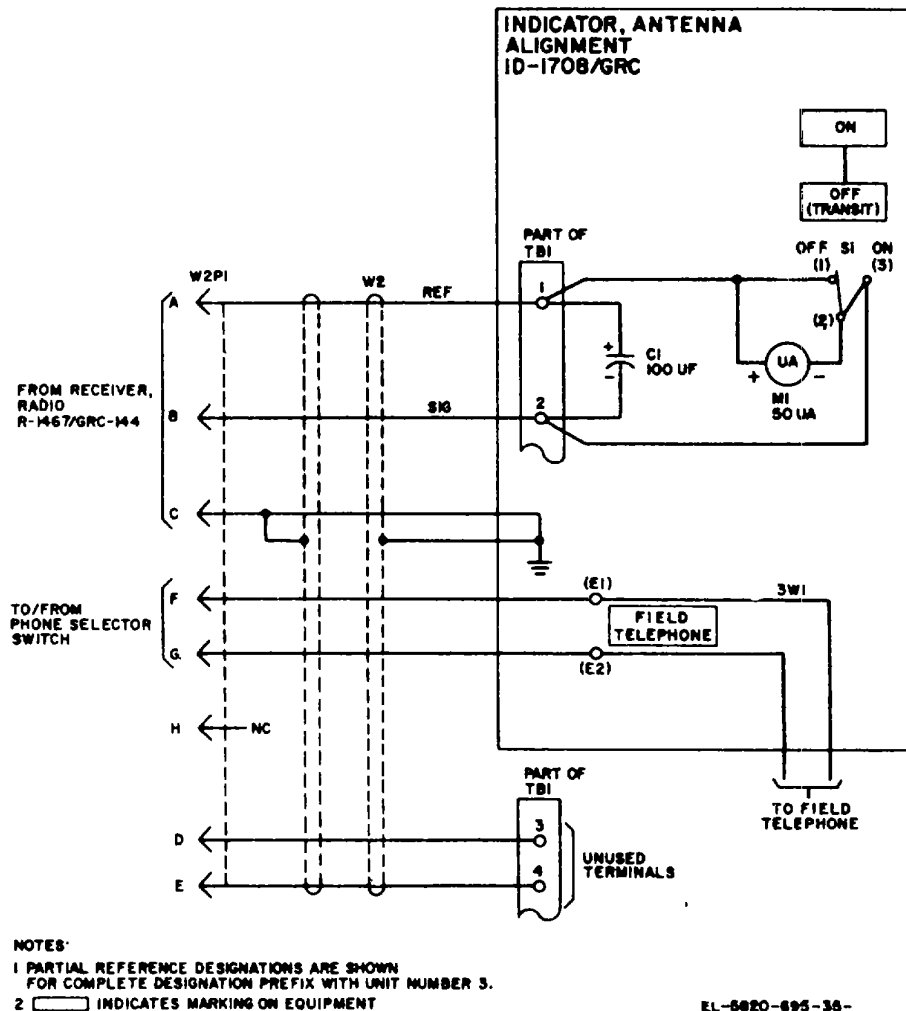


Figure 2-28. Indicator, Antenna Alignment ID-1708/GRC, schematic diagram.

## Section V. FUNCTIONING OF WAVEGUIDE SWITCH POSITION INDICATOR CIRCUITS

### 2-80. AN/GRC-144(V)3 and AN/GRC-144(V)4 Waveguide Switch Position Indications

The waveguide switches that route the RF energy between the radio set and the antenna have auxiliary dc switches that are used to provide signals for remote indication of the RF switch position. There are three configurations to be considered; they are explained in a through c below.

#### a. AN/GRC-144(V)3, Hi-Cap LOS Configuration

In this configuration, only one waveguide switch is used; its positions are antenna and dummy load. Auxiliary switch terminals A through F are used to route position-indication signals to connector P11 (mounted in the shelter) and to relay assembly 1A15A18 in the transmitter. Figure 2-29 is a simplified schematic diagram of the connections. The waveguide switch is shown in the figure in the dummy load position. In this position, P11-J and -L are connected together through switch terminals E and F and P11-K is open circuit. The connection from terminal A of the waveguide switch to 1A15J4-g is open circuit. For dummy load position relay 1A15A18K4 is not energized (para 2-64.1). For the antenna position of the waveguide switch, terminal B is connected to terminals A and D and terminals E and F are open circuit. P11-K is then connected to +28 Vdc and P11-J and -L are open circuit. The +28 Vdc at terminal B is connected through terminal A and 1A15J4-g to relay 1A15A18K4. For the antenna position, relay 1A15A18K4 is energized (para 2-64.1).

#### b. AN/GRC-144(V)4 C-band/K-band Configuration

In this configuration two waveguide switches are used. The position indication signals are routed to the FREQUENCY BAND IN USE (GHZ) indicator at STATUS PANEL 3A8 in Unit 3 and to relay assembly 1A15A18 in the transmitter. Figure 2-30 is a simplified schematic diagram of the connections. The waveguide switches are shown in the figure in the C-band position. In this position, the +28 Vdc source in the transmitter supplies the voltage (at 3A7J2-E and -H) to light the indicator at STATUS PANEL 3A8. The +28 Vdc at 3A7J2-H is also connected to 3A7J2-W and through the waveguide switch to 1A1534-g and 1A15A18K4. For K-band position, the +28 Vdc is connected through the waveguide switches to 3A7J2-F and -G and to STATUS PANEL 3A8. It is also connected from 3A7J2-F to 3A7J2-V and applied through the waveguide switch to 1A15J4-g and relay 1A15A18K4. Note that for either C-band or K-band position of the waveguide switches, +28 Vdc is routed to STATUS PANEL 3A8 and to relay 1A15A18K4 through both transmit and receive waveguide switches. Thus, unless both waveguide switches are in the same band position, the signal paths described above are incomplete. The chart below lists the indications at STATUS PANEL 3A8 for each condition described; it also shows the corresponding status of relay 1A15A18K4. Operation of relay assembly 1A15A18 is described in paragraph 2-64.1. The bottom section of the chart lists STATUS PANEL indications for the K-band only configuration for reference in c below.

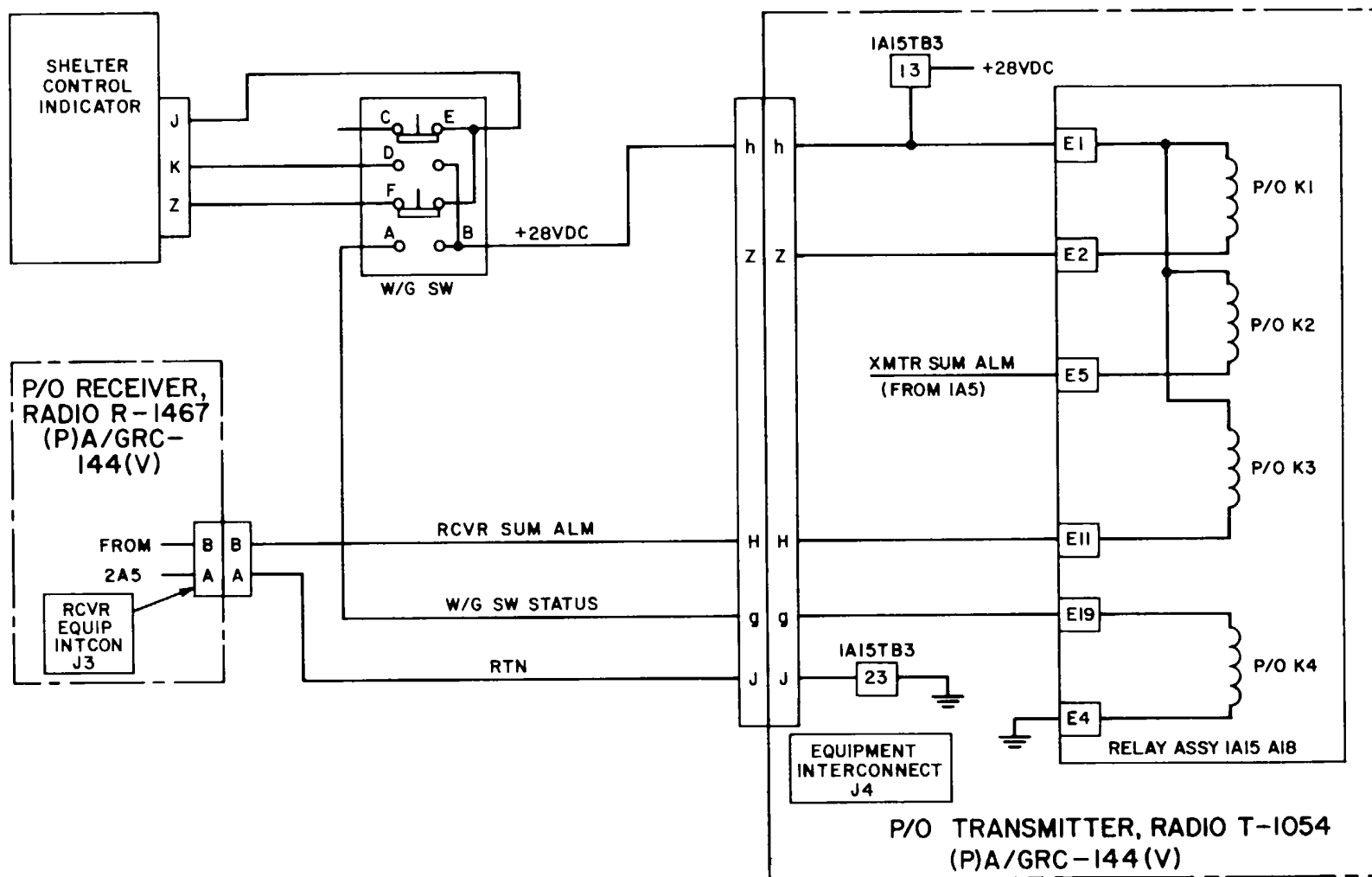
AN/GRC-144(V)4 Waveguide Switch Status Indications

Operating Mode	Waveguide Switch Position	STATUS PANEL 3A8		Relay 1A15A18K4 Status
		FREQUENCY BAND IN USE (GHZ)		
		4.4 to 5.0	14.4 to 15.0	
Dual Band (2 W/G Switches)	Both in C-Band	Green	White	Energized
	Both in K-Band	White	Green	Energized
	Switches not in same band position	Not Lighted	Not Lighted	Not Energized
K-Band Only (1 W/G Switch)	Antenna	White	Green	Energized
	Dummy Load	White	White	Not Energized

c. AN/GRC-144(V)4, K-Band Only (Optional Configuration). In this configuration, only one waveguide switch is required; its positions are antenna and dummy load. Figure 2-31 is a simplified schematic diagram of the connections. The waveguide switch is shown in the dummy load position. In this position, +28 Vdc is connected through the waveguide switch to 3A7J2-H to light the K-band (14.4 to 15.0) indicator (white) at STATUS PANEL 3A8. Connector 3A7J2-V applies +28 Vdc constantly (not switched) to the C-band (4.4 to 5.0) indicator (white) which is then always lighted white in this configuration. The connection from

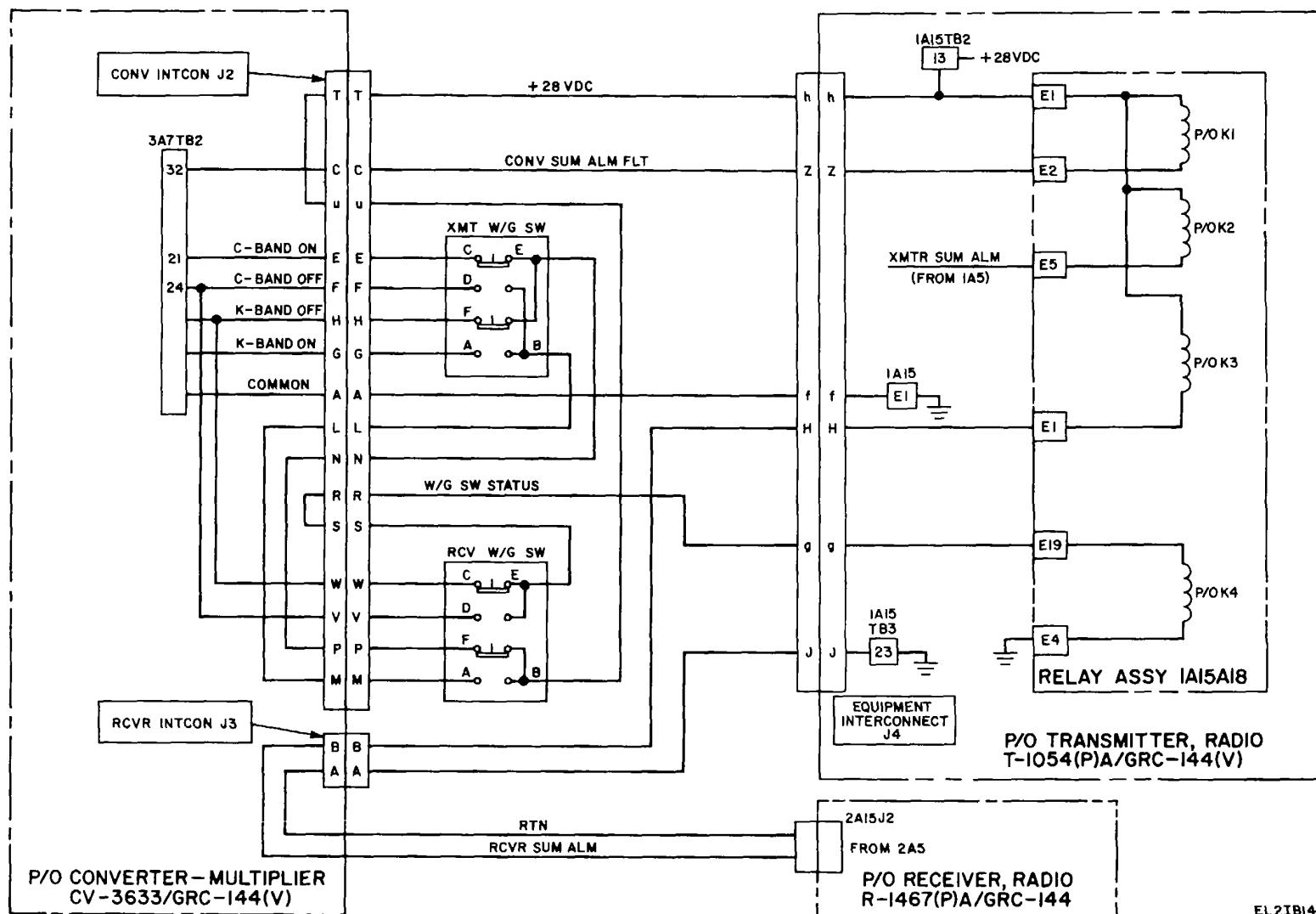
waveguide switch terminal B to relay 1A15A18K4 is open circuit and relay K4 is not energized. In the antenna position, +28 Vdc is connected through the waveguide switch to 3A7J2-G and -R. The signal at 3A7J2-G lights the K-band indicator (green) at STATUS PANEL 3A8. The signal at 3A7J2-R is applied to relay 1A15A18K4 which is then energized. The chart above shows the STATUS PANEL indications and the corresponding status-of relay 1A15A18K4 for both positions of the waveguide switch.





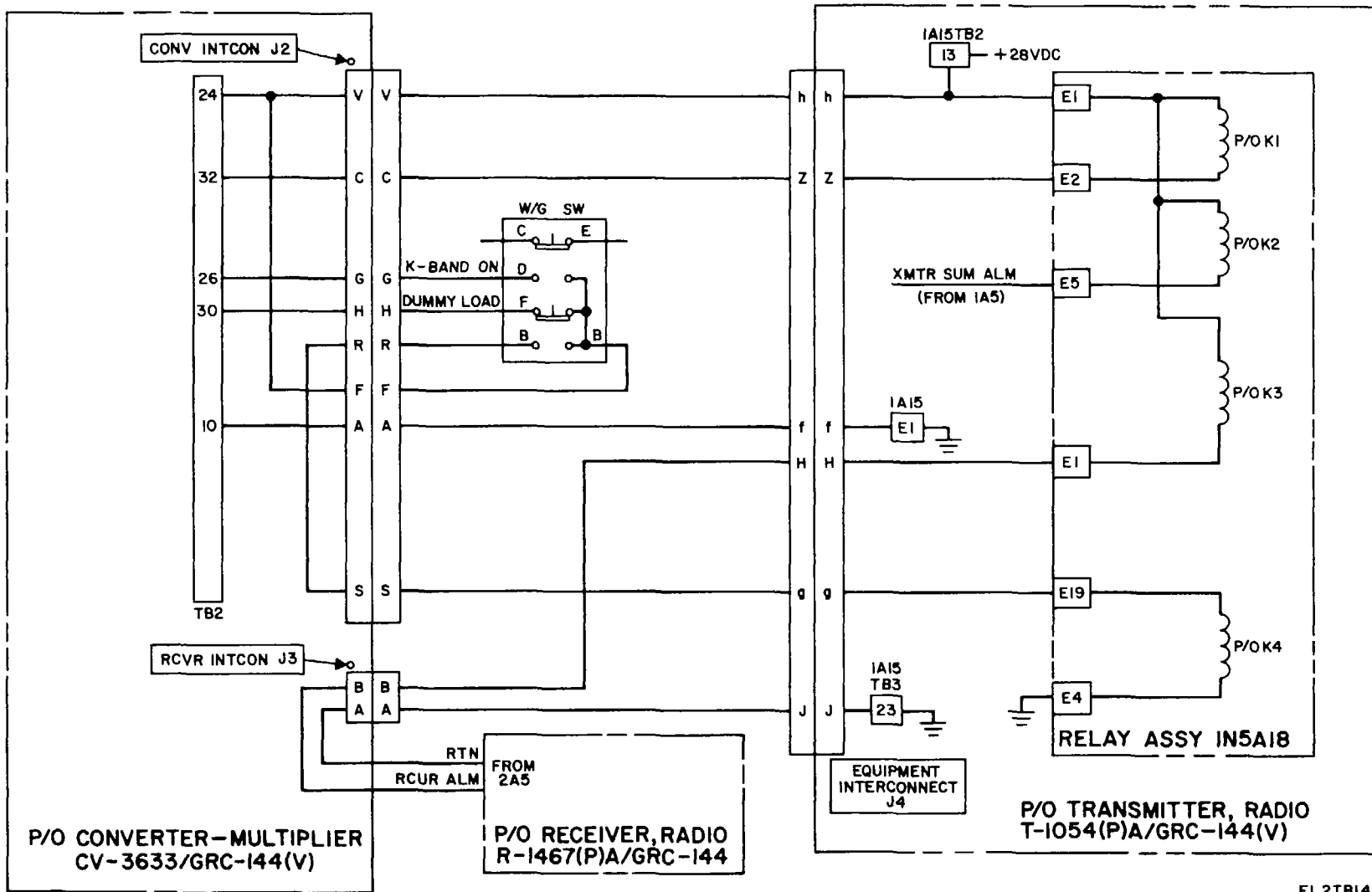
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Figure 2-29. AN/GRC-144(V)3 waveguide switch position indicator simplified schematic diagram.



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Figure 2-30. AN/GRC-144(V)4 waveguide switch position indicator simplified schematic diagram.



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Figure 2-31. AN/GRC-144(V)4 optional configuration waveguide switch position indicator simplified schematic diagram.

**Section VI, FUNCTIONING OF CONVERTER-MULTIPLIER ASSEMBLY CV-3633/GRC-144(V) CIRCUITS**

**2-81. General**

This section covers the functioning of circuits used in Converter-Multiplier Assembly CV-3633/GRC-144(V), Unit 3. The coverage is not presented in sequential reference designation order but in the functional operating sequence and is at the schematic diagram level. Circuit functioning and schematic diagrams are not provided for the nonrepairable assemblies (i.e. BP filters 3A3 and 3A4, circulator 3HY1, etc). Circuit descriptions for cabinet mounted components such as rfi filters are covered in this section. All electrical equipment cabinet 3A7 mounted circuits and all interconnections in the CV-3633/GRC-144(V) are shown in figure 5-98 and subassembly schematic diagrams are shown in figures 5-99 through 5-106.

**2-82. Chassis, Electrical Equipment 3A7**

Chassis, Electrical Equipment 3A7 contains all necessary wiring that interconnect components of an operable AN/CRC-144(V)4 radio set together. Primary 115-120 Vdc power (fig. 2-32) is applied and returned to source through connector J1 at pins A, B and C. The primary power is then distributed through terminal boards to Receiver, Radio R-1467(P)A/QCC-144 by cable assembly connector P1 pins A, B and C and to the status panel 3A8 by cable assembly connector P2, pins A1, A3 and A4. The status panel contains POWER ON/OFF switch 3A8S1 and the necessary fuses to protect the CV-3633/GRC-144(V) circuits and is discussed in paragraph 2-83. When the status panel POWER ON/OFF switch is in the ON position, primary power is applied to power transformer 3A7T1 and amplifier-multiplier 3A5 heater circuits consisting of thermostat 3A5S1 and heater 3A5HR1 through

connector plug P2 pins A6, A8 and A5, and rfi filters 3ATFL1 through 3A7FL3. Filters, rfi 3A7FL1, 3A7FL2 and 3A7FL3 prevent unwanted interference of electromagnetic radiation of radio frequency from transformer 3A7T1 and amplifier-multiplier 3A5 heater circuits from entering into the operating circuits.

a. Transformer 3A7T1 is a step down transformer with a single primary and four secondary windings. Each secondary winding is connected to power supply 3A6 rectifying and control circuits (refer to paragraph 2-84 for circuit descriptions). The RMS voltage output of each transformer secondary winding is as follows:

<u>Winding</u>	<u>Voltage</u>
3-4	95V RMS
5-7 (CT)	7-2V RMS
8-9	14.7V RMS
10-11	14.7V RMS

b. Direct current (dc) power (fig. 2-33) is distributed from power supply 3A6 through terminal boards to the CV-3633/GRC-144(V) amplifier-multiplier 3A5, alarm monitor 3AI, frequency electronic converter 3A2, status panel 3A8 and air flow sensor circuits consisting of thermostat 3A7S1 and air flow sensor 3A7S2. The power supply 3A6 +100 Vdc is applied to amplifier-multiplier 3A5 current regulator 3ASA8 circuits through connector XA5 pins 3 and 4. The power supply 3A6 +28 Vdc is applied to the

CV-3633/GRC-144(V) modules through the various terminal board and connector pins shown in figure 2-33 and is used to provide the bias voltages for transistor and integrated circuit operation, closure voltage for relay operation, illuminates all monitor and fault indicators and provides operating voltage for electronic frequency converter tunnel diode amplifier 3A2A1 and local oscillator 3A2A3. The +28 Vdc is also switched by amplifier-multiplier 3A5 thermostat 3A5S2 to illuminate status panel 3A8 TEMP indicator green or red indicating amplifier-multiplier 3A5 temperature normal and alarm conditions respectively. In addition, the air flow sensing switch 3A7S2 heating element is powered by +28 Vdc through rfi filters 3A7FL4, 3A7FL5 and 3A7FL8 that prevent unwanted interference of electromagnetic radiation of radio frequency from the opening or closing of thermostat 3A7S1, air flow sensing switch 3A7S2, or status panel 3A8 OSC TEMP indicator PUSH TO TEST switch 3A8DS1.

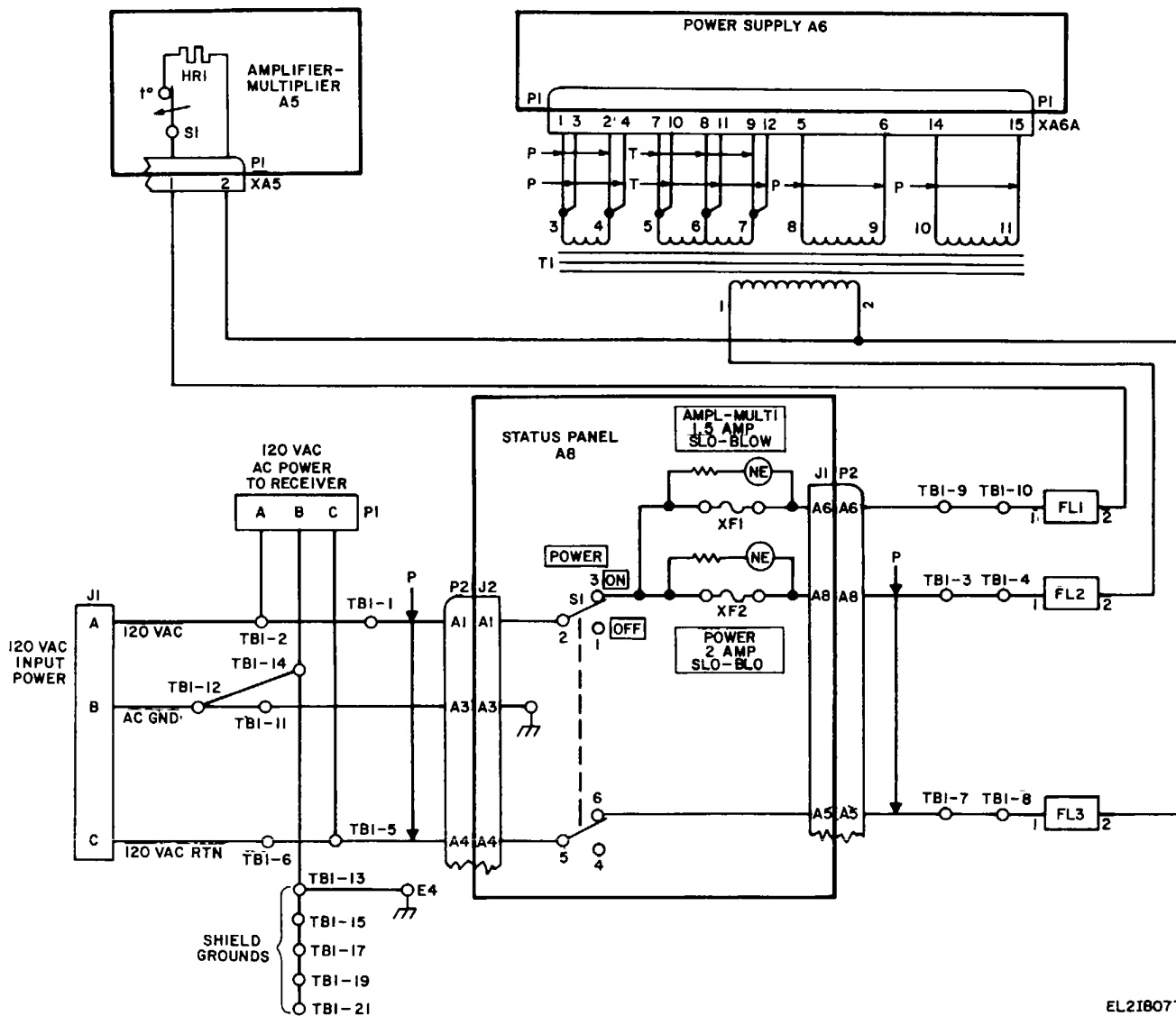
c. Under ambient operating temperatures and temperatures below approximately 140° F (60° C), thermostat 3A7S1 is closed applying +28 Vdc to a heating element in air flow sensing switch 3A7S2. When the air flow sensing switch 3A7S2 temperatures are maintained by adequate air flow from the R-1467(P)A/GRC-144 blower 2A1561, airflow sensing switch is closed applying +28 Vdc to alarm monitor 3A1 air flow fault relay 3A1K2 through rfi filter FL8-A3 and connector 3AXAI pin 14. If adequate air flow from blower 2A1581 is not maintained, air flow sensing switch

opens deenergizing air flow fault relay 3A1K2. If the air flow fault relay is energized because of adequate air flow or deactivated by thermostat 3A7S1 when the CV-3633/GC-144(V) operating temperatures; are above approximately 158°F (70°C); the status panel lamp 3A80S2 illuminates AIR FLOW fault indicator monitor green. When the air flow fault relay is deenergized because of inadequate air flow the status panel lamp 3A80S4 illuminates AIR FLOW fault indicator monitor red. Refer to paragraph 3-87 for a complete description of alarm monitor 3A1 circuit functioning.

d. Mounted on the electrical equipment chassis 3A7 are the necessary components to rf couple operating modules of the CV-3633/GRFC-144(V) and antenna system together (fig. 2-34). The transmit and receive paths from Transmitter, Radio T-1054(P)A/IRC-144 and Receiver, Radio R-1467(P)A/GFC-144 to and from the antenna system through the electrical equipment chassis 3A7 components are described in (1) and (2) below.

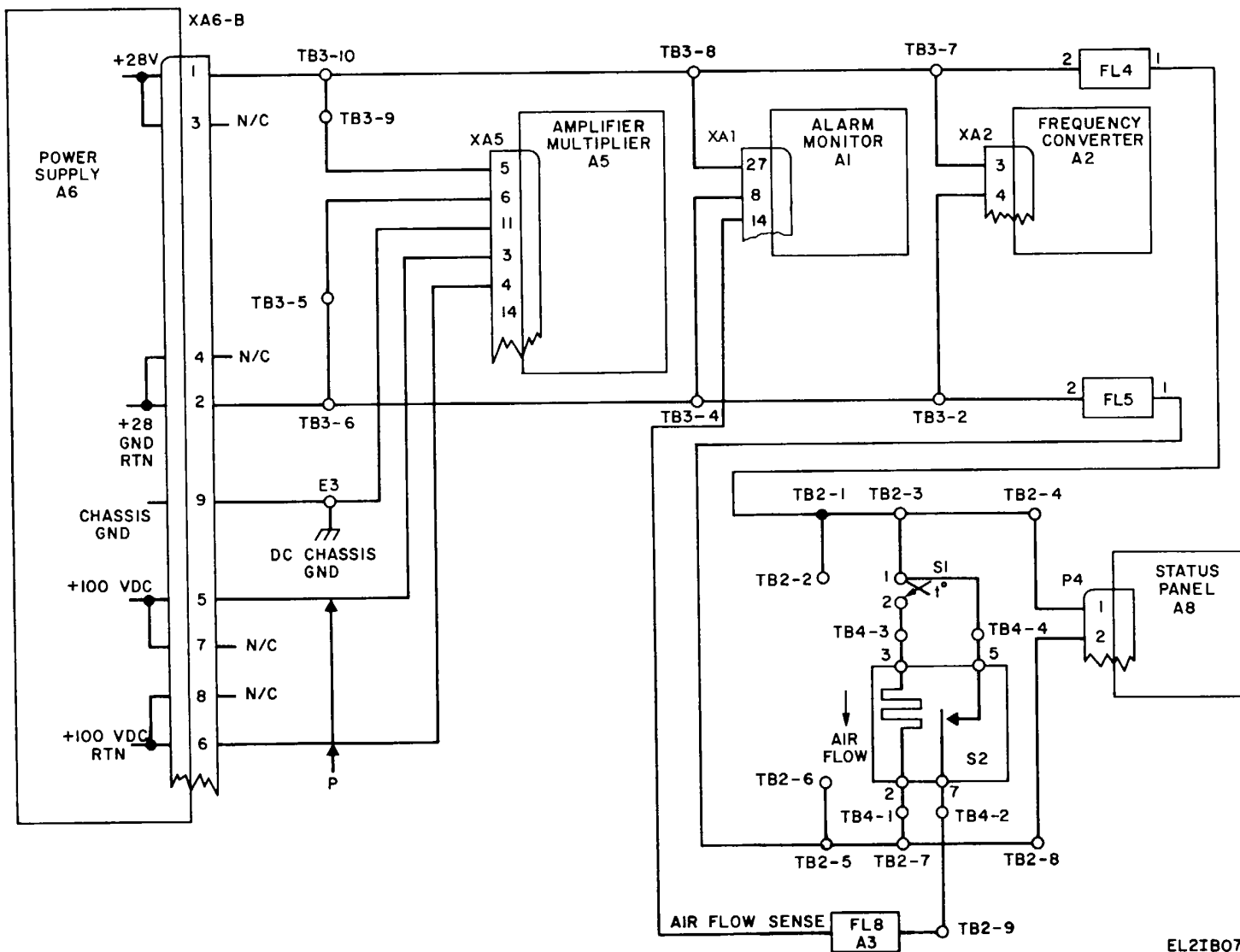
(1) The C-band 4.8 to 5.0 GHz output from Transmitter, Radio T-1054(P)A/GRC-144 is applied to the CV-3633/GRC-144(V) amplifier multiplier 3A5 circuits. Amplifier multiplier 3A5 is a fixed tuned broadband amplifier that contains a X3 multiplier 3A5A1 and impatt amplifier circuits and a constant current source 3A5A8. The amplifier-multiplier circuits up-convert the 4.8 to 5.0 GHz

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Figure 2-32. Converter-Multiplier CV-3633/GRC-144(V) Primary Power Distribution.



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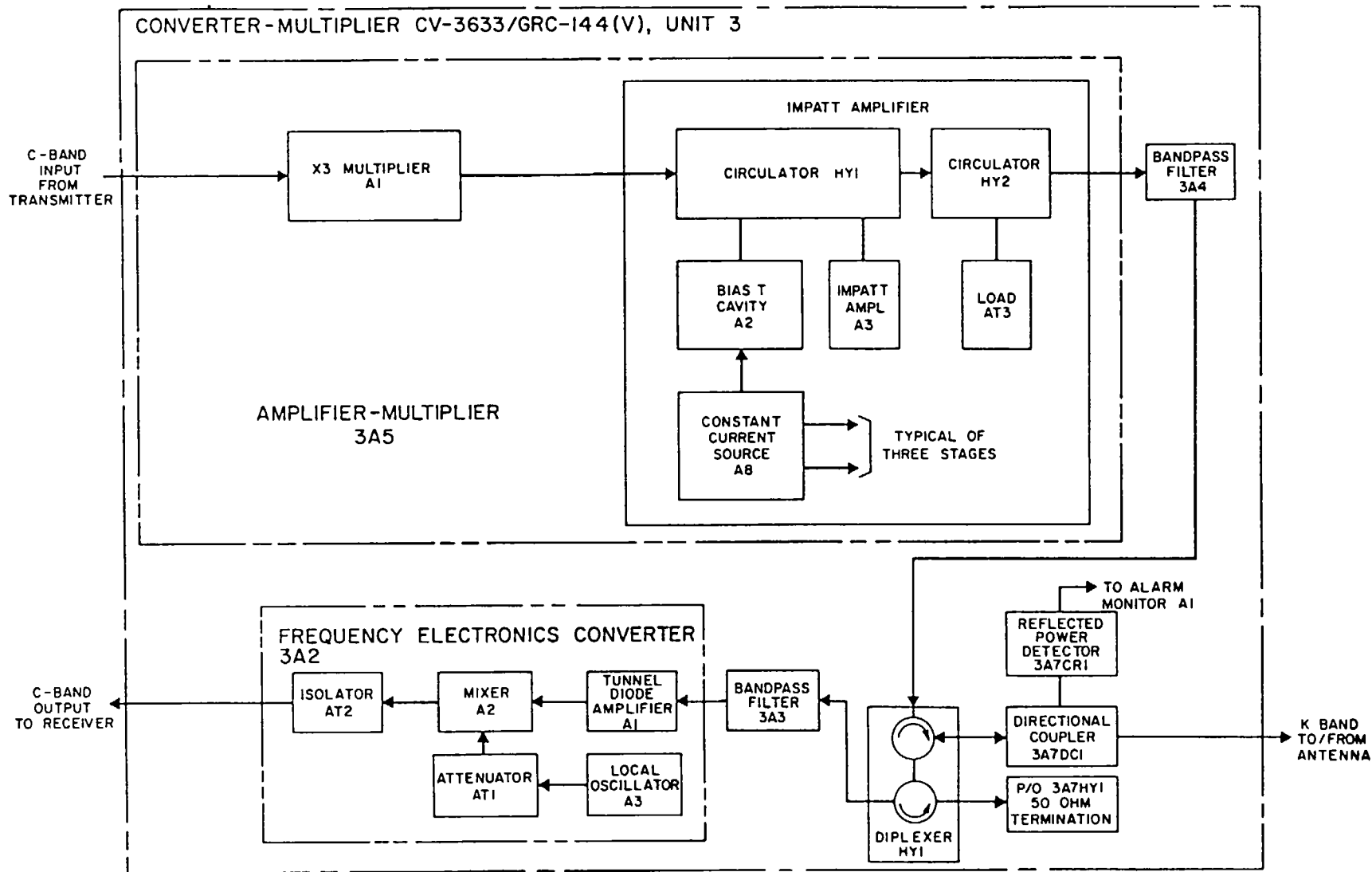
Figure 2-33. Converter Multiplier CV-3633/GRC-144(V) DC Power Distribution.

rf input to 14.4 to 15.0 GHz and amplifies it sufficiently to provide a 250 mw nominal output at the electrical equipment chassis 3A7 J4 ANT waveguide output. Refer to paragraph 2-86 for a complete description of amplifier multiplier 3A5 circuit functioning. The rf output from amplifier multiplier 3A5 RF OUTPUT waveguide flange is applied to the input waveguide flange of bandpass filter 3A7A4 that is a tunable frequency selective filter whose output is connected at a rear waveguide flange to diplexer 3A7HY1. The bandpass filter 3A7A4 is used for tuning (attenuating frequencies on either side of tuned frequency) amplifier-multiplier 3A5 output signals to the antenna. Diplexer 3A7HY1 permits diplexing (simultaneously sending and receiving) the 14.4 to 15.0 GHz band frequency from Antenna AS-3398/GRC-144(V) using a common antenna and waveguides. The diplexer 3A7HY1 is rf connected to BP filter 3A4 through waveguide adapter 3A7W4 and to the antenna system through directional coupler 3A7DC1. Diplexer 3A7HY1 (fig. 2-34) consists of two circulators which route transmit and receive signals into the required paths. In each circulator, the RF energy entering at any port circulates in the direction indicated by the arrow and exits at the next circulator port. Directional coupler 3A7DC1 and power detector 3A7CR1 serve as the sensing network to detect reflected forward power fault conditions

when the shelter waveguide or antenna system cause a sufficiently high voltage standing wave ratio (VSWR) to exist because of faulty waveguide connections, water, etc. The reflected 14.4 to 15.0 GHz rf power is rectified by power detector 3A7CR1 to provide the dc signal to operate alarm monitor 3A1 reflected power monitor circuits (para 2-87).

(2) The K-band 14.4 to 15.0 rf signal from the antenna is applied to the transmit/receive port 2 of diplexer 3A7HY1. Diplexer 3A7HY1 routes the rf input frequency to bandpass filter 3A3 and frequency converter 3A2. Bandpass filter 3A3 is used to tune the input frequency for down-conversion to 4.4 to 5.0 GHz by the electronic frequency converter 3A2. The diplexer 3A7HY1 is rf connected to BP filter 3A3 through waveguide adapter 3A7W4 and to the antenna system through directional coupler 3A7DC1. Electronic frequency converter 3A2 consists of tunnel diode amplifier 3A2A1, mixer 3A2A2, local oscillator 3A2A3, attenuator 3A2AT1 and isolator 3A2AT2 circuits whose functional descriptions are provided in paragraph 2-84. The output signal from the isolator 3A2AT-2 is the down-converted 4.4 to 5.0 GHz output from Converter-Multiplier CV-3633/GRC-144(V) that is applied to Receiver, Radio R-1467(P)A/GRC-144 through the receiver waveguide switch through Adapter, Waveguide UG-1883/GRC.





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Figure 2-34. Converter-Multiplier CV-3633/GRC-144(V) Functional Block Diagram.

**2-83. Status Panel 3A8 Functioning**

Status panel assembly 3A8 (fig. 5-106) contains the main power switch protective fuses and alarm indicators to monitor waveguide switch position and the CV-3633/GRC-144(V) and R-1467(P)A/GRC-144 operation. A description of primary power distribution through status panel 3A8 and electrical equipment chassis 3A7 is provided in paragraph 3-82. The POWER 2 AMP SLO-BLO fuse 3A8F1 protects amplifier-multiplier 3A5 heater 3A5HR1 and POWER 1.5 AMP SLO-BLO fuse 3A8F2 protects transformer 3A7T1 from overload conditions. Each fuse is housed in a fuse holder 3A8FX1 and 3A8FX2 that contain a neon indicator that illuminates if a fuse is open. Status panel 3A8 AIR FLOW indicator is discussed in paragraph 2-82c and 2-87 along with alarm monitor 3AT circuit descriptions. All indicators 3A8DS1 through DS13 have one side connected to ground. The other side receives either a +28 vdc signal (indicator ON) or an open circuit signal (indicator OFF) from the monitored circuit through 3A8J1. Normal/fault status indicators AIR FLOW, TEMP, and ALARM SUMMARY are lighted green for normal status and red for fault status. OSC TEMP and FREQUENCY BAND IN USE (GHZ) are operating mode status indicators. OSC TEMP (white) cycles ON/OFF as the oscillator temperature varies. For C-band operation, the upper part, 4.4 to 5.0, of FREQUENCY BAND IN

USE (GHZ) indicator is lighted green and the lower part, 14.4 to 15.0, is lighted white. For K-band operation the colors are reversed. The control signals are generated by the waveguide switches (para. 2-80)

**2-84. Power Supply 3A6 Functioning**

Power Supply 3A6 (fig. 5-103) rectifies ac power from transformer 3A7T1 to provide the required dc operating power for the alarm monitor 3A1, electric frequency converter 3A2 and amplifier-multiplier 3A5 circuits. Power supply 3A6 contains +28 Vdc and +100 Vdc rectifier and regulator circuits. There are also two thermal switches 3A6S1 and 3A6S2 that protect power supply 3A6 +28 Vdc and +100 Vdc circuits from damage due to excessive temperatures caused by circuit overloading. As described in paragraph 2-81, 120 Vac power is stepped down by transformer 3A7T1. The outputs from the secondary windings provide the appropriate voltages for the 28 volt 3A6CR5 and 3A6CR6 rectifiers, 100 volt 3A16CR1 through 3A6CR4 rectifiers, +28 V regulator and +100 V regulator boards 3A6A1 (fig. 5-104) and 3A6A2 (fig. 5-105). The following secondary transformer 3A7T1 windings listed below supply ac power to power supply 3A6 rectifier circuits.

<u>Winding</u>	<u>Voltage</u>	<u>Power Supply 3A6 Rectifiers</u>
3-4	92V RMS	CR1 through CR4
5-7	72V RMS	CR5 and CR6
8-9	14.7V RMS	A2CR1 through A2CR4
10-11	14.7V RMS	A1CR1 through A1CR4

The circuit description for the +100 V and +28 V rectifier circuits are provided in the following subparagraphs.

a. +100 V Rectifier Circuits. The 100-volt rectifier produces approximately 126 VDC. In this circuit, power from transformer windings 3-4 (95 VRMS) is applied to the fullwave bridge rectifier formed by diodes 3A6CR1 through 3A6CR4. Parallel connected filter capacitors 3A6C1 through 3A6C4 smooth the rectifier ripple, and Darlington connected transistors 3A6Q1 and 3A6Q2 act as the regulator series pass transistors. Silicon controlled rectifier 3A6Q3 forms an overvoltage crowbar circuit across the rectifier output terminals, pins 5, 6, 7 and 8 of connector 3A6P2. The crowbar circuit short-circuits the regulated output in the event of a regulator failure, or momentary overvoltage condition. Control voltages for the series regulator and crowbar circuits are obtained from +100 V regulator printed wiring board assembly 3A6A2 through terminals 3A6A2E3 through 3A6A2E7. The output voltage of the regulator is sensed by the control circuit through terminals 3A3E5 and 3A3E6. In turn, the control circuit (fig. 5-105) precision voltage regu-voltage at terminal 3A3E3, which varies the voltage across the series pass transistors (3A6Q1 and 3A6Q2) so a constant output voltage is maintained. Resistor 3A6R2 provides a path for any low level base to emitter current through pass transistor 3A5Q1 and 3A6Q2 when they are cut off. This assures that the pass transistors will not conduct due to noise in the control circuits. Current limiting is initiated by the action of sensing resistor 3A6R3 which causes a voltage representative of the load current to be applied to the current sensing terminals (3A6A2E4 and 3A6A2E6) of the control circuit. Thermal protection for the regulator components is provided by switch 3A6S2. This switch senses the heat sink temperature of the Darlington pair between the limits of 230 and 260 degrees F, and opens

if an excessive temperature develops.

(1) Within control circuit 3A6A2 (fig. 5-105) develops a corrective lator 3A6A2Q1 develops the pass transistor control voltage and current limiting control signals; and transistor stage 3A6A2Q1 provides the overvoltage trip signal. Power to operate the control circuit is derived by a bridge rectifier (A2CR1-A2CR4), which is energized by a separate secondary winding (pins 3A7T1-5 and 3A7T1-6) on 3A7 transformer 3A7T1. Voltage regulator 3A6A2U1 contains a reference voltage amplifier, a differential error amplifier, a current limiting transistor, and a series pass output transistor. The reference amplifier output of 7.15 volts appears at pin 3A6A2U1-6. This voltage is connected to the voltage sensing network formed by resistors 3A6A2R4 and 3A6A2R5, potentiometer 3A6A2R3, and 6.3 volt zener diode 3A6A2VR2. The divider network establishes a reference level at the noninverting input to the error amplifier (pin 3A6A2U1-5). The tap on potentiometer 3A6A2R3 picks off a voltage which is proportionate to the regulator output, and therefore causes changes in the output voltage to be proportionately applied to the inverting input (pin 3A6A2U1-4) of the error amplifier. If a rise in output voltage occurs due to a change in load, the output of the error amplifier proportionately becomes more positive. This causes the series pass transistor in regulator 3A6A2U1 to conduct less and thereby decreases the voltage at terminal 3A6A2E3. In turn, conduction through Darlington pair 3A6Q1-3A6Q2 is reduced, causing the regulator output voltage to decrease to the nominal level determined by the setting of potentiometer 3A6A2R3. Decreases in the supply output voltage create the opposite reaction to that explained above.

(2) Foldback current limiting is provided by the current limiting transistor within voltage regulator

3A6A3U1. This transistor is normally biased off by the voltage at the junction of divider resistors 3A6A3R1 and 3A6A3R2, applied at pin 3A6A3U1-2. When an overload occurs, the increased voltage drop across current sensing resistor 3A6R3 causes the current limiting transistor in 3A6A3U1 to conduct, and bias the series pass transistors toward cut off. As a result, the voltage drop across the series pass transistors increases greatly, causing the output voltage to drop to a very low level and thereby limit the load current. When the cause of the overload is removed, the current limiting transistor cuts off and the circuit automatically resumes regulation at the preset level. Bypass capacitors 3A6A3C3 and 3A6A3C3 and 3A6A3C6 limit the circuit response to short duration spurious noise pulses. Capacitor 3A6A3C2 introduces a rolloff in the error amplifier high frequency response and thereby prevents parasitic oscillation.

(3) Overvoltage protection is provided by the crowbar control circuit (3A6A3Q1 and SCR 3A6Q3). Stage 3A6A3Q1 senses the output voltage between terminal 3A6A3E5 and 3A6A3E6, and triggers SCR.3A6Q3 into conduction when the overvoltage limit is reached. The overvoltage limit is set by potentiometer 3A6A3R3, which controls the bias applied to transistor 3A6A3Q1. When an overvoltage condition develops, transistor 3A6A3Q1 becomes forward biased and conducts through pulse forming network 3A6A3C4-3A6A3R9, which forms the trigger pulse. Once triggered, SCR 3A6Q3 impresses a heavy load at the circuit output terminals and thereby causes current foldback through the limiting circuit described above. Because of the nature of SCR 3A6Q3, the CV-3633/GRC-144(V) power supply must be momentarily turned off to reset the SCR crowbar circuit. If the cause of the overvoltage condition is a shortcircuited series pass transistor (3A6Q1 or 3A6Q2), the triggering of SCR 3A6Q3 will cause fuse F1 to open. This prevents the power supply from being reset even through the supply

has been momentarily turned off. Capacitor 3A6A3C5 suppresses transient noise spikes which put transistor 3A6A3Q1 into conduction, thereby eliminating undesirable crow-barring. Resistor 3A6A3R6 limits the base drive current' through transistor stage 3A6A3Q1.

b. +28 V Rectifier Circuits. The 28 Vdc rectifier circuit and its regulator control printed wiring board A1 (fig. 5-104), except for part values and designations function the same as the corresponding portions of the high voltage regulator-rectifier described above. Operating power for the 28-volt rectifier is obtained from the center-tapped winding (terminals 5, 6 and 7) of transformer 3A7T1. The 28-volt rectifier is full-wave using diodes 3A6CR5 and 3A6CR6. Transistors 3A6Q4, 3A6Q5 and 3A6Q6 form the 28-volt regulator series pass stage, and SCR 3A6Q7 provides the crowbar protection. Winding terminals 10 and 11 of transformer 3A7T1 provide operating power for control board 3A6A1 which functions the same as board 3A6A2. The +28 Vdc output and return is made available through pins 1, 3, 2 and 4 of connector 3A6P2.

## **2-85. Electronic Frequency Converter 3A2**

Electronic frequency converter 3A2 (fig. 5-100) performs as a K-band to C-band down converter, converting the incoming 14.4 to 15.0 GHz band frequency signal from Filter BP, 3A3 to 4.4 to 5.0 GHz.

a. The input signal at RF IN jack 3A2 A1J3 is a receive frequency in the K-band (14.4 to 15.0 GHz) range. The signal level at A1J3 is a nominal -40 dBm. Tunnel diode amplifier A1 provides a gain of 20 dB (min) to 23 dB (max) over the K-band range. There are three stages of amplification consisting of negative resistance tunnel diode amplifiers. The input and output impedances of A1 are 50 ohms and input

and output VSWR's are 1.25: 1 (max). The output signal, at a nominal level of -20 dBm, is applied through semirigid cable W3 to coaxial mixer 3A2A2.

b. Local oscillator 3A2A3 supplies the second input to mixer 3A2A2 for the down conversion of the RF signal to C-band range. Oscillator 3A2A3 is a voltage controlled oscillator with crystal oscillator frequency control of output signal frequency in a phase-lock loop circuit. To assure frequency stability and constant level output, the dc operating voltage is internally regulated and the crystal oscillator is enclosed in a temperature controlled oven. When BAND SELECT switch 3A2S1 is in position 1, the operating frequency of 3A2A3 is 10.00 GHz. When 3A2S1 is in position 2, 3A2A3 pin 7 is grounded at E1 through switch 3A2S1-2, 3A2SI-C and 3A2TB1 terminal 14; the frequency of A3 is then 10.02 GHz. In either case the frequency stability is 1 part in 107 per day. The output signal level is a nominal +13 dBm (11 dBm, min.; 15 dBm max.). This signal is applied through coaxial attenuator 3A2AT1 to mixer 3A2A2. Isolator 3A2AT1 has an attenuation of 3 dB; it isolates oscillator 3A2A3 from the loading effects of 3A2A2 for frequency and signal level stability. The conversion process in 3A2A2 produces a signal power loss of 10.5 dB (max.). The output signal from 3A2A2 consists of the input signals and the sum and difference frequencies and their harmonics. Isolator 3A2AT2 (0.5 dB insertion loss) provides an impedance matching load for 3A2A2. The RF OUT signal at jack 3A2AT2J2 is routed to a receiver. The desired operating frequency signal (RF frequency minus local oscillator frequency) is selected by a bandpass filter in the receiver.

c. An oven temperature monitor in the 3A2A3 supplies a status signal at connector 3A2A3 pin 9. This signal is routed through filter 3A2FL2 and connector plug 3A2P1 pin 7 as an OSC TEMP NORM signal to illuminate the

status panel 3A8 OSC TEMP indicator when the local oscillator 3A2A3 oven is on. TP1 is colored black and resistors 3A2R2, 3A2R3 and potentiometer 3A2R4 form the divider network that scales the power monitor signal current for a test meter indication of between 60 and 140 (25.0 +8.0 ua) on Receiver, Radio R-1467(P)/A/GRC-144 meter panel assembly 2A15A2 meter when the power level is in the normal range. The LO POWER signal is also routed through filter 3A2FL3 and connector plug 3A2P1 pin 8 as an LO PWR monitor signal to the alarm monitor 3A1 circuits. Test point TP2 +28 V at 3A2J2 is the +28 Vdc operating voltage monitor point. TP2 is colored black and resistor R1 scales the current for indication in the test meter black band for normal range. Readings at all the test points are taken by means of a test lead from the test meter at the panel of the R-1467(P)/A/GRC-144.

## 2-86. Amplifier-Multiplier 3A5

Amplifier-Multiplier 3A5 (fig. 5-101) performs as a C-band to K-band up converter, converting the Transmitter, Radio T-1054(P)/A/GRC-144 4.8 to 5.0 GHz band frequency signal to 14.4 to 15.0 GHz. It is a fixed-tuned broadband amplifier and frequency multiplier. The frequency multiplier 3A5A1 (fig. 5-101.1) is comprised of a frequency tripler-amplifier A1A1 and converter-regulator A1A2. The fixed tuned broadband amplifier portion is comprised of three impatt amplifiers and associated circuits, including current regulator 3A8.

a. The signal at J1 RF IN is a transmit signal in the C-band range, at a level of +24 dBm (min.). This signal is coupled through circulator A1A1HY1. Circulator A1A1HY1 is a 4.8 to 5.9 GHz ferrite device that isolates 3A5A1 from the transmit circuit and acts as a termination for the cable. The frequency tripler portion A1A1Z1, Z2 and field effect transistor (FET) Q1 of frequency multiplier 3A5A1 is tuned to

the third harmonic of the input signal and isolated from, and coupled to the amplifier portion through circulator A1A1HY2. The amplifier portion of the frequency multiplier is a series of tuned FET circuits comprising Q2 and Q3 with tuned inputs and outputs. Transistors Q2 and Q3 input and output filters (Z3, Z4 and Z5) are tuned to the third harmonic, is the load impedance, and selects the third harmonic for each output. The output signal from frequency multiplier 3A5A1 is set for an input signal level of +24 dBm at 31 RF IN when the output level feeding cable W2 is +12.5 dBm, minimum. All power to operate the frequency multiplier is supplied by converter-regulator A1A2. Converter-Regulator A1A2 is a +28 vdc to +5 vdc and -5 vdc regulated converter that supplies bias voltages to frequency tripler amplifier A1A1 circuits as follows:

CONV-REG TERMINAL	VOLTAGE (DC)
E3	4.65 to 5.05 V
E4, E5	5.65 to 6.05 V
E6, E7	-0.5 to 0 V (R2 or R9 max ccw) -3.3 to -5.3 V (R2 or R 9 max cw)
E8	-1.65 to -2.65 V
E9	5.65 to 6.05 V (Test Point)
E10	-3.3 to -5.3 V (Test Point)

The converter-regulator is powered from the converter-multiplier power supply 3A6 (fig. 5-103). See figure 5.102-2. Voltage regulator VR1 is a linear +5 V, 1.OA regulator whose internal circuits contain short circuit and thermal shut down protective elements. Thermal shut down occurs whenever VR1 junction temperature is in excess of 150° C, Regulated +5 vdc is applied to frequency tripler-amplifier A1A1 circuits through relay K1 and to CMOS voltage converter IU1. The CMOS voltage converter performs supply voltage conversion

from an input of +5 (positive) to a -5 (negative) output voltage. The converter-regulator also has a turn-on protect circuit comprised of dual transistor Q1, associated bias resistors, capacitor C4 and relay K1. The dual transistor and associated circuits protect the frequency-amplifier 1A1A FET's, Q1 thru Q3, from burn-out by making certain that the -5 V is applied to the gates of Q1 thru Q3 prior to +5 V being applied to the drains. The +5 V keeps dual transistor Q1 turned off which in turn keeps relay K1 deenergized until the dual transistor Q1, biased by the -5 V, is turned on. When relay K1 is energized, +5 V is applied to frequency tripler amplifier A1A1 circuits. The +5 V to -5 V turn on delay is 5 msec minimum.

b. The impatt amplifier is comprised of circulators 3A5HY1 through 3A5HY4 and associated circuits; it provides a total gain of 13.5 dB in three stages. The first stage is a circulator coupled reflection amplifier consisting of 3A5A2, 3A5HY1 and 3A5A3, with a gain of 5 dB (input 14.5 dBm, output 19.5 dBm). Bias "T" cavity 3A5A2 is a biasing and impedance matching circuit for impatt diode 3A5A3CR1 (refer to para c and d below for the current regulator 3A5A8 functional description). Ferrite circulator 3A5HY1 provides the RF transmission path to the following stage and also provides RF isolation between the impatt diode and the driving source. Assembly 3A5A3 is a coaxial impatt diode mounting circuit with coaxial matching circuit for regenerative amplification. Impatt diode 3A5A3CR1 is a high efficiency (10%) silicon drift device with low thermal resistance (10° C/W). The output signal from the first stage is coupled to the second stage through isolating circulator 3A5HY2. The 50 ohm load 3A5AT3 is a termination for port 3 of 3A5HY2. The second stage amplifier, 3A5HY3, 3A5A4 and 3A5A5 provides a gain of 4.5 dB (19.5 dBm input, 24 dBm output). It is similar in operation to stage 1. The

third stage, 3A5HY4, 3A5A6 and 3A5A7 provides a gain of 4 dB (input 24 dBm, output 28 dBm). This stage is similar in operation to stage 1. The output port of 3A5HY4 is a waveguide which has a directional detector circuit to provide a dc indication of the output signal level for metering and status indication. The output signal (level +28 dBm, min.) is coupled to output flange RF OUT through a short length of waveguide, W3. This signal is coupled through bandpass filter A4 (fig. 2-31) to diplexer 3A7HY1.

c. Current regulator 3A5A8 (fig. 5-102) contains three current regulators that provide the constant current (high source impedance) bias supply required by the impatt diodes. The constant bias current outputs at 3A5A8E3, E4 and E5 are applied at bias "T" cavities 3A5A2 for diode 3A5A3CR1, at 3A5A5 for diode 3A5A6CR1 and at 3A5A7 for diode 3A5A6CR1 respectively. The input voltage for 3A5A8 is 100 vdc (regulated) applied at connector P1 pin 3 and pin 4 and 3A5A8 terminals E1 and E2.

d. In current regulator 3A5A8 (fig. 5-102) the +100 vdc input voltage at E1 is applied through a pi filter (L1, C1, C2) to current regulator stages 1, 2 and 3 with outputs at E3 (75 vdc, 105 ma., stage 1) E4 (75 vdc, 115 ma., stage 2) and E5 (75 vdc, 125 ma., stage 3). The three constant current regulator stages are identical in circuit and operation; the following description of circuit operation uses reference designations of stage 1. The output voltage from the pi filter is applied across a voltage divider; CR1, CR2, CR4, R3, R4 and R6 (ground). Zener diode CR4 maintains a constant voltage to ground at the junction

of R3 and CR2. Potentiometer R3 applies a fixed voltage at the base of transistor Q11 to set the operating point for the required bias current. The base-to-emitter voltage of both Q1 and Q2 is essentially fixed at 0.7 vdc and the voltage drop across R2 in the emitter circuit of Q2 is constant. The current through R2 is also constant and includes the current drawn by the impatt diode through E3 and Q3.

e. The RF output monitor signal DET OUT (fig. 5-101) is connected to A8-E8. On A8 (fig. 5-102), the signal at E8 is fed through R22 to E7 and to PI-9. Potentiometer R22 is adjusted to set the normal level of the signal. Resistors R21 and R23 divide this signal to provide the proper level at the test point PWR TP1. The +100 vdc input voltage is divided down by resistors R19 and R20 to provide the signal at test point +100 vdc TP2.

f. Heater 3A5HR1 (fig. 5-101) is connected to 120 Vac at 3A5PI-1 and -2; it is used to maintain a minimum temperature in 3A5. Thermostatic switch 3A5S1 controls 3A5HR1. Thermostat 3A5S1 opens at a temperature of  $30^{\circ} \pm 5^{\circ}\text{F}$  and closes at  $15^{\circ} \pm 5^{\circ}\text{F}$ . Thermostatic switch S2 is located in another area of 3A5 and acts as temperature monitor for the impatt diodes. In the normal position S2-2 and -3 are connected together; the TEMP NORM signal at P1-7 is then +28 vdc. If the temperature rises above  $210 \pm 40^{\circ}\text{F}$ , S2 operates to connect S2-1 to S2-2. The TEMP ALM signal at P1-8 is then +28 vdc. After a temperature alarm condition, the temperature must drop below  $185^{\circ} \pm 4^{\circ}\text{F}$  before 3A5S2 will reset to the normal position.

**Change 6 2-136.1/(2-136.2 blank)**

**2-87. Alarm Monitor 3A1**

Alarm monitor 3A1 (fig. 2-32) monitors status signals of Converter-Multiplier Assembly CV-3633/GRC-144 (unit 3). The characteristics, functions and sources of the input signals are described in (a) below. Output signals (b below) are routed to STATUS PANEL 3A8 (para 2-82). A converter summary alarm signal (c below) is routed to orderwire assembly 1A13 and applied to module 1A13A2 (para 2-8i). Figure 2-32 is a simplified schematic diagram that shows interconnections between monitored circuits, alarm monitor 3A1, and STATUS PANEL 3A8. Refer to figure 5-99 for the complete schematic diagram of alarm monitor 3A1.

a. Alarm monitor 3A1 receives input signals from the monitored circuits at pins 14, 24, 25, 26, and 33.

(1) The signal at 3A1P1-33 comes from the thermostatic switch (S2) in amplifier-multiplier 3A5 (para 2-85f), and it is applied to the coil of relay K1. This signal is +28 vdc when the temperature in 3A5 is normal and it is 0 vdc (open circuit) when the temperature is out of normal range.

(2) The signal at 3A1P1-26 comes from the forward power monitor circuit in 3A5 (para 2-85e), and it is applied to pin 7 of voltage comparator U1A. The signal level is 0.5 +0.1 vdc (normal) or less than 0.15 Vdc (fault). U1A is a high gain amplifier with positive feedback. The positive feedback through R8 prevents oscillations when the output signal switches states, and also speeds up the transitions. The reference

voltage at U1A-6 is derived from the +28 Vdc supply through resistors R1, R2, and R3. It is set to a level of +0.15 Vdc by adjustment of R2. When the signal at U1A-7 is normal, it is higher than the reference signal at U1A-6, and the output signal at U1A-1 is high (open circuit). The supply voltage (+28 Vdc) through R4 and R6 then reverse biases diode CR1. When the signal at U1A-7 drops below 0.15 vdc (fault status), the output signal at U1A-1 changes to ground (0 Vdc). Diode CR1 is then forward biased, with ground at the cathode through R6.

(3) The signal at 3A1P1-25 comes from the local oscillator power monitor circuit in frequency converter 3A2 (para 2-85); and it is applied to pin 11 of voltage comparator U1C. The normal and fault levels of this signal and the operation of U1C are the same as those for U1A, as described in a(2) above. For normal status +28 Vdc is applied to CR3 through R15 and R17. For fault status ground is applied to CR3.

(4) The signal at 3A1P1-24 comes from the chassis mounted reflected power detector 3A7CR1 (para 2-82d(1)), and it is applied to pin 3 of amplifier U2. A reflected power signal level of 70 mv corresponds to an antenna VSWR of 1.5: 1, so the reflected power signal level is normally less than 70 mv. If the antenna VSWR is greater than 1.5: 1, the reflected power signal will be greater than 70 mv (fault). Amplifier U2 has a gain of 10 and the output signal at U2-6 is normally less than 700 mv. An output level greater than 700 mv indicates fault status. This signal is connected through resistors R35 and R37 to test point J2 (TP2 REFLD PWR), and it is also



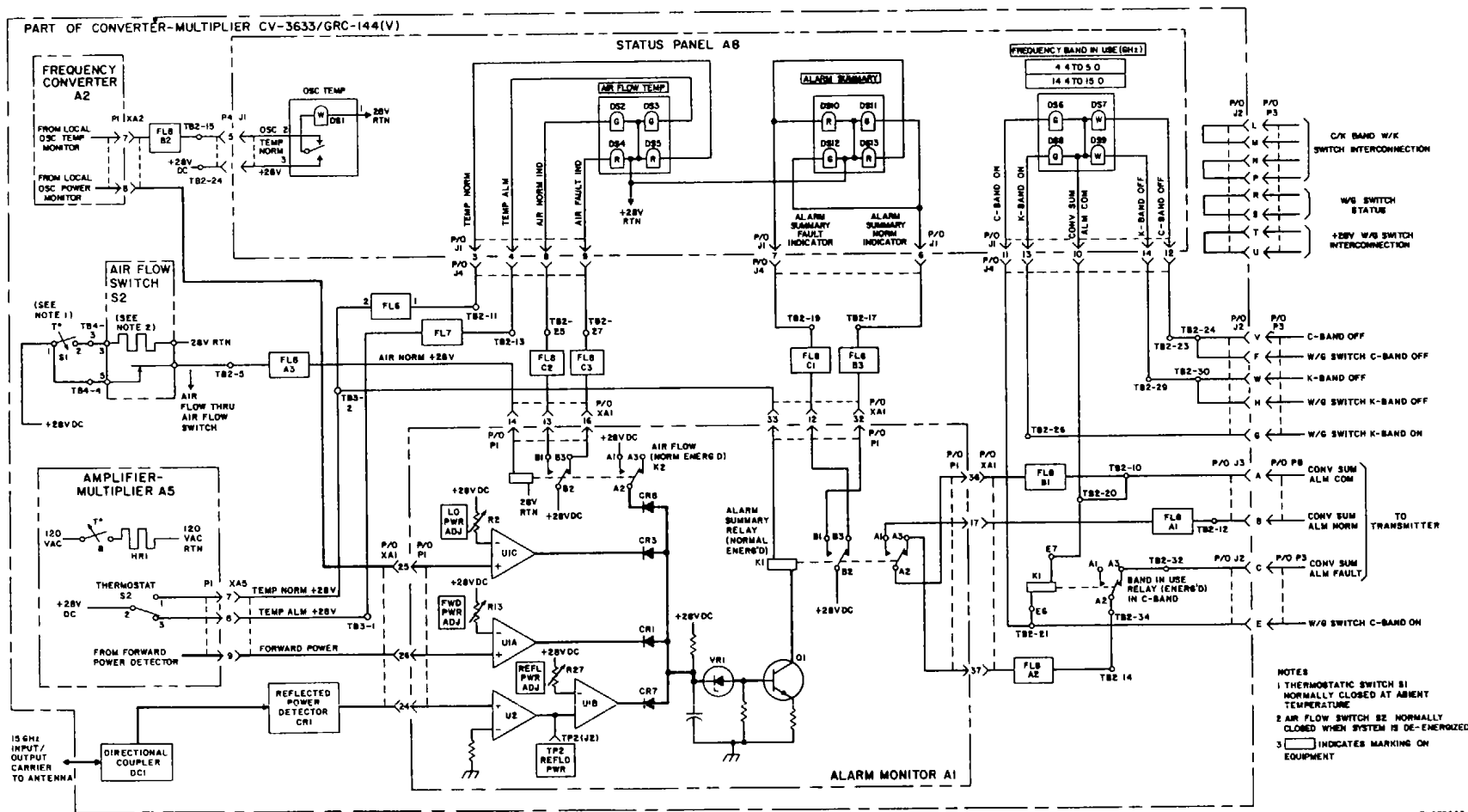


Figure 2-35. Converter-Multiplier CV-3633/GRC-144(V) alarm circuit diagram.

connected through R32 to pin 4 of threshold detector U1B. The signal level at U1B.4 is normally less than 700 mv and for fault status it is greater than 700 mv. A reference signal at U1B-5 is derived from +28 vdc through

R25, R27 and R28 and the level is adjusted (R27) to slightly less than 700 mv. The output signal at U18-2 is normally high (open circuit) and +28 vdc through R30 and R33 reverse biases CR7. For fault status the signal at U18B-2 is ground and CR7 is forward biased.

**Change 6 2-139**

(5) The signal 3AIP1-14 comes from the chassis mounted temperature monitor, thermostatic switch 3A7S2 (para 2-82), and it is applied to the coil of relay 3A1K2. This signal is either +28 Vdc (normal) or open circuit (fault). For normal status, +28 Vdc energizes relay K2, and +28 Vdc through closed contacts 82/B1 is applied to AIR FLOW indicator 3A8DS2 (green). DS2 is lighted. Contact K2-83 is open and AIR FLOW indicator 3A8DS4 (red) is off. At the same time, +28 Vdc through closed contacts K2-A1/A2 is applied through voltage divider resistors R22 and R23 to the cathode of diode CR6. CR6 is reverse biased. For the fault status, 0 Vdc (open circuit) at 3AIP1-14 causes K2 to be deenergized. Contacts K2-B2/B3 are closed and K2-B1 is open. The AIR FLOW red indicator lights and the green indicator is off. For fault status, closed contacts K2-A2/A3 apply open circuit to R22/R23 and diode CR6 is forward biased.

b. Diodes CR1, CR3, CR6 and CR7 comprise an OR gate. For normal status of the monitored signals, they are all reverse biased (a(2) through (5) above). Resistor R10 is then open circuit at the junction with the common anode connection of the diodes. The supply voltage (+28 Vdc) through R9, VR1, and R11 turns on VR1 (low impedance state) and forward biases transistor Q1. Relay K1 has +28 Vdc applied to the coil a(1) above) and Q1 is forward biased, so for normal status, K1 is energized. Closed contacts K1-B1/B82 apply +28 Vdc through 3A1P1-32 and cause ALARM SUMMARY indicator at 3A8 to light green (normal). Relay K1 will be deenergized if the +28 Vdc coil voltage is cut off or if Q1 is cut off. When K1 is deenergized, closed contacts K1-B2/B3 apply +28 Vdc through 3A1P1-12 and cause ALARM SUMMARY indicator to light red (fault). Relay K1 is deenergized if any one of the five monitored signals goes to fault status.

(1) If the temperature in 3A5 is out of normal range, the signal at

3A1P1-33 is open circuit. K1 has no coil voltage and is deenergized.

(2) If any of the signals at 3AIP1-24, -25, or --26 goes to fault status, the corresponding diode CR1, CR3 or CR7 will be forward biased (a(2), (3) and (4) above). When any OR gate diode (CR1, CR3, CR6, or CR7) is forward biased, a path to ground (a above) for +28 Vdc through R9, R10, and the diode is provided. The resulting voltage drop across R9 reduces the voltage applied to VR1. VR1 switches to the high impedance state and cuts off the voltage at the base of Q1. Q1 is then reverse biased; it cuts off and relay K1 is deenergized.

(3) If the signal at 3A1P1-14 goes to fault status, relay K2 is deenergized (a(5) above). CR6 is then forward biased, Q1 is cut off and relay K1 is deenergized.

c. The A-contacts for relay 3A1K1 are used to route the summary alarm signal of unit 3 to orderwire assembly 1A13 through J22-8 (CONV ALM NORM) and J22-C (CONV ALM FLT). Three combinations of logic signals at J22-B and -C are used to indicate the normal/fault status of unit 3 and the operating mode of AN/GRC-144(V)4. They are shown in the chart below, along with all operating conditions associated with each state. Chassis mounted relay 3A7K1 is used with relay 3A1K1 to generate these status signals. The signal at J22-A is always logic 0 (ground); this signal is connected through 3AIP1-36 to 3A1K1-A2. The coil of relay 3A7K1 is connected to 322-A (ground) and to J22-E. For C-band operating mode, the signal at J22-E is +28 Vdc and relay 3A7K1 is energized. For K-band operating mode, the signal at J22-E is 0 Vdc (open circuit) and relay 3A7K1 is deenergized. The chart on the following page indicates the logic status of the summary alarm signals and the signal routing for all operating conditions.

AN/GRC-144(V)4 Operating Mode	Unit 3 Status	Relay 3A1K1 Status	Relay 3A7K1 Status	Unit 3 Summary Alarm Signal Route	Status
K-band	Normal	Energized A1 connected to A2, A3 open	Not energized: A1 open, A2 connected to A3	Logic 0 routed from J22-A to 3A1P1-36 through 3A1K1- A1/A2 and 3A1P1-17 to J22-B Logic 1 routed from open contact 3A1K1-A3 through 3A1P1-37 and 3A7K1-A2/A3 to J22-C	Normal J22-B  logic 0  322-C  logic 1
	Fault	Not energized:  A1 open, A2 connected to  A3		Logic 1 (open) routed from 3A1K1- A1 through 3A1P1-17 to J22-8 Logic 0 from J22-A routed through 3A1P1-36, 3A1K1-A2/A3, 3A1P- 37 and 3A7K1-A2/A3 to J22C	Fault  J22-B logic 1  J22-C  logic 0
C-band	N/A	to A2, A3	Energized A1 connected J22-B open	Logic 1 routed from open contact 3A1K1-A1 through 3A1P1-17 to J22-C Logic 1 from open contact 3A7K1-A3 to J22-C	J22-B  logic 1  logic 1

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CHAPTER 3

DIRECT SUPPORT MAINTENANCE

Section I. GENERAL

3-1. Scope of Direct Support Maintenance

a. The direct support maintenance procedures contained in this chapter supplement the organizational maintenance procedures contained in TM 11-5820-695-12. Section I of this chapter identifies the test equipment and materials required to perform direct support maintenance, and lists the periodic calibration checks and tests that must be performed by direct support maintenance personnel as periodic preventive maintenance.

b. Section II contains direct support troubleshooting procedures. The procedures are a continuation of those covered at organizational level to a higher maintenance level.

c. Section III contains repair procedures for connectors with replaceable contacts or coaxial inserts; and removal and replacement procedures for piece parts and nonrepairable assemblies.

d. Section IV contains the calibration and adjustment procedures required to maintain the AN/GRC-144(V), AN/GRC144(V)3 and AN/GRC-144(V)4 at the direct support maintenance level.

e. Section V provides testing procedures to determine that repaired equipment is performing satisfactorily for return to users.

3-2. Tools, Test Equipment, and Materials Required

The following chart lists the test equipment, tools and other items required to troubleshoot, test, repair and adjust all AN/GRC-144 radio sets at the direct support maintenance level. Refer to paragraphs 3-53.1 and 3-69c for fabricated tools used to repair and adjust Converter-Multiplier CV-3633/GRC-144(V) at the direct support level.

Item	National stock No.	References
Socket, Wrench, DHEX 12 PT, 1/4-inch	5120-00235-5869.....	
Hand Ratchet, Socket Wrench , T Sliding	5120-00-221-7966.....	
Attachment, Bar Extension Solid.....	5120-00-243-7325.....	
Tool Kit, Electronic Equipment..... TK-100/G	5180-00-605-0079.....	SC 5180-9-CL-S21
Tool Kit, Electronic Equipment TK-105/G	5180-00-610-8177.....	SC 5180-91-CL-R07
Meter Calibration Facilities Kit MW-1207/GRC	6625-00-133-7863.....	
Counter Electronic, Digital Readout HP 5340A	6625-00-911-6368.....	
Multimeter TS-352B/U.....	6625-00-242-5203.....	TM 11-6625-366-15
Test Set, Radio Frequency Power AN/USM-161	6625-00-892-5541.....	TM 11-6625-498-12
Oscilloscope OS-261/V.....	6625-00-053-3112.....	
Signal Generator AN/uRM-528B.....	6625-00-965-1501.....	TM 11-6625-214-10
Test Set, Electrical Meter TS-656/U.....	6625-00-806-4485.....	TM 11-6625-226-12
Crimping Tool MS 3191-4 with Head Assembly W1	5120-00-856-3732.....	

<u>Item</u>	<u>National stock No.</u>	<u>References</u>
Crimping Tool MS 3101-4 with Head Assembly W25	5120-00-230-3771	_____
Extraction Tool MS 18278 size 20	5120-00-230-3770	_____
Extraction Tool MS 24256 R20	5120-00-079-4601	_____
Extraction Tool CET-C6B	5120-00-063-7661	_____
Insertion Tool MS 24256 A20	5120-00-079-4598	_____
Signal Generator (Ku Band) HP 626A		
Adapter, SMA(M) to N(F), Narda 57		
Adapter W/G/SMA. Narda 4609		
Attenuator, Narda 4779-3		
Test Cable N(M) to N(M) Pamona 1658-T-60		
Termination, short, Narda 4230-416		
Thermistor Mount, (C Band) HP 478A		
Thermistor Mount (Ku Band) HP 486A		
Power Meter Hewlett-Packard 432A		
Directional Coupler, Hewlett-Packard P752D		
Waveguide, Flexible Airtron AT-3-3-062-60		
Waveguide, flexible Hewlett-Packard 11503A		
Attenuator, Waveline 707-20		

### 3-3. Periodic Calibration Checks and Tests

Periodic calibration checks and tests (listed in a through c below) must be performed by direct support maintenance personnel as part of preventive maintenance. The calibration checks and tests must be performed at the interval specified, and should be scheduled concurrent with other maintenance activities. The maintenance interval specified in a through c below is based on a 40hour week. If the equipment is used for longer periods, the maintenance intervals must be adjusted to compensate for the extended operation of the equipment. Maintenance forms and records to be used and maintained on this equipment are specified in TM 38750. If trouble is encountered during performance of the calibration checks and test, refer to the troubleshooting charts (para 36b and 3-12b) for corrective action.

#### NOTE

**When performing periodic calibration checks and test for Radio Set AN/GRC-144(V)4 it is necessary to break the K-band, 14.4 to 15.0 GHZ, waveguide connection at Converter-Multiplier CV3633/GRC-144 (V) J4 ANT output. After performing test and reassembling waveguide, pressurize waveguide system in accordance with the procedures given in TM-11-5985-335-15.**

#### a. Quarterly Calibration Checks and Tests

(1) T-1054(P)/GRC-144(V) and T-1054(P)A/GRC-144(V) frequency accuracy test (para 3-71).

(2) T-1054(P)/GRC-144(V) and T-1054(P)A/GRC-144(V) output power test (para 3-72).

(3) Calibration of T-1054(P)/ GRC-144(V) and T-1054(P)A/(RC-144(V) radio test set (para 3-61).

(4) R-1467(P)/GRC-144(V) and 1R-1467(P)A/GRC-144(V) frequency accuracy test (para 3-73).

(5) R-1467(P)/GRC-144(V) and R-1467(P)A/GRC-144(V) if gain and carrier alarm test (para 3-75).

(6) AN/GRC-144(V)4 output power test at 14.4 to 15.0 6Hz and power alarm calibration (para 3-76).

(7) CV-3633/GRC-144(V) reflected power alarm threshold test and calibration (para 3-77).

(8) CV-3633/GRC-144(V) local oscillator frequency accuracy test and alarm calibration (para 3-78).

#### b. Semiannual Calibration Checks and Tests.

(1) Calibration of T-1054(P)/GRC-144(V) and T-1054(P)A/GRC-144(V) rf power metering circuit (para 3-57).

(2) Calibration of T-1054(P)/GRC-144(V) and T-1054(P)A/GRC-144(V) reflected rf power metering circuit (para 3-58).

(3) Calibration of T-1054(P)/GRC-144(V) and T-1054(P)A/GRC-144(V) frequency multiplier metering circuits (para 3-59).

(4) Calibration of T-1054(P)/GRC-144(V) traffic metering circuit (para 3-60).

(5) R-1467(P)/GRC-144(V) and R-1467(P)A/GRC-144(V) local oscillator power test (para 3-74).

(6) CV-3633/GRC-144(V) receive section conversion gain test (para 3-79).

#### c. Yearly Calibration Checks and Tests.

(1) Calibration of transmitter meter 1A15-A8M1 (para 3-55).

(2) Calibration of transmitter meter 1A16-M2 (para 3-56).

(3) Calibration of receiver meter 2A15A2-M1 (para 3-63).

(4) Calibration of R-1467(P)/GRC-144(V) and R-1467(P)A/ GRC-144(V) traffic metering circuit (para 3-64).

(5) Calibration of R-1467(P)/ GRC-144(V) and R-1467(P)A/GRC-144(V) local oscillator metering circuits (para 3-65).

(6) Calibration of ID-1708/GRC metering 3M1 (para 3-67).

## Section II. TROUBLESHOOTING

### WARNING

115 vac is present in Transmitter, Radio T-1054(P)/GRC-144(V), T1054(P)A/GRC-144(V), Receiver Radio R-1467(P)/GRC-144(V), R1467(P)A/GRC-144(V) and Converter Multiplier CV-3633/GRC144(V). Do not remove or replace parts, nor perform continuity or resistance checks while primary power is applied to the equipment.

### NOTE

For all removal and replacement of units listed in the procedures not described below, where applicable, refer to TM 11-5820-695-12.

### 3-4 General

Troubleshooting procedures described in this section provide maintenance personnel with a systematic method of isolating troubles within Transmitter, Radio T-1054(P)/GRC144(V), T-1054(P)A/GRC-144(V), Receiver Radio R-1467(P)/GRC-144(V), R-1467(P)A/GRC-144(V), and Indicator, Antenna Alignment ID-1708/GRC. The troubleshooting procedures for T-1054(P)/GRC-144(V), T1054(P)A/GRC-144(V), R-1467(P)/GRC144(V) and R-1467(P)A/GRC-144(V) consist of troubleshooting charts (para 3-6b and 3-12b); and trouble isolation checks (para 3-7 through 3-11, and 3-13 through 3-17). Troubleshooting procedures for Indicator, Antenna Alignment ID-1708/GRC are contained in paragraph 3-18 and troubleshooting procedures for Converter-Multiplier CV-3633/GRC-144(V) are contained in paragraph 3-18.1.

### 3-5. Organization of Troubleshooting Procedures

*a. General.* The first step in servicing a defective radio set is to sectionalize the fault to the

major unit responsible for abnormal operation. The second step is to localize the fault to a group of components or circuits within the faulty unit. After the fault has been localized, it must be isolated to a single component, wire, or piece part that is defective.

*b. Sectionalization.* Use the checks listed in (1) through (3) below to sectionalize the fault in all AN/GRC-144(V) Radio Sets to a major unit. The Checks are arranged to reduce unnecessary work and aid in tracing the fault to the major unit responsible for abnormal operations.

(1) Visual inspection. Most faults in Radio Set AN/GRC-144(V) can be sectionalized to a major unit by observing the status and alarm indicators on Transmitter, Radio T-1054(P)/GRC-144(V), T-1054(P)A/GRC-144(V), Receiver, Radio R-1467(P)/GRC-144(V), R-1467(P)A/GRC-144(V) and CV-3633/CGRC-144(V).

(2) Operational checks. When visual inspection fails to sectionalize a fault in Radio Set AN/GRC-144 to a major unit, use the operational -checks provided in the monthly preventive maintenance checks and services chart in TM 115820495-12 to sectionalize the fault.

(3) Interunit cable checks. When a fault cannot be sectionalized to a major unit using the sectionalization techniques listed above, check the interconnecting cables between Transmitter, Radio T-1054(P)/GRC--144(V), T-1054(P) A/GRC-144(V), Receiver Radio R-1467(P) /GRC-144(V), R-1467(P)A/GRC-144(V) and Converter-Multiplier CV-3633/GRC144(V). Interconnection cabling diagrams in TM 11-5820-695-12 provide routing information for performing the interunit cable checks.

*c. Localization.* After the fault has been sectionalized to a major unit, it is necessary to localize the fault to a group of components or circuits within the faulty unit. The localization procedures consist of troubleshooting charts (para 3-6b, 3-12b, and 3-18.1b) that will aid the repairman in localizing faults in AN/GRC-144 Radio Sets. In many instances the localization proce-



dures will isolate the fault to a replaceable component, wire or piece part. If not, the localization procedure will reference the isolation procedure to be used.

*d. Isolation.* When use of the localization procedures fails to isolate the fault to a replaceable component, wire, or piece part; continuity and resistance checks must be made to isolate the fault. The trouble isolation checks (para 3-7 through 3-11 and 3-13 through 3-17 and 3-18.2 through 3-18.4) provide point-to-point continuity and resistance checks to isolate defective wiring or circuit elements within Transmitter, Radio T-1054(P)/ GRC-144(), T-1054(P)A/GRC-144(V), Receiver Radio R-1467(P)/GRC-144V, R-1467(P)A/GRC-144 (V) and Converter-Multiplier CV-3633/GRC144(V). The trouble isolation checks are referenced in the troubleshooting charts (para 3-6b, 2-12b and 3-18.lb) and specify those sections of the trouble isolation checks that must be performed. A resistance and capacitor color code diagram (fig. 5-1) is provided to aid maintenance personnel in determining the exact value, voltage rating, and tolerance of capacitors and resistors.

**3-6. Transmitter, Radio T-1054(P)/GRC-144(V) and T-1054(P)A/GRC-144(V) Troubleshooting Chart**

**WARNING**

115 vac is present in Transmitter, Radio T-1054(P)/GRC-144(V). Do not remove or replace parts nor perform continuity or resistance checks while primary power is applied to AN/GRC-144(V) Radio Sets.

a. Use of the Chart. The T-1054(P)/ GRC-144(V) and T-1054(P)A/GRC-144(V) troubleshooting chart (b below) supplements the operational checks and corrective measures contained in TM 11-5820-695-12. If the operational checks and corrective measures in TM 11-5820695-12 fail to correct the trouble or indicates that higher category maintenance is required, apply the corrective action in the chart below. To use the chart, read down the Symptom column of the troubleshooting chart until the abnormal symptom or condition is found. Perform the corrective actions indicated in the chart until the abnormal symptom or condition is corrected. Figures 3-1 through 3-16 are parts location diagrams which will aid the maintenance man in locating parts.

b. T-1054(P)/GRC-144(V) and T-1054 (P)A/GRC-144(V) Troubleshooting Chart.

**NOTE**

Unless otherwise specified the troubleshooting chart below pertains to Transmitter, Radios T-1054(P)/ (C-144(V) T-1054(P)A/GRC-144(V). Refer to figure 5-15 for T-1054(P)/GRC-144(V) interconnection diagram and refer to figure 5-15.1 for the T-1054(P)A/ GRC-144(V) interconnection diagram. For Radio Sets AN/GRC-144(V)3 and AN/GRC-144(V)4, when the probable trouble or corrective action columns refer to digital data modem chassis 1A12 (para 3-29) substitute digital data combiner 1A12 chassis (para 3-29.1).

<i>Item No.</i>	<i>Symptom</i>	<i>Probable trouble</i>	<i>Corrective action</i>
1	5 AMP SLO-BLO fuse blows when replaced.	a. Defective component or wire in primary power distribution circuits.	a. Remove power supply 1A1 (para 3-22a) and electrical frequency synthesizer 1A14 (para 331a) from electrical equipment cabinet 1A15. Insert replacement fuse and then set POWER ON/OFF switch on meter panel assembly 1A15A8 to ON. If replacement fuse blows, proceed to step d below. Otherwise, proceed to steps b and c below to isolate the fault.

Item No.	Symptom	Probable trouble	Corrective action
		<ul style="list-style-type: none"> <li>b. Defective component or wire in power supply chassis assembly 1A1A13.</li> <li>c. Electrical equipment chassis 1A14A10 defective.</li> <li>d. Defective wiring in primary power distribution circuits.</li> </ul>	<ul style="list-style-type: none"> <li>b. Perform the power supply chassis assembly 1A1A13 checks (para 3-9c, sections 1 through 11).</li> <li>c. Replace electrical equipment chassis 1A14A10 (para 3-31).</li> <li>d. Perform the T-1054/GRC-144 primary power distribution checks (par 8-7c, sections 2, 4, and 5).</li> </ul>
		e. Vane axial fan IA1SBi defective-----	e. Remove vane axial fan 1A16B1 (para 3-28) and use the TE-852 B/U to check its resistance as follows: T1 to T4 should be $500 \pm 100$ ohms, and T1 to T5 should be $ze \pm 100$ ohms,
		f. Capacitor 1Ar6CI defective-----	f. Check capacitor 1A1C51 (para 3-24) by substitution.
		g. Power transformer 1A1SA10T1-----	g. Check power transformer 1A16A10T (para 8) by substitution.
2	All indicators on meter panel assembly 1A16AS not lighted.	a. 5 AMP SLO-BLO fuse 1A1SASF1-----	a. Check 5 AMP SLO-BLO neon fuse indicator on meter panel assembly 1A16A8. If lighted, refer to item No. 1 in this chart.
		b. Same as item No. 7 in this chart -----	b. Check indicators on power supply 1A. If any indicator not lighted, refer to item No. 7 in this chart
3	SYNTH OVEN indicator not lighted.	a. Defective wiring-----	a. Remove power from T-10S4/GR-144 (para 3-2a) and check for continuity between: pin 2 of 1A15A6XDS9 (fig. 5-15) and pin 1 of connector 1A15W27-XA14; pin 1 of 1A15ASXDS9 and pin G of 1A16A8XDS10; and pin 8 of 1A16A8XDS9 and the E1 CABINET GROUND lug on top of T-1054/GRC-144.
		b. Indicator assembly IAiSASXDS9 defective.	b. Replace indicator assembly 1A15A8XDS9 (fig. 3-4).
		c. Electrical equipment chassis 1A11A10 defective.	c. Replace electrical equipment chassis 1A14A10 (para 3-31).
4	5V and 28V indicators on electrical frequency synthesizer 1A14 not lighted.	a. Defective wiring-----	a. Remove electrical frequency synthesizer 1A14 (para 3-31) and check for continuity between pins 5 and 6 of connector 1A15W27XA14 (fig. 5-1,5).
		b. Electrical equipment chassis 1A14A10 defective.	b. Replace electrical equipment chassis 1A14A10 (para 3-31).
5	Any fault indicator lamp on electrical frequency synthesizer IA14 lighted.	Electrical equipment chassis 1A14A10 defective.	Replace electrical equipment chassis 1A14A10 (para 341).
6	Power on and vane axial fan 1A1SB1 not operating.	a. Vane axial fan 1A1SB1 defective-----	a. Remove vane axial fan 1A16B1 (para 3-23) and use the TS-352 B/U to check its resistance as follows: T1 to T4 should be $500 \pm 100$ ohms, and T1 to T5 should be $800 \pm 100$ ohms.
		b. Capacitor 1A15C1 defective-----	b. Check capacitor 1A15C1 (para 3-24) by substitution.

Item No.	Symptom	Probable trouble	Corrective action
7	Any indicator lamp on power supply 1A1 not lighted.	<ul style="list-style-type: none"> <li>c. Defective wiring primary power distribution circuits.</li> <li>a. Power Supply, chassis assembly 1A1A13 defective.</li> <li>b. Defective component or wire in dc power distribution circuits.</li> <li>c. Defective component or wire in primary power distribution circuits</li> </ul>	<ul style="list-style-type: none"> <li>c. Use the -1064/GRC-144 inter-connecting diagram (fig. 5-15) and T8562 B/U to check continuity of wiring between vane axial fan 1A1B1 and POWER ON/OFF switch 1A15A883.</li> <li>a. Check power supply chassis assembly 1A1A13 by substitution (para 8-22). If indicator lights after 1A1A18 is replaced, use the power supply chassis assembly 1A1A18 checks (para 89) to isolate the trouble.</li> <li>b. Perform the T-1054/GRC-144 dc Power distribution checks (para 3-8c, sections 1 through 11).</li> <li>c. Perform the T-1054/GRC-144 primary power distribution checks (para 87c, sections 1 through 5).</li> </ul>
8	Out of color band meter indication obtained at any of the component test points (TM 11-5820-695-12).	Same as item No. 7 in this chart-----	Perform the corrective action given for Item No. 7 in this chart.
9	Zero meter indication obtained when meter selector switch is placed in any position.	<ul style="list-style-type: none"> <li>a. Defective wiring on meter panel assy 1A15A8 tad T8-52 B/U to check wiring bet-, meter selector switch</li> <li>b. Meter 1A15ASM1 defective -----</li> <li>c. Meter selector switch 1A15ASS4 defective.</li> </ul>	<ul style="list-style-type: none"> <li>a. Use the T-1054/GRC-144 inter-connecting diagram (fig. 5-15) 1A15A8S4 and meter 1A15A8M1.</li> <li>b. Use the transmitter meter 1A1A8M1 calibration procedure (para 6) to check meter 1A16A8M1.</li> <li>c. Replace meter selector switch 1A16A8S4 (fig. 84).</li> </ul>
10	Orderwire channel inoperative (cannot originate a orderwire call).	<ul style="list-style-type: none"> <li>a. Defective wiring in electrical equipment cabinet 1A15.</li> <li>b. Orderwire chassis 1A18A7 defective</li> </ul>	<ul style="list-style-type: none"> <li>a. Perform the electrical equipment cabinet 1A15 checks (para 3-11c, sections 6 and 7).</li> <li>b. Replace orderwire chassis 1A18A7 (para -20).</li> </ul>
11	1600 Hz ring signal not generated when RING pushbutton is depressed	<ul style="list-style-type: none"> <li>a. Defective wiring in electrical equipment cabinet A.</li> <li>b. RING pushbutton switch 1A16A8S1 defective</li> <li>c. Orderwire chassis 1A13A7 defective.</li> </ul>	<ul style="list-style-type: none"> <li>c. Perform the electrical equipment cabinet 1A5 checks (paras 3-11, section 7 (steps ad through ag)).</li> <li>b. Check RING pushbutton switch 1A15A8S1 by substitution (fig. 84).</li> <li>c. Replace orderwire chassis 1A18A7 (para 3-30).</li> </ul>
12	Audible alarm signal cannot be silenced by depressing the RESET pushbutton.	<ul style="list-style-type: none"> <li>a. Defective wiring in electrical equipment cabinet 1A1.</li> <li>b. Orderwire chassis 1A18A7 defective</li> </ul>	<ul style="list-style-type: none"> <li>b. Perform the electrical equipment cabinet 1A16 checks (para 3-11c, section 1 (step x) and section 7 (step l and m)).</li> <li>b. Replace orderwire chassis 1A18A7 (Para 3-30).</li> </ul>
13	Any indicator lamp on digital data modem 1A12 not lighted.	<ul style="list-style-type: none"> <li>a. Defective wiring in electrical equipment cabinet 1A15.</li> <li>b. Digital data modem chassis 1A12A12 defective.</li> </ul>	<ul style="list-style-type: none"> <li>a. Perform the electrical equipment cabinet 1A15 checks (para 3-11c sections 4 and 5).</li> <li>b. Replace digital data modem chassis 1A12A12 (para 8-29).</li> </ul>

<i>Item No.</i>	<i>Symptom</i>	<i>Probable trouble</i>	<i>Corrective action</i>
14	Speaker output low-----	<p>a. Defective component or wire in electrical equipment cabinet 1A16.</p> <p>b. Speaker 1A15A8LS1 defective-----</p> <p>c. Orderwire chassis 1A13A7 defective.</p>	<p>a. Perform the electrical equipment cabinet 1A16 checks (para 3-11, section 7 (step i, J, and k)).</p> <p>b. Check ea- r 1A15A8LS1 by substitution (fig. 3-4).</p> <p>c. Replace orderwire chassis 1A13A7 (para 3-30).</p>
15	Both the green and red lamps of any status or alarm indicator lighted	Defective wiring between indicator and its associated lamp driver.	Use the T-1064/GRC-144 interconnecting diagram (fig. 5-15) and TS-862 B/U to isolate the defective wiring.
16	RING indicator does not light amber when 1600 Hz ring signal is present.	<p>a. Defective wiring in electrical equipment 1A16.</p> <p>b. Orderwire chassis 1A18A7 defective</p>	<p>a. Perform the electrical equipment cabinet 1A15 checks (para 3-11c, section 8 (step u)).</p> <p>b. Replace orderwire chassis 1A18A7 (para 3-30).</p>
17	CNTRL ALARM indicator lighted red (all other alarm indicators lighted green).	<p>a. Defective wiring in electrical equipment cabinet 1A15.</p> <p>b. Orderwire chassis 1A18A7 defective</p>	<p>a. Remove the orderwire assembly 1A13 (para 3-30) and use the TS-.52 B/U to check for eon- tinity between pins 22, 23, and 25 of connector A165W27XA13B and CABINET GROUND lug E1 (fig. 6-15). If continuity is obtained, perform the electrical equipment cabinet 1A16 checks (para 3-11c, section 7 (steps p, q, and r)).</p> <p>b. Replace orderwire chassis 1A1A7 (para 3-0).</p>
18	TRAF indicator lighted red-----	<p>a. Defective wiring in plate assembly 1A16</p> <p>b. Defective wiring in electrical equipment cabinet 1A1.</p> <p>c. Digital data modem chassis 1A12A12 defective.</p>	<p>a. Perform the plate assembly 1A16 checks (para -10c sections 2, 3, 5, and 6).</p> <p>b. Perform the electrical equipment cabinet 1A16 cheeks (para 3-11c, sections 4 and 5).</p> <p>e. Replace digital data modem chassis 1A12A12 (para 8-29).</p>
19	RF POWER indicator lighted red.	<p>a. Coaxial cable 1A16W22 defective-----</p> <p>b. Transmitter frequency mixer stage 1A9 defective.</p> <p>c. Radio frequency bandpass filter 1FL3 defective</p> <p>d. Radio frequency low pass filter 1FL4 defective.</p> <p>e. Connector adapter 1CP4 or direc- tional coupler IDC1 defective.</p>	<p>a. Turn meter selector switch on meter panel assembly 1A15A8 to 3RD MULT (LOCAL OSC). If meter indication is not in the yellow band, proceed to step f below. If meter indication is in the yellow band, remove alarm- monitor 1A5 and perform the plate assembly 1A16 checks (para 8-10a, section 4, (step o)).</p> <p>b. Check transmitter frequency mixer stage 1A9 by substitution (TM 11-5820-695-12).</p> <p>c. Check radio frequency bandpass filter 1FL8 (para 3-36) by substitution.</p> <p>d. Check radio frequency low pass filter 1FIA by substitution (para 3-36).</p> <p>e. Check connector adapter 1CP4 and directional coupler 1DC1 by substitution (para 336).</p>

Item No.	Symptom	Probable trouble	Corrective action
20	SYNTH LOCK indicator lighted red.	<p>f. Transmitter frequency mixer stage 1A9 defective.</p> <p>g. Transmitter frequency multiplier group 1A10 defective.</p> <p>h. Defective wiring in plate assembly 1A16.</p> <p>t. Coaxial cable 1A15W16 defective-----i. (fig. 3-13) by substitution.</p> <p>j. Coaxial circulator 1HY,1 defective-----j.</p> <p>k. Defective wiring in electrical equipment cabinet 1A15.</p> <p>l. Electrical equipment chassis 1A14A10 defective.</p> <p>a. Electrical equipment chassis 1A14A10 defective.</p> <p>b. Defective wiring -----b.</p>	<p>f. Turn meter selector switch to ZND MULT. If meter indication is not in yellow band, proceed to step q below. If meter indication is in yellow band, check 1A9 by substitution.</p> <p>g. Turn meter selector switch to AMPL-MULT. If meter indication is not in yellow band, proceed to step h below. If meter indication is in yellow band, check transmitter frequency multiplier group 1A10 by substitution (TM 11-5820-696-12).</p> <p>h. Turn meter selector switch to SYNTHESIZER. If meter indication is not in yellow band, proceed to step k below. If meter indication is in yellow band, perform the plate assembly 1A16 checks (para -10c, section 7).</p> <p>i. Check coaxial cable 1A15W16</p> <p>j. Check coaxial circulator 1HY1 by substitution (para -28).</p> <p>k. Perform the electrical equipment cabinet 1A15 checks (para 3-31, section 8).</p> <p>l. Replace electrical equipment chassis 1A14A10 (para 3-31).</p> <p>a. Check electrical equipment chassis 1A14A10 by substitution (para 3-S1).</p> <p>b. Remove electrical frequency synthesizer 1A14 (para 38-1) and alarm monitor 1A5, and check for continuity between pin 7 of connector 1A16W27XA14 and pin 17 of connector 1A16W25-XASB (fig. 5-15). Also check resistance between pin 8 and 9 of connector 1A16W26XA5A. Resistance should be greater than 10 ohms.</p>
21	REFL RF POWER indicator lighted red.	<p>a. Coaxial cable 1W25 defective-----a.</p> <p>b. Directional coupler 1DC1 defective.</p> <p>c. Duplexer CU-1891/GRC defective-----c.</p>	<p>a. Check coaxial cable 1W26 (fig. 3-13) by substitution.</p> <p>b. Check directional coupler 1DC1 by substitution (para 3-36).</p> <p>c. Check Duplexer CU-1891/GRC by substitution.</p>
22	CABLE TO RADIO MODEM indicator lighted red. (Applicable to standard cable terminal operation only).	<p>d. Switch, Waveguide SA-1679/GRC defective</p> <p>a. Defective wiring in electrical equipment cabinet 1A16.</p> <p>b. Digital data modem chassis LA12A12 defective.</p>	<p>d. Check Switch, Waveguide SA-1679/GRC by substitution.</p> <p>a. Perform the electrical equipment cabinet 1A16 checks (para 311c, sections 4 and 5).</p> <p>b. Replace digital data modem chassis 1A12A12 (par 3-29).</p>

<i>Item No.</i>	<i>Symptom</i>	<i>Probable trouble</i>	<i>Corrective action</i>
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**NOTE**

**For Radio Sets AN/GRC144(V)3 and AN/GRC-144 (V)4, the radio patch panel is not used for radio repeater operation and plug 1A15W27P2 is always patched into jack 1A15W27J13.**

23	RADIO TO CABLE MODEM alarm indicator lighted red. (Applicable to standard cable terminal and standard radio repeater operation only).	Same as item No. 22 in this chart-----	Perform the corrective action given in item No. 22 in this chart.
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**NOTE**

**Item 24 is not applicable for AN/GRC-144(V)3 and (V)4 Radio Sets.**

**Change 6 3-7**

<i>Item No.</i>	<i>Symptom</i>	<i>Probable trouble</i>	<i>Corrective action</i>
24	RADIO REPEATER OPERATION indicator not lighted and standard radio repeater operation is being used.	<p>a. Defective wiring in electrical equipment cabinet 1A15.</p> <p>b. Indicator assembly 1A15XDSZ defective.</p>	<p>a. Use the T-10 U4/OFR-144 interconnecting diagram (fig. 5-16) and TS-352 B/U to check continuity of wiring between pin 2 of connector 1A15W27XA1B and indicator assembly 1A1XDS28.</p> <p>b. Replace indicator assembly 1A16XDS2s (fig. 5-15).</p>
25	CABLE TERMINAL OPERATION indicator not lighted and standard cable terminal operation is being used.	<p>a. Defective wiring in electrical equipment cabinet 1A15.</p> <p>b. Indicator assembly 1A16XDS22 defective.</p>	<p>a. Use the T-1014/GR-144 interconnecting diagram (fig. 615) and TS452 B/U to check continuity of wiring between pin 2 of connector 1A15WT7XA1B and indicator assembly 1A15XDS22.</p> <p>b. Replace indicator assembly 1A16XDS22 (fig. 3-5).</p>
26	Meter indication for MODULATOR OUTPUT, FREQ CONTROL CTR FREQ, or FREQ CONTROL OUTPUT meter selector switch position not in its color band.	Defective wiring or component in plate assembly 1A16. and 6).	Perform the plate assembly 1A16 checks (para 3-10c, sections 5
27	Meter indication for TRAFFIC meter selector switch position not in orange band.	<p>a. Meter calibration required -----</p> <p>b. Defective wiring in plate assembly 1A16.</p>	<p>a. Calibrate the T-1054/GRC-144 traffic metering circuit (para 3-60).</p> <p>b. Perform the corrective action given for item No. 18 in this chart.</p>
28	Meter indication for SYNTHESIZER meter selector switch position not in yellow band.	<p>a. Defective wiring in electrical equipment cabinet LA11.</p> <p>b. Electrical equipment chassis 1A14A10 defective.</p>	<p>a. Perform the electrical equipment Cabinet 1A1S checks (para 3-11c, section 8).</p> <p>b. Replace electrical equipment chassis 1A14A10 (para 3-1).</p>
29	Meter indication for AMPI, MULT meter selector switch position in yellow band.	<p>a. Meter calibration required -----</p> <p>b. Defective wiring in plate assembly 1A16.</p> <p>c. Coaxial cable 1A16W16 defective -----</p> <p>d. Coaxial circulator 1HY1 defective -----</p>	<p>a. Turn meter selector switch to SYNTHESIZER. If meter indication is not in yellow band, perform the corrective action given for item No. 28 in this chart. If meter indication is in yellow band, calibrate the AMPILMULT metering circuit (para 3-849).</p> <p>b. Perform the plate assembly 1A16 checks (para 3-10c, section 7).</p> <p>c. Check coaxial cable 1A1SW16 (fig. 3-13) by substitution.</p> <p>d. Replace coaxial circulator 1HY1 (para 3-28).</p>
30	Meter indication for 2 <sup>ND</sup> MULT meter selector switch position not in yellow band.	<p>a. Meter calibration required -----</p> <p>b. Coaxial circulator 1HY1 defective -----</p>	<p>a. Turn meter selector switch to AMPI-PLMULT. If meter indication is not in yellow band, perform the corrective action given for item No. 29 in this chart. If meter indication is in the yellow band, calibrate the 2ND MULT metering circuit (para 3-59).</p> <p>b. Replace coaxial circulator 1HY1 (para 3-28).</p>

<i>Item No.</i>	<i>Symptom</i>	<i>Probable trouble</i>	<i>Corrective action</i>
31	Meter indication for 3 <sup>RD</sup> MULT (LOCAL OSC) meter selector switch position not in yellow band.	a. Meter calibration required-----  b. Coaxial circulator 1A10HY1 defective.	a. Turn meter selector switch to 2ND MULT. If meter indication is not in yellow band, perform the corrective action given for item No. 30 in this chart. If meter indication is in yellow band, calibrate the 3RD MULT (LOCAL OSC) metering circuit (para 3-59).  b. Replace coaxial circulator 1A10HY1 (para 3-27)
32	Meter indication for RF POWER meter selector switch position not in yellow band.	a. Meter calibration required-----  b. Same as item No. 19 in this chart----	a. Calibrate the T-1054(P)/GRC-144(V) rf power metering circuit (para 3-57).  b. Perform the corrective action given in item No. 19 in this chart.
33	Meter indication for REFL RF POWER meter selector switch position is greater than 20.	a. Meter calibration required-----  b. Defective wiring in plate assembly 1A16.	a. Calibrate the T-1054(P)/GRC -144(V) reflected rf power metering circuit (para 3-58).  b. Perform the corrective action given for item No. 21 in this chart.
34	Meter indication for OW TEST meter selector switch position not 100 ± 10.	a. Defective wiring in plate assembly 1A16. b. Defective wiring in electrical equipment cabinet 1A15.  c. Digital data modem chassis 1A12A12 defective.	a. Perform the plate assembly 1A16 checks (para 3-10c, section 2). b. Perform the electrical equipment cabinet 1A15 checks (para 3-11c, sections 4, 5, and 7).  c. If standard cable terminal operation is being used, replace digital data modem chassis 1A12A12 (para 3-29).
35	Modulator frequency not 50 MHz +20 kHz as determined by test (para 3-71).	a. Modulator frequency adjustment required. b. Component 1A8 or 1A7 defective	a. Perform the modulator frequency adjustment (para 3-62). b. Check components 1A8 and 1A7 by substitution (TM 11-5820-695-12).
36	Electrical frequency synthesizer 1A14 frequency error greater than 3 kHz as determined by test (para 3-71).	a. Defective component in electrical frequency synthesizer 1A14.  b. Electrical equipment chassis 1A14A10 defective.	a. One at a time, replace each component (1A14A1 through 1A14A7) in electrical frequency synthesizer 1A14 (TM 11-5820-695-12).  b. Replace electrical equipment chassis 1A14A10 (para 3-31).

**CHANGE 6 3-8.1/(3-8.2 blank)**



**NOTE**

**For Radio Sets AN/GRC-144(V)3 and AN/GRC-144(V)4 check Switch, Waveguide SC-D-958093-001 (AN/TRC-175) K band, SC-D-958093-002 (AN/TRC-138) SRWBR receiver, or SC-D-958093-003 (AN/TRC-138) SRWBR transmitter.**

- |    |  |   |   |
|----|--|---|---|
| 37 | T-1054(P)/GRC-144(V) rf output power less than 150 milliwatts as determined by test (para 3-72). | <ul style="list-style-type: none"> <li>a. Same as item No. 19 in this chart</li> <li>b. Switch, Waveguide SA-1679/GRC defective.</li> <li>c. Adapter, Waveguide UG-1883/GRC defective.</li> </ul> | <ul style="list-style-type: none"> <li>a. Perform the corrective action for item No. 19 in this chart.</li> <li>b. Check Switch, Waveguide SA-1679/GRC by substitution.</li> <li>c. Check Adapter, Waveguide UG-1883/GRC by substitution.</li> </ul>  |
| 38 | Cannot calibrate the T-1054(P)/GRC-144(V) traffic metering circuit (para 3-60).                  | Defective component or wire in metering circuit.  | <p>Remove alarm monitor 1A5 (TM 11-5820-695-12) and check resistance between pin 12 of connector 1A16W25XA6B and the E1 CABINET GROUND lug on top of 1A15 (fig. 5-15). Note that resistance varies smoothly from zero to 5,000 ohms as potentiometer 1A15A8R7 (fig. 3-4) is varied from one extreme to the other. Make the same resistance check between pin 17 of 1A15A8S4B and pin 12 of connector 1A16W25XASB.</p> |

<i>Item No.</i>	<i>Symptom</i>	<i>Probable trouble</i>	<i>Corrective actions</i>
39	Cannot calibrate the T-1054/GRC-144 rf power metering circuit (para 3-67).	<p>a. Defective wiring</p> <p>b. Defective component or wire in metering circuit.</p> <p>c. Directional coupler 1DC1 defective</p>	<p>a. Remove alarm monitor 1A6 (TM 11-820695-12) and check for continuity between pin 2 of Connector 1A16W26XA6B and the center conductor of coaxial cable 1A16W22P1 (fig. 5-15).</p> <p>b. Check resistance between pin 4 of connector 1A16W25XA6B and the E1 CABINET GROUND lug on top of 1A1 (fig. 5-15). Note that resistance varies smoothly from zero to 5600 ohms as potentiometer 1A15-A8R6 (fig. 3-4) is varied from one extreme to the other. Make the same resistance check between pin 4 of connector 1A16W25XACB and pin 27 of 1A16A8S4B.</p> <p>c. Check directional coupler 1DC1 by substitution (para 3-36).</p>
40	Cannot calibrate the T-1054/GRC-144 reflected rf power metering circuit (para 3-58).	<p>a. Defective wiring</p> <p>b. Defective component or wire in metering circuit.</p> <p>c. Directional coupler 1DC1 defective.</p>	<p>a. Remove alarm monitor 1A6 (TM 11-5820-695-12) and check for continuity between pin 14 of -connector 1A16W25XA5B and the center conductor of coaxial cable 1A16W23P1 (fig 5-15).</p> <p>b. Check resistance between pin 15 of connector 1A16W25XA5B and the E1 CABINET GROUND lug on top of 1A1 (fig. 5-15). Note that resistance varies smoothly from zero to 5,000 ohms as potentiometer 1A15A-8R5 (fig. 3-4) is varied from one extreme to the other. Make the same resistance check between pin 16 of connector 1A16W25XASB and pin 29 of 1A15A8S4B.</p> <p>c. Check directional coupler 1DC1 by substitution (para 3-36).</p>
41	Cannot calibrate the 3RD MULT (LOCAL OSC) section of the T-1054/GRC-144 frequency multiplier metering circuits (para 3-59).	<p>a. Defective wiring</p> <p>b. Defective component or wire in metering circuit.</p> <p>c. Coaxial circulator 1A9HY1 defective.</p>	<p>a. Check for continuity between terminal U of connector 1A15W27J1 and terminal 1 of potentiometer 1A15A8R2 (fig. 5-15).</p> <p>b. Check resistance between terminal 1 of potentiometer 1A15A8R2 and pin 26 of 1A15A8S4A (fig. 5-15). Note that resistance varies smoothly from zero to 50,000 ohms as potentiometer 1A15A8R2 (fig. 3-4) is varied from one extreme to the other.</p> <p>c. Check coaxial circulator 1A9HY1 by substitution (para 3-26).</p>
42	Cannot calibrate the 2ND MULT section of the T-1054/GRC-144 frequency multiplier metering circuits (para 3-59).	<p>a. Defective wiring</p> <p>b. Defective component or wire in metering circuit.</p>	<p>a. Check for continuity between terminal T of connector 1A15W27J1 and terminal 1 of potentiometer 1A15A8R3 (fig. 5-15).</p> <p>b. Check resistance between terminal 1 of potentiometer 1A15A8R3</p>

<i>Item No.</i>	<i>Symptom</i>	<i>Probable trouble</i>	<i>Corrective actions</i>
			and pin 28 of 1A15A8S4A (fig 5-15)..Note that residence varies smoothly from zero to 50,000 ohms as potentiometer 1A15A8R3 (fig. 3-4) is varied from one extreme to the other.
43	Cannot calibrate the AMPL-MULT section of the T-1054 (P)/GRC-144(V) frequency multiplier metering circuit (para S9).	<ul style="list-style-type: none"> <li>c. Coaxial circulator 1A10HY1 defective.</li> <li>a. Defective wiring</li> <li>b. Defective component or wire in metering circuit.</li> </ul>	<ul style="list-style-type: none"> <li>c. Check circulator 1A10HY1 by substitution (para 3-27).</li> <li>a. Check for continuity between terminal S of connector 1A156W27J1 and terminal 1 of potentiometer 1A165A8R (fig. 5-16).</li> <li>b. Check resistance between terminal 1 of potentiometer 1A15A8R4 and pin 21 of 1A16ABS4A (fig. 5-15). Note that resistance varies monthly from zero to 50,000 ohms as potentiometer 1A15A8R4 (fig. 3-4) is varied from one extreme to the other.</li> </ul>
44	Cannot calibrate the T-1054(P)/GRC-1 44(V) radio test set (para-61).	<ul style="list-style-type: none"> <li>a. 100 MHz radio frequency oscillator 1A2 defective.</li> <li>b. Coaxial cable 1A16W24 defective</li> <li>c. Crystal mixer 1A16Z1 defective</li> <li>d. Variable attenuator 1A16A1 defective.</li> <li>e. Coaxial cable 1A15W26 defective</li> <li>f. Coaxial cable between T-1 054(P)/GRC-144(V) teat output and coupler, Directional CU-1890, GRC defective.</li> <li>g. Coupler, Directional CU-1890/GRC defective.</li> </ul>	<ul style="list-style-type: none"> <li>a. Check 100 MHz radio frequency oscillator 1A2 by substitution.</li> <li>b. Check continuity of coaxial cable 1A16W24 (fig. S-18).</li> <li>c. Check crystal mixer 1A16Z1 by substitution (para S-6).</li> <li>d. Check variable attenuator 1A16AT1 by substitution (para 8--5).</li> <li>e. Check coaxial cable 1A15W6 by substitution (fig. 18).</li> <li>f. Check coaxial cable by substitution.</li> <li>g. Check Coupler, Directional CU-18S9/GRC by substitution.</li> </ul>

**NOTE**

**Step 45 applies to AN/GRC-144(V) Radio Set only. For Radio Sets AN/GRC-144(V)3 and AN/GRC-144(V)4, see step 46.**

46	Cable loop back test (TM 11-682(}312) indicates that AN/GRC-44 is faulty.	<ul style="list-style-type: none"> <li>a. Coaxial cable 1A15W1 or 1A15W2 defective.</li> <li>b. Digital data modem chassis 1A12A12 defective.</li> </ul>	<ul style="list-style-type: none"> <li>a. Check coaxial cables 1A15W1 and 1A15W2 (fig. -1S) by substitution, using an external hookup.</li> <li>b. Check digital data modem ca 1A1A12 by substitution (para 3-29).</li> </ul>
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<i>Item No.</i>	<i>Symptom</i>	<i>Probable trouble</i>	<i>Corrective actions</i>
46	Cable loopback test (TM 11-5820-695-12) indicates that Radio Set AN/GRC-144(V)3 of AN/GRC-144(V)4 is faulty.	<ul style="list-style-type: none"> <li>a. Coaxial cable 1A15W7 or 1A15W4.</li> <li>b. Digital data combiner 1A12 chassis defective.</li> </ul>	<ul style="list-style-type: none"> <li>a. Check coaxial Cables 1A15W7 and 1A15W4 (fig. 3-13) by substitution, using an external hookup.</li> <li>b. Check digital data combiner 1A12 chassis by substitution.</li> </ul>

3-7. Isolating Troubles in T-1054(P)/ GRC-144(V) Primary Power Distribution Circuits

(3) Remove composite assembly 1A13/ 1A14 (para 3-30).

**WARNING**

b. *Procedure.*

**115 vac is present in T-1054(P)/ GRC-144(V). Do not perform any of the continuity or resistance checks given in this paragraph while the equipment is connected to the primary power source.**

(1) Refer to the chart (c below) and connect the multimeter leads between the two pins referenced in the troubleshooting chart (para 3-6) by section and step number. If the troubleshooting chart indicates a section but does not give a step number, perform all of the steps given in that section starting with step a.

a. *Preparation of T-1054(P)/GRC-144(V).*

(2) Observe that multimeter indication is within the tolerance specified in the chart for each step. If it is not, refer to the T-1054(P)/GRC-144(V) interconnecting diagram (fig. 5-15 or 5-15.1) to determine whether the fault is defective wiring or a defective circuit element.

(1) Remove power supply 1A1 (para 3-22).

(2) Remove switch 1A15A8S3 protective cover (fig. 3-4) by removing the two nuts and screw that secure it to meter panel assembly 1A15A8.

c. T-1054(P)/GRC-144(V) Primary Power Distribution Checks Chart.

Section	Step	Connect multimeter leads between pin and pin		Multimeter indication (ohms)
1	a	1A15A6J18-A	1A15AS3-4	Less than 1
	b	-B	1A15E1	Zero
	c	-C	1A15A8S3-2	Less than 1
2	a	1A15A8S3-1	1A15W12XA14-6	Zero
	b	-1	-10	Zero
	c	-3	-5	Zero
	d	-3	-9	Zero
3		1A15A8S3-1	1A16ASS	Less than 2
4	a	1A16A10W1XA1A-1	1A15A10W1XA1X-20	Less than 1
	b	-3	-22	Less than 1
	c	-4	-25	Less than 1
	d	-7	-26	Less than 1
	e	-9	-28	Less than 1
	f	-10	-29	Less than 1
	g	-11	-30	Less than 1
	h	12	-31	Less than 1
	i	-14	-33	Less than 1
	j	-16	-35	Less than 1
	k	-18	-37	Less than 1
5	l	-19	1A16E1	Zero
	a	1A15A8S3-1	1A16B1-T1	Zero
	b	-1	1A16J20-C	Zero
	c	13	1A15B1-T4	Zero
	d	-3	1A15J20-A	Zero

3-8. Isolating Troubles in T-1054(P)/ GRC-144(V) Primary Power Distribution Circuits.

**WARNING**

**115 vac is present in T-1054(P) A/GRC-144(V) Do not perform any of the continuity or resistance checks given in this paragraph while the equipment is connected to the primary power source.**

a. *Preparation of T-1054(P)/GRC-144(V)*

(1) Remove power supply 1A1 (para 3-22).

(2) Remove orderwire assembly 1A13/ 1A14 (pare 3-30) and digital data modem 1A12 or digital data combiner 1A12 (para 3-29 or 3-29.1).

(3) Disconnect plug 1A16W25P1 (fig. 3-2) from jack 1A15W27J1 (fig. 3-8). Disconnect the equipment interconnection cable from jack 1A15W27J4 (fig. 3-7).

b. *Procedure.*

(1) Refer to the chart (c below). Connect the multimeter leads between the two pins listed in the steps of the sections that were referenced in the troubleshooting chart (para 3-6b). If the troubleshooting chart indicates a section but does not give a step number, perform all of the steps given in that section starting with step a.

(2) Observe that multimeter indication is within the tolerance specified in the chart for each step. If it is not, refer to the T-1054(P)/GRC-144(V) interconnecting diagram (fig. 5-15 or 5.15.1) to determine whether the fault is defective wiring or a defective circuit element.

c. T-1054(P)A/ GRC-144(V) DC  
Power Distribution Checks Chart.

Section	Step	Connect multimeter leads between		Multimeter indication (ohms)
		pin	and pin	
1	a	1A15W27XA1B-	2	Zero
	b		-2	Zero
	c		-2	Zero
2	a	1AISW27XAIJ-	21	Zero
	b		-21	Zero

Section	Step	Connect multimeter leads between		Multimeter indication (ohms)
		pin	and pin	
3	c	1A15W27XA1B-3	1A15W27XA12B-4	Zero
	d	-22	1A15W27XA12B-5	Zero
	a	1A15W27XA1B-7	1A15W27XA12B-6	Zero
	b	-26	-19	Zero
	e	-27	-37	Zero
4		1A15W27XA1B-8	1A15W27XA13B-36	Zero
5	a	1A15W27XA1B-10	1A15W27XA13B-38	Zero
	b	-29	-39	Zero
6	a	1A15W27XA1B-11	1A15W27XA13B-34	Zero
	b	-60	-35	Zero
7	a	1A15W27XA1B-12	1A15W27XA12B-1	Zero
	b	-12	1A15W7J4-A	Zero
	c	-47	1A15W27XA12B-2	Zero
	d	-47	1A15W27J4-B	Zero
8	a	1A15W27XA1B-14	1A15W27J1-A	Zero
	b	-14	1A15W27XA1B-7	Zero
	c	-14	1A15W27J4-E	Zero
	d	-33	1A15W27J1-B	Zero
	e	-33	1A15W27XA12B-8	Zero
		-33	1A15W2J4-F	Zero
		-33	1A15W27J1-C	Zero
9	a	1A15W27XA1B-15	1A15W27J1-D	Zero
	b	-34		Zero
10	a	1A15W27XA1B-16	1A15A8XDS5-C2	Zero
	b	-16	1A15W27XA13B-29	Zero
	c	-16	1A15W27J1-E	Zero
	d	-16	1A15W27J4-K	Zero
	e	-16	1A15A8XDS10-G	Zero
	f	-16	1A15A8XDS1-G	Zero
	g	-16	1A15A8XDS14-G	Zero
	h	1A16W27XA1B-16	1A15A8XDS18-G	Zero
	i	-16	1A15A8XDS9-1	Zero
	k	-16	1A15W27XA12B-2	Zero
	l	-16	1A15W27J4-B	Zero
	m	-35	1A15A8XDS-B2	Zero
	n	-35	1A15E1	Zero
11	a	1A15W27XA1B-18	1A15W27J1-G	Zero
	b	-37	-H	Zero

**3-9. Isolating Troubles in Power Supply Chassis Assembly 1A1A13**

*a. Preparation of Power Supply Chassis Assembly 1A1A13.*

(1) Remove power supply 1A1 (para 3-22).  
 (2) Remove plug-in components 1A1A1 through 1A1A4, and 1A1A6 through 1A1A12 (TM 11-20-695-12).

(3) Remove the ten screws and associated washers securing rear shield (fig. 3-9) to power supply chassis assembly 1A1A13.

*b. Procedure.*

*c. Power Supply Chassis Assembly 1A1A13 (Checks Chart).*

(1) Refer to the chart (c below). Connect the multimeter leads between the two pins listed in the steps of the sections that were referenced in the troubleshooting chart (para 3-6b). If the troubleshooting chart indicates a section but does not give a step number, perform all of the steps given in that section starting with step a.

(2) Observe that multimeter indication is within the tolerance specified in the chart for each step. If it is not, refer to the power supply 1A1 interconnecting diagram (fig. 5-17) and determine whether the fault is defective wiring or a defective circuit element.

Section	Step	Connect multimeter leads between		Multimeter indication (ohms)
		pin	and pin	
1	a	1A1A13XA1-5	1A1A13J1	200K ±2K
	b	-5	1A1A13P2-2	Zero
	c	-6	-21	Zero

Section	Step	Connect multimeter leads between		Multimeter indication (ohms)	
		pin	and pin		
2	d	-8	1A1A13XDS1-2	Zero	
	e	-9	1A1A13P2-21	Zero	
	f	-13	-2	Zero	
	g	-13	1A1A13XDS1-1	20 ± 2	
	h	-14	1A1A13P1-1	Less than 1	
	i	-15	-20	Zero	
	a	1A1A3XA2-5	1A1A13J2	200 K ± 2K	
	b	-5	1A1A13P-3	Zero	
	c	-8	1A1A13XDS2-2	Zero	
	d	1A1A13XA2-8	1A1A13P2-22	Zero	
3	e	-9	-22	Zero	
	f	-18	-2	Zero	
	g	-18	1A1A13XDS2-1	20 ± 2	
	h	-14	1A1A13P1-3	Less than 1	
	i	-15	-22	Zero	
	a	1A1A13XA3-7	1A1A13XDS3-2	Zero	
	b	-7	1A1A13P2-26	Zero	
	c	-8	1A1A13J6	237 K ± 2.5K	
	d	-8	1A1A1P2-7	Zero	
	e	-13	1A1A13XDS3-1	39 ± 4	
4	f	13	1A1A13P2-26	Zero	
	g	-14	1A1A13P1-6	Less than 1	
	h	-15	-25	Zero	
	a	1A1A13XA4-7	1A1A13XDS4-2	Zero	
	b	-7	1A1A13P2-27	Zero	
	c	-8	1A1A13J4	237 K ± 2.5K	
	d	-8	1A1A13P2-8	Zero	
	e	-8	1A1A13XDS4-1	39 ± 4	
	f	1A1A13XA4-13	1A1A13P2-27	Zero	
	g	-14	1A1A13P1-7	Less than 1	
5	h	-15	-26	Zero	
	a	1A1A13XA6-3	1A1A1J6	475 K ± 5K	
	b	-8	1A1A1P2-10	Zero	
	c	-8	1A1A13XDS6-2	Zero	
	d	-4	1A1A13P2-29	Zero	
	e	-13	-10	Zero	
	f	-13	1A1A3XDS6-1	150 ± 15	
	g	-14	1A1A13P1-9	Less than 1	
	h	-15	-28	Zero	
	6	a	1A1A13XA7-3	1A1A3J7	475 ± K
b		-3	1A1A13P2-11	Zero	
c		-6	1A1A13XDS7-2	Zero	
d		-8	1A1A13P2-30	Zero	
e		-13	-11	Zero	
f		-13	1A1A13XDS7-1	150 ± 15	
g		-14	1A1A1AP1-10	Less than 1	
h		-15	-29	Zero	
7		a	1A1A3XA6-3	1A1A18J8	475 K ± 5K
		b	-3	1A1A13P1-10	Zero
	c	-8	1A1A13XDS8-2	Zero	
	d	-8	1A1A13P2-31	Zero	
	e	-13	-12	Zero	
	f	-13	1A1A1SXDS8-1	150 ± 15	
	g	-14	1A1A13P1-11	Less than 1	
	h	-15	-30	Zero	
	8	a	1A1A3XA9-3	1A1A13XDS9-2	Zero
		b	-6	11A18P	Zero
c		-8	1A1A1SJ9	475 K ± 5K	
d		-8	1A1A10P-14	Zero	
e		-8	1A1A13XDS9-1	150 ± 15	
f		-13	1A1A13P2-33	Zero	
g		-14	1A1A13P1-12	Less than 1	
h		-15	-31	Zero	



Section	Step	Connect multimeter leads between		Multimeter indication (ohms)
		pin	and pin	
9	a	1A1A13XA10-5	1A1A13J10	604K ± 6K
	b	-5	1A1A13P2-13	Zero
	c	-5	-15	Zero
	d	-8	1A1A13XDS10-2	Zero
	e	1A1A13XA10-8	1A1A1P2-32	Zero
	f	-8	-34	Zero
	g	-9	-34	Zero
	h	-13	-15	Zero
	i	-13	1A1A13XDS10-1	220 ± 22
	j	-14	1A1A13P1-14	Less than 1
	k	-15	-33	Zero
10	a	1A1A13XA11-7	1A1A13J11	1.1 M ± 55K
	b	-7	1A1A13P2-16	Zero
	c	-8	1A1A13XDS11-2	Zero
	d	-8	1A1A13P2-35	Zero
	e	-13	-16	Zero
	f	-13	1A1A13XD11-1	470 ± 47
	g	-14	1A1A13P1-16	Less than 1
	h	-15	-35	Zero
11	a	1A1A13XA12-7	1A1A13J12	1.1 M ± 65K
	b	-7	1A1A13P2-18	Zero
	c	-8	1A1A13XDS12-2	Zero
	d	-8	1A1A13P2-37	Zero
	e	-13	-18	Zero
	f	1A1AISXA12-13	1A1A13XDS12-1	470 ± 47
	g	-14	1A1A13P1-18	Less than 1
	h	-15	-37	Zero

**3-10. Isolating Troubles in Plate Assembly 1A16**

a. *Preparation of T-1054(P)/GRC-144(V)* Refer to the troubleshooting chart (para 3-6b) and determine those sections of the plate assembly 1A16 checks to be performed. Refer to the chart given in c below and figures 3-16 and 3-16 to determine the components to be removed to gain access to the connector pins. Do not remove plate assembly 1A16. Procedures for removal of components 1A2 through 1A11 are given in TM 115820-695-12. Procedures for removal of power supply 1A1 or composite assembly 1A13/1A14 are given in paragraphs 3-22 and 3-30.

b. *Procedure.*

(1) Refer to the chart (c below). Connect the multimeter leads between the two pins listed in the steps of the sections that were referenced in the troubleshooting chart (para 3-6b). If the troubleshooting chart indicates a section but does not give a step number, perform all of the steps given in that section starting with step a.

(2) Observe that multimeter indication is within the tolerance specified in the chart for each step. If it is not, refer to the T-1054(P)/GRC-144(V) or T-1054(P)A/GRC-144(V) interconnecting diagram (figs 5-15 or 5-15.1) and determine whether the fault is defective wiring or a defective circuit element.

c. *Plate Assembly 1A16 Checks Chart.*

Section	Step	Connect multimeter leads between		Multimeter indication (ohms)
		pin	and pin	
1	a	1A1I6W25XA2-1	1A16A8XDS10-A	Zero
	b	-2	-D	Zero
	c	4	1A15W27XA1B-15	Zero
	d	-4	-34	Zero
	e	-5	1A15E1	Zero
2	a	1A16W25XA3-5	1A15E1	Zero
	b		1A16W25XA3-10	Zero
	c	-7	-11	Zero
	d	-8	A16W25XA8-8	Zero
	e	-9	1A16W25XA5B-A3	Zero
	f	-10	1A16W26XA4-8	Zero
	g	-11	1A15A8S4B-3	Zero

Section	Step	Connect multimeter leads between		Multimeter indication (ohms)
		pin	and pin	
3	a	1A16W25XA4-3	A15W27XA1B-15	Zero
	b	-4	-34	Zero
	a	-4	1A16E1	Zero
	d	-8	1A16W25XAS10	Zero
4	a	1A16W25XA5A-1	1A15W27X1A1B-16	Zero
	b	-2	-35	Zero
	c	-6	1A16E1	Zero
	d	1A16W25XA5A-7	1A15W271A13B-23	Zero
	e	-8	1A15AXDS18-A	Zero
	f	-9	-D	Zero
	g	-10	1A15ASXDS14-A	Zero
	h	-11	-D	Zero
	i	-16	1A1W27XA1B-14	Zero
	j	-17	-33	Zero
	k	-25	1A15A8XIS14-C	Zero
	l	-26	-B	Zero
	m	-29	1A5ABXDS1-C	Zero
	n	-30	-B	Zero
	o	-2	1A16W22P1	Zero
	p	-4	1A15A8S4B-27	Less than 5K
q	-5	1A1E1	Zero	
r	-12	1A15A8SB-17	Less than 5K	
s	-14	1A1W23P1	Zero	
t	-15	1A16ASS4B-29	Less than 5K	
u	1A16W26XA6A-17	1AISW27XA14-7	Zero	
v	-A3	1A16W25XA3	Zero	
5	a	1A16W25XA7-2	1AIW25XA8-7	Zero
	b	-3	1A15W27XA1B-15	Zero
	c	-4	-34	Zero
	d	-6	1A16E1	Zero
	e	-6	1A15A8S4B-13	Zero
	f	-7	1A15ASS4A-13	Zero
	g	-8	1A16W25XA84-	Zero
	h	-9	1A1A8S4B-15	Zero
6	a	1A16W25XA8-1	1A15W27XA1B-16	Zero
	b	-2	-34	Zero
	c	-3	-15	Zero
	d	-4	-34	Zero
	e	-5	1A15E1	Zero
	f	-6	1A16W26XA7-8	Zero
	g	-7	-2	Zero
	h	-8	1A16W25XA3-8	Zero
	i	-9	1A15A8S4B-11	Zero
	j	-10	-9	Zero
7	a	1A16W25XA11-2	1A15W27XA1B-37	Zero
	b	-5	1A15E1	Zero
	c	-1	1A15W27XA1B-18	Zero

**3-11. Isolating Troubles in Electrical Equipment Cabinet 1A15**

**WARNING**

115 vac is present in T-1054(P) A/GRC-144(V) and T-1054(P)/ GRC-144(V). Do not perform any of the continuity or resistance checks given in this paragraph while the equipment is connected to the primary power source.

a. Preparation of T-1054(P)/GRC-144(V) and T-1054(P)A/GRC-144(V).

- (1) Remove power supply 1A1 (para 3-22).
- (2) Remove orderwire assembly 1A13/ 1A14 (para 3-30).
- (3) Remove digital data modem 1A12 or digital data combiner (para 3-29 or 3-29.1).

(4) Remove components 1A3 and 1A5 (TM 11-5820-695-12).

**NOTE**

**For Radio Sets AN/GRC-144(V)3 and AN/GRC-144 (V)4 also disconnect equipment interconnection cables from 1A15J22 and 1A15J23 (fig. 3-7.1).**

(5) Disconnect the equipment interconnections cables from jacks 1A15W27J4, 1A15W27J5, and 1A15W27J6 (fig. 3-7).

**NOTE**

**For Radio Sets AN/GRC-144(V)3 and AN/GRC-144 (V)4 also disconnect cable 1A15W28 and 1A15W29 connectors 1A15P4 and 1A15P5 from digital data combiner 1A12 jacks 1A12J1 and 1A12J2 (fig. 3-13).**

(6) Disconnect coaxial cable 1A15W4 from jack 1A12J3 (fig. 3-13), and disconnect plug 1A15P6 from jack 1A15J20 (fig. 3-7).

*b. Procedure.*

(1) Refer to the chart (c below). Connect the multimeter leads between the two pins listed in the steps of the sections that were referenced in the troubleshooting chart (para 3-6b). If the troubleshooting chart indicates a section but does not give a step number, perform all of the steps given in that section starting with step a.

(2) Observe that multimeter indication is within the tolerance specified in the chart for each step. If it is not, refer to the T-1054(P)/GRC-144(v) or T-1054(P)A/GRC-144(V) interconnecting diagram (fig. 5-15 or 5-15.1) to determine whether the fault is defective wiring or a defective circuit element.

c. Electrical Equipment Cabinet 1A15 Checks Chart.

Section	Step	Connect multimeter leads between		Multimeter indication (ohms)	
		pin	and pin		
1	a	1A1SWS7J4-A	1A15W27XAB-12	Zero	
	b	-B	-37	Zero	
	c	-C	-2	Zero	
	d	-D	-21	Zero	
	e	-E	-14	Zero	
	f	-F	-33	Zero	
	g	-G	1A15W27XA12B-22	Zero	
	h	-H	1A1SW2TXA13B-22	Zero	
	i	J	1A15E1	Zero	
	j	K	1A15W27XA1-16	Zero	
	k	-L	1A15W W7XA12-23	Zero	
	l	-M	1A15W27XA112A-3	Zero	
	m	-N	-4	Zero	
	n	-P	-9	Zero	
	o	-R	-10	Zero	
	p	-S	1A15W27XA13B-1	Zero	
	q	-T	1A15W27XA13B-2	Zero	
	r	1A16WUTJ4-U	1A15A8XDS10-C	Zero	
	s	-V	1A15A8XDS10-B	Zero	
	t	-W	1A15E1	Zero	
	u	-X	1A15W27XA2B-10	Zero	
	v	-Y	1A15W27XA12B-11	Zero	
	w	-a	A1AWmXA13B-19	Zero	
	x	-c	1A15ASS2-N4I	Zero	
	y	-e	1A15E1	Zero	
	2	a	1A1SW27J-A	1A1SW27XA13B-60	Zero
b		-C	-46	Zero	
3	a	1A165AJ19 (TEST LEAD)	1A15A8S4B-5	Zero	
4	b		1A15A8S4A-7	Zero	
	a	1A15W27XA12A-1	1A15A8XDS1-D	Zero	
	b	-2	-A	Zero	
	c	-3	1A15W27J4-M	Zero	
	d	-4	-N	Zero	
	e	-5	1A1SW27XA13A-1	Zero	
	f	-6	1A15W27XA13B-7	Zero	
	g	-7	1A15W27XA13B-4	Zero	
	h	1A16W27XA12A-8	1A15W27XA13B-4	Zero	
	i	-9	1A15W27J4-P	Zero	
	j	-10	-R	Zero	
	k	-11	1A15A8XDS1-C	Zero	
	l	-12	-B	Zero	
	m	-15	1A15W27XA13B-25	Zero	
	n	1A16WM7XA12A-16	1A15J14-16	Zero	
	o	-19	1A15W27A13B-8	Zero	
	p	-20	-5	Zero	
	q	1A11W27XA12A-21	1A15W27XA13B-12	Zero	
	5	a	1A15W27XA12B-1	1A15W27XA1B-12	Zero
		b	-2	-31	Zero
c		-3	-2	Zero	
d		-4	-3	Zero	
e		-5	-22	Zero	
f		-6	-7	Zero	
		-7	-14	Zero	

Section	Step	Connect multimeter leads between		Multimeter indication (ohms)
		pin	and pin	
6	g	-8	-38	Zero
	h	-9	1A1AE1	Zero
	i	-13	1A16J20-E	Zero
	j	1A15W27A12B-16	1A15W27XA1B-21	Zero
	k	-23	1A15E1	Zero
		-25	1A15J20-D	Zero
	a	1A15W27XA1SA-1	1A15W27XA12A-5	Zero
	b	-6	-21	Zero
	c	-4	-8	Zero
	d	-A1	1A15W4P1	Zero
7	e	-A2	1A15W3J6	Zero
	a	1A15W27XA13B-1	1A1W27J4-S	Zero
	b	-2	-T	Zero
	c	-4	1A15W27XA12A-7	Zero
	d	-4	-20	Zero
	e	-7	-6	Zero
	f	-8	-19	Zero
	g	-10	1A15W26XAS-6	Zero
	h	-11	-7	Zero
	i	-13	1A1E1	25K ± 2.5 K
8	j	-13	1A15W27XA1B-15	Less than 25K
	k	-17	1A16E1	8.0
	l	-18	1A15A8S2C1	Zero
	m	1A15W27XA13-19	1A156W2J4-2	Zero
	n	-20	1A15AXDS5-C1	Zero
	o	-21	-B1	Zero
	p	-22	1A15W27J4-H	Zero
	q	-23	1A16W25XA5A-7	Zero
	r	-25	1A15W27XA12A-15	Zero
	s	-26	1A15E1	Zero
	t	-27	1A16E2	Zero
	u	-28	1A15A8XDS5-D1	Zero
	v	-29	1A15W27XA1B-16	Zero
	w	-30	-35	Zero
	x	-34	-11	Zero
	y	-35	30	Zero
	z	-36	-8	Zero
	aa	-37	-27	Zero
	ab	-38	-10	Zero
	ac	-39	29	Zero
	ad	-41	1A15A8S1-NC1	Zero
	ae	-43	-NO1	Zero
	af	-42	-C1	Zero
	ag	1A15W27XA13-44	1A15A8S1-C2	Zero
	ah	-45	1A15A8XDS5-A1	Zero
	ai	-46	1A15W27J6-C	Zero
aj	-50	1A15W27J5-A	Zero	
a	1A15W27X14-1	1A15A8XD9-2	Zero	
b	-2	1A16E1	Less than 1	
c	-3	1A15E1	Zero	
d	-5	1A15A8S3-3	Zero	
e	-6	-1	Zero	
f	-7	1A16W25XA5B-17	Less than 1	
g	-8	1A1SE1	Zero	
h	-9	1A15A8-3	Zero	
i	-10	-1	Zero	
j	-A1	1A15A8S4B-19	Zero	

Section	Step	Connect multimeter leads between		Multimeter indication
		pin	and pin	(ohms)
<b>NOTE</b>				
<b>Section 9 and 10 steps pertain to AN/GRC-144(V)3 and AN/GRC-144(V)4 only.</b>				
9	a	1A15P4-1	1A15J22-A	Zero
	b	-2	-B	Zero
	c	-12	-Y	Zero
	d	-13	-Z	Zero
	e	-14	-G	Zero
	f	-15	-H	Zero
	g	-4	-D	Zero
	h	-5	-E	Zero
	i	-16	-K	Zero
	j	-17	-J	Zero
	k	-7	-M	Zero
	l	-18	-N	Zero
	m	-19	J23-C	Zero
	n	-20	-D	Zero
	o	-9	-E	Zero
	p	-10	-F	Zero
	q	P4-A1	1A15W7J13-A2	Zero
	r	1A15P4-3	1A15P4-11	Zero
	s	-3	1A15J22-C	Zero
t	-3	-F	Zero	
	u	-6	-L	Zero
10	a	1A15P5-1	1A15J22-j	Zero
	b	-2	-i	Zero
	c	-4	-9	Zero
	d	-5	-f	Zero
	e	-12	-p	Zero
	f	-13	-n	Zero
	g	-9	-a	Zero
	h	-10	-b	Zero
	i	-6	J23-A	Zero
	j	-7	-B	Zero
	k	-18	-M	Zero
	l	-19	-N	Zero
	m	-15	J22-P	Zero
	n	-16	-R	Zero
	o	1A15W4-P2	P5-A1	Zero
	p	1A15P5-3	1A15J22-h	Zero
	q	-14	-e	Zero
	r	-11	-q	Zero
	s	-17	1A15J23-p	Zero
t	-20	1A15J22-c	Zero	

3-12. Receiver, Radio R-1467(P)/GRC-144(V) and R-1467(P)A/GRC-144(V) Troubleshooting Chart

**WARNING**

**115 vac is present in Receiver, Radio R-1467(P)/GRC-144(V) and R-1467(P)A/GRC-144(V). Do not remove or replace parts, or perform continuity or resistance checks while primary power is applied to AN/GRC-144(V) Radio Sets.**

a. *Use of the Chart.* The R-1467(P)/GRC-144(V) and R-1467(P)A/GRC-144(V) Troubleshooting Chart below supplements the operational checks and corrective measures contained in TM 11-5820-695-12. If the operational checks and measures fail to correct the trouble or indicates that higher maintenance is required, apply the corrective action in the chart below. To use the chart, read down the Symptom column of the troubleshooting chart until the abnormal symptom or

condition is found. Perform the corrective actions indicated in the chart until the abnormal symptom or condition is corrected. Figures 3-17 through 3-24 are ports location diagrams which will aid the maintenance man in locating parts.

b. *R-1467(P)/GRC-144(V) and R-1467(P)A/GRC-144(V) Troubleshooting Chart.*

**NOTE**

**Unless otherwise specified, the troubleshooting chart below pertains to Receiver, Radios R-1467(P)/GRC-144(V) and R-1467(P)A/GRC-144(V). Refer to figure 5-21 for the R-1467(P)/GRC-144(V) interconnection diagram and refer to figure 5-21.1 for the R-1467(P)A/GRC-144(V) interconnection diagram.**

<i>Item No.</i>	<i>Symptom</i>	<i>Probable trouble</i>	<i>Corrective actions</i>
1	POWER 5 AMP SLO-BLO fuse blows when replaced.	<p>a. Defective component or wire in primary power distribution circuits.</p> <p>b. Defective component or wire in power supply assembly 2A1A5.</p> <p>c. Electrical equipment chassis 2A14A10 defective.</p> <p>d. Defective wiring in primary power distribution circuit</p>	<p>a. Remove power supply 2A1 (para 340) end electrical frequency synthesizer 2A14 (para 349) from electrical equipment cabinet 2A15. Insert replacement fuse and then set POWER ON/OFF switch on meter pane assembly 2A15A2 to ON. If replacement fuse blows, proceed to step d below. Otherwise, proceed to steps b and c below to isolate the fault.</p> <p>b. Perform the power supply chassis assembly 2A1A6 cheeks (para 3-15c, sections 1 through 4).</p> <p>c. Check electrical equipment chassis 2A14A10 (para 3-49) by substitution.</p> <p>d. Perform the R-1467(P)/GRC-144(V) primary power distribution checks (para 3-13c, sections 3 and 5).</p>

<i>Item No.</i>	<i>Symptom</i>	<i>Probable trouble</i>	<i>Corrective actions</i>
		e. Vane axial fan 2A15B1 defective	e. Remove vane axial fan 2A15B1 (para 3-41) and use the TS-352 B/U to check its resistance as follows: T1 to T4 should be $500 \pm 100$ ohms, and T1 to T5 should be $800 \pm 100$ ohms.
		f. Capacitor 2A15C1 defective	f. Check capacitor 2A15C1 (para 2) by substitution.
		g. Power transformer 2A15A4T1 defective.	g. Replace power transformer 2A15A4T1 (par 3a-4).
2	TDA 1 AMP SLO-BLO fuse blows when replaced.	a. Defective wiring in primary power distribution circuits.	a. Perform the R-1467/GRC-144 primary power distribution checks (para-1c, section 2).
		b. Tunnel diode amplifier 2A2 defective.	b. Replace tunnel diode amplifier 2A2 (TM 11-5820-695-12).
3	All indicators on meter panel assembly 2A15A2 not lighted.	a. POWER 5 AMP SLO-BLO fuse 2A16A2F1 defective.	a. Check POWER 5 AMP SLO-BLO neon fuse indicator on meter panel assembly 2A15A2. If lighted, refer to item No. 1 in this chart.
		b. Same as item No. 9 in this chart	b. Check indicators on power supply 2A1. If any indicator not lighted, refer to item No. 9 in this chart.



<i>Item No.</i>	<i>Symptom</i>	<i>Probable trouble</i>	<i>Corrective actions</i>
4	TDA OVEN indicator does not cycle on and off.	<p>a. Defective wiring</p> <p>b. Indicator assembly 2A15A2XDS1 defective.</p>	<p>a. Check for continuity between: pin 2 of 2A15A2XDS1 (fig. 5-21) and pin C of connector 2A165W2P; and pin 1 of 2A15A2XDS1 and pin D of connector 2A15W2P2 Also check resistance between pin 9 of 2A15A2XIS1 and terminal 2 of POWER 5 AMP SLO-BLO fuse 2A165A2F1. Resistance should be <math>2200 \pm 20</math> ohms.</p> <p>b. Replace indicator assembly 2A165A2XDS1 (fig. 3-19).</p>
5	SYNTH OVEN indicator not lighted	<p>a. Defective wiring</p> <p>b. Indicator assembly 2A15A2XDS10 defective.</p> <p>c. Electrical equipment chassis 2A14A10 defective</p>	<p>a. Check for continuity between: pin 2 of 2ALSA2XDSL1 (fig. 5-21) and pin 1 of connector 2A15W2XA14; pin 1 of 2A15A2XD610 and pin G of 2A15A2XDS6; and pin 3 of 2A15A2XDS10 and the E2 CAB GRD lug on top of 2A15.</p> <p>b. Replace indicator assembly 2A15A2XDS10 (fig. 3-19).</p> <p>c. Replace electrical equipment chassis 12A14A10 (para 3-49).</p>
6	5V and 28V indicators on electrical frequency synthesizer 2A14 not lighted.	<p>a. Defective wiring</p> <p>b. Electrical equipment chassis 2A14A10 defective.</p>	<p>a. Remove electrical frequency synthesizer 2A14 (para 849) and check for continuity between pins 5 and 6 of connector 2A15W2XA14 (fig. 21).</p> <p>b. Replace electrical equipment chassis 2A14A10 (para 3-49).</p>
7	Any fault indicator on electrical frequency synthesizer 2A14 lighted.	<p>c. Electrical equipment chassis 2A14A0 defective.</p>	<p>Replace electrical equipment chassis 2A14A10 (par 3-49).</p>
8	Power on and vane axial fan 2A15B1 not operating.	<p>a. Vane axial fan 2A15B1 defective</p> <p>b. Capacitor 2A15C1 defective</p> <p>c. Defective wiring in primary power distribution circuits.</p>	<p>a. Remove vane axial fan 2A15B1 (para 341) and use the TS-352 B/U to check its resistance as follows: T1 to T4 should be <math>600 \pm 100</math> ohms, and T1 to T6 should be <math>800 \pm 100</math> ohms.</p> <p>b. Check capacitor 2A15C1 (para 3-42) by substitution</p> <p>c. Use the R-147/GRC-144 Interconnecting diagram (fig5-21) and TS-42 B/U to check wiring between vane axial fan 2A15B1 and POWER ON/OFF switch 2A15A2S2</p>
9	Any indicator lamp on power supply 2A1 not lighted.	<p>a. Power supply chassis assembly 2A1A5 defective.</p> <p>b. Defective component or wire in dc power distribution circuits.</p> <p>c. Defective component or wire in primary power distribution circuits.</p>	<p>a. Check power supply chassis assembly 2A1A5 by substitution (para 3-40). If indicator lights after 2A1A5 is replaced, use the power supply chassis assembly 2A1A5 checks (para 3-15c, sections 1 through 4) to isolate the trouble.</p> <p>b. Perform the R-1467/GRC-144 dc power distribution checks (para-3-14c, sections 1 through 4).</p> <p>c. Perform the R14617/GRC-144 primary power distribution checks (para 3-13c, sections 1 through 5).</p>

<i>Item No.</i>	<i>Symptom</i>	<i>Probable trouble</i>	<i>Corrective actions</i>
10	Out of color band meter indication obtained at any of the component test points (TM 11-5820-695-12)	Same as item No.9 in this chart	Perform the corrective action listed for item No. 9 in this chart.
11	Zero meter indication obtained when meter selector switch is placed in any position.	<ul style="list-style-type: none"> <li>a. Defective wiring on meter panel assembly 2A15A2.</li> <li>b. Meter 2A15A2M1 defective</li> <li>c. Meter selector switch 2A15A2S1 defective.</li> </ul>	<ul style="list-style-type: none"> <li>a. Use the R-1467/GRC-144 interconnecting diagram (fig. 5-21) and TS-S62 B/U to check wiring between meter selector switch 2A15A2S1 and meter 2A15A2M1.</li> <li>b. Use the receiver meter 2A15A2M1 calibration procedure (para 3-63) to check meter 2A15A2M1.</li> <li>c. Replace meter selector switch 2A15A2S1 (fig. 3-18).</li> </ul>
12	Both the green and red lamps in any status or alarm indicator lighted.	Defective wiring between indicator and its associated lamp driver. TS-352 B/U to isolate the defective wiring.	Use the R-1467/GRC-144 interconnecting diagram (fig. 5-21) and
13	CARR (IF) indicator lighted red	<ul style="list-style-type: none"> <li>a. Defective wiring in plate assembly 2A16</li> <li>b. Defective wiring or component in local oscillator circuits.</li> <li>c. Defective wiring in plate assembly 2A16.</li> <li>d. Coaxial cable 2W2 or 2A15W1 defective.</li> <li>e. Components 2FL4 or 2FL6 defective.</li> </ul>	<ul style="list-style-type: none"> <li>a. Turn meter selector switch on meter panel assembly 2A15A2 to CARRIER (IF). If meter indication is less than 110, proceed to b below. Otherwise, perform the plate assembly 2A16 checks (para 3-16c, section 8 (step c))</li> <li>b. Turn meter selector switch on meter panel assembly 2A15A2 to LOCAL OSC POWER. If meter indication is less than 30, refer to item No. 26 in this chart</li> <li>c. Perform the plate assembly 2A16 checks (para 3-16c, sections 1 and 4).</li> <li>d. Check coaxial cables 2W2 and 2A15W1 (fig. 3-24) by substitution.</li> <li>c. Check components 2FL4 and 2FL6 (para 344 and S45) by substitution.</li> </ul>
14	SYNTH LOCK indicator lighted red.	<ul style="list-style-type: none"> <li>a. Electrical equipment chassis 2A14A10 defective.</li> <li>b. Defective wiring</li> </ul>	<ul style="list-style-type: none"> <li>a. Check electrical equipment chassis 2A14A10 by substitution (para 3-49).</li> <li>b. Remove electrical frequency synthesizer 2A14 (para 3-49) and alarm monitor 2A12, and check for continuity between pin 7 of connector 2A15W2XA14 and 17 of connector 2A16W1XA12A (fig 6-21). Also check resistance between pin 8 and 9 of connector 2A16W1XA12B. Resistance should be greater than 10 ohms.</li> </ul>
15	TRAF indicator lighted red	<ul style="list-style-type: none"> <li>a. Defective wiring in plate assembly 2A16.</li> <li>b. 1.0 MHz/3.8 MHz low pass filter 2A3 defective</li> </ul>	<ul style="list-style-type: none"> <li>a. Perform the plate assembly 2A16 checks (para S-16c, section 7 (step d)).</li> <li>b. Replace 1.0 MHz/3.8 MHz low pass filter 2A3(fig. 3-17),</li> </ul>
16	Meter indication for SYNTH meter selector switch position not in yellow band.	<ul style="list-style-type: none"> <li>a. Defective wiring In electrical equipment cabinet 2A15.</li> </ul>	<ul style="list-style-type: none"> <li>a. Perform the electrical equipment cabinet 2A15 checks (para 3-17c, section 3 (step a)).</li> </ul>

<i>Item No.</i>	<i>Symptom</i>	<i>Probable trouble</i>	<i>Corrective actions</i>
17.	Meter indication for <b>FREQ MIXER CURRENT 1</b> meter selector switch position not in yellow band.	<ul style="list-style-type: none"> <li>b. Electrical equipment channels 2A14A10 defective</li> <li>a. Meter calibration required</li>   <li>b. Same as item No. 16 in this chart</li>   <li>c. Defective wiring in plate assembly. 2A16.</li> <li>d. Coaxial cable 2A15W3 defective</li> <li>e. Bandpass filter 2FL21 defective</li> <li>f. Electrical equipment chassis 2A14A10 defective</li> </ul>	<ul style="list-style-type: none"> <li>b. Replace electrical equipment chassis 2A14A10 (para 3-49).</li> <li>a. Turn meter selector switch on meter panel assembly 2A15A2 to LOCAL OSC POWER. If this meter indication is not in yellow band, proceed to step b below. If meter indication is in yellow band, perform the R-1407/GRC-144 local oscillator metering circuits calibration procedure (para-65).</li> <li>b. Turn meter selector switch on meter panel assembly 2A15A2 to SYNTH. If this meter indication is not in yellow band, perform the corrective action given for item No. 16 in this chart.</li> <li>c. Perform the plate assembly 2A16 checks (para 3-16c, sections 2 and 3).</li> <li>d. Check coaxial cable 2A15W3 (fig. 82) by substitution</li> <li>a. Check bandpass filter 2FL21 (fig. 3-16) by substitution.</li> <li>f. Replace electrical equipment chase 2A14A10 (para 3-49).</li> </ul>
18	Meter indication for <b>FREQ MIXER CURRENT 2</b> meter selector switch position not in yellow band.	<ul style="list-style-type: none"> <li>a. Meter calibration required</li>   <li>b. Same as item No. 16 in this chart</li>   <li>c. Defective wiring in plate assembly 2A16</li> <li>d. Same as item No. 17 in this chart</li> </ul>	<ul style="list-style-type: none"> <li>a. Turn meter selector switch on meter panel assembly 2A15A2 to LOCAL OSC POWER. If this meter indication is not in yellow band, proceed to <i>b</i> below. If meter indication is in yellow band, perform the R-1467/GRC-144 local oscillator metering circuit calibration procedure (para 3-65).</li> <li>b. Turn meter selector &amp;witch on meter panel assembly 2A15A2 to SYNTH. If this meter indication not in the yellow band, perform the corrective action given for item No. 16 in this chart</li> <li>c. Perform the plate assembly 2A16 checks (para 3-16c, section 5).</li> <li>d. Perform the corrective action given in steps <i>c</i> through <i>f</i> of item No. 17 in this chart.</li> </ul>
19	Meter indication for <b>MULT OSC</b> meter selector switch position not in black band.	<ul style="list-style-type: none"> <li>a. Meter calibration required</li>   <li>b. Defective wiring in plate assembly 2A16</li> </ul>	<ul style="list-style-type: none"> <li>a. Turn meter selector switch to LOCAL OSC POWER. If this meter indication is not in the yellow band, proceed to step 6 below. If this meter indication is in yellow band, perform the R-1467/GRC-144 local oscillator metering circuits calibration procedure (para 3-65).</li> <li>b. Perform the para assembly 2A16 checks (para 3-16c, section 5).</li> </ul>

<i>Item No.</i>	<i>Symptom</i>	<i>Probable trouble</i>	<i>Corrective actions</i>
20	Meter indication for AGC meter selector switch position is less than 10 or greater than 150.	<ul style="list-style-type: none"> <li>a. Same as item No, 13 In this chart</li> <li>b. Defective plate assembly 2A16 wiring.</li> <li>c. Defective wiring in electrical equipment cabinet 2A15.</li> </ul>	<ul style="list-style-type: none"> <li>a. Check CARR (IF) alarm indicator. If this alarm Indicator is lighted red, perform the corrective action given for item No.11 in this chart.</li> <li>b. Perform the plate assembly 2A16 checks (para 3-1c, section 4 (steps f and g)).</li> <li>c. Use the R1467/GRC-144 inter-connecting diagram (fig. 521) and TS-52 B/U to check wiring between pins P and R of connector 2A15W2J1 and meter panel assembly 2A15A2.</li> </ul>
21	Meter indication for AMPL-MIXER CURRENT 1 meter selector switch position not in yellow band.	Defective wiring in electrical equipment cabinet 2A15.	Turn meter selector switch on meter panel assembly 2A15A2 to LOCAL OSC POWER If this meter indication is not in yellow band, perform the corrective action given for item No. 25 (b through e) in this chart. If meter Indication is in yellow band, use the R-1467/GRC-144 inter-connecting diagram (fig. 5-21) and TS-352 B/U to check continuity of wiring between pin g of connector 2A16W1XA7 and meter panel assembly 2A15A2.
22	Meter indication for AMPL MIXER CURRENT 2 meter selector switch position not in yellow band.	Defective wiring in electrical equipment cabinet 2A15.	Turn meter selector switch on meter panel assembly 2A15A2 to LOCAL OSC POWER. If this meter indication is not in yellow band, perform the corrective action given for item No. 25 (b through e) in this chart If meter indication is in yellow band, use the R-1467/GRC-144 inter-connecting diagram (fig. 5-21) and TS-352 B/U to check continuity of wiring between pin 9 of connector 2A16W1XA7 and meter paned assembly 2A15A2.
23	Meter Indication for CARR (IF) meter selector switch position is less than 110 or greater than 140.	Defective wiring in electrical up-ment cabinet 2A15.	Check CARR (IF) alarm indicator. If this alarm indicator is lighted red, perform the corrective action given for item No. 18 in this chart. If alarm indicator is not lighted red, use the R-1467/GRC-144 inter-connecting diagram (fig. 5-21) and TS-352 B/U to check continuity of wiring between pin 10 of 2A16W1XA5 and meter panel assembly 2A15A2
24	Meter indication for TRAFFIC meter selector switch position not n orange bend	<ul style="list-style-type: none"> <li>a. Meter calibration required</li> <li>b. Defective plate assembly 2A16 wiring.</li> <li>c. Defective wiring In electrical equipment cabinet &amp;A15</li> </ul>	<ul style="list-style-type: none"> <li>a. Perform the traffic metering circuit calibration procedure (para 3-64).</li> <li>b. Perform the plate assembly 2A16 checks (para 3-16c, section 7 (step d)).</li> <li>c. Use the R-1467/GRC-144 Inter-connecting diagram (fig. 5-21) and TS-352 B/U to check continuity of wiring between pin 12 of connector 2A16W1XA12A and meter panel assembly 2A15A2.</li> </ul>

<i>Item No.</i>	<i>Symptom</i>	<i>Probable trouble</i>	<i>Corrective actions</i>
25	(Meter indication for LOCAL OSC POWER meter selector switch position not in yellow band.	<ul style="list-style-type: none"> <li>a. Meter calibration required</li> <li>b. Defective wiring or component in local oscillator circuits.</li> <li>c. Defective wiring in plate assembly 2A16.</li> <li>d. Coaxial cable 2W8 or 2W9 defective.</li> <li>e. Local oscillator bandpass filter 2F16 defective.</li> </ul>	<ul style="list-style-type: none"> <li>a. Perform the R-1467/GRC-144 local oscillator metering circuits - calibration procedure (para-65).</li> <li>b. Turn meter selector switch on Meter panel assembly 2A15A2 to FREQ MIXER CURRENT 1 mad 2, If either meter indication is not in the yellow band, perform the corrective action given for Item No. 17 in this chart</li> <li>c. Perform the plate assembly 2A16 checks (para f-16c, section 1).</li> <li>d. Check coaxial cables 2W8 and 2W9 (fig. 342) by substitution.</li> <li>e. Replace local oscillator bandpass filter 2FL6 (para 3-46).</li> </ul>
26	200 MHz frequency multiplier-osc 2A13 frequency error greater than 20 kHz as determined by test (para 3-73).	<ul style="list-style-type: none"> <li>a. Defective wiring in plate assembly 2A16.</li> <li>b. 220 MHz frequency multiplier -osc 2A13 defective.</li> </ul>	<ul style="list-style-type: none"> <li>a. Perform the plate assembly 2A16 checks (para 6-1&amp;c, section 5).</li> <li>b. Replace 220 MHz frequency multiplier-osc 2A13 (TM 11-20-695-12)</li> </ul>
27	Electrical frequency synthesizer 2A14 frequency error greater than 3 kHz as determined by test (para 3-73).	<ul style="list-style-type: none"> <li>a. Defective wiring in electrical equipment cabinet 2A15.</li> <li>b. Defective plug-in component in electrical frequency synthesizer 2A14.</li> <li>c. Electrical equipment chassis 2A14A10 defective.</li> </ul>	<ul style="list-style-type: none"> <li>a. Perform the electrical equipment cabinet 2A165 checks (para 3-17c, section 3).</li> <li>b. One at a time, replace each plug-in component (2A14A1 through 2A14A7) in electrical frequency synthesizer 2A114 (TM 11-5 695-12).</li> <li>c. Replace electrical Equipment chassis 2A14A10 (para 3-49).</li> </ul>
28	Local oscillator output power less than 0.4 milliwatts as determined by test (para 3-74).	Same as item No. 26 in this chart for item No. 25 in this chart.	Perform the corrective action given
29	R-1467/GRC-144 if gain less than 150 as determined by test (Para 3-76).	<ul style="list-style-type: none"> <li>a. 70 MHz intermediate frequency amplifier 2A5 defective.</li> <li>b. Amplifier mixer 2A7 defective</li> <li>c. Tunnel diode amplifier 2A2 defective.</li> <li>d. Same as item No. 13 in this chart</li> </ul>	<ul style="list-style-type: none"> <li>a. Check 70 MHz intermediate frequency amplifier 2A5 by substitution (TM 116820-895-12).</li> <li>b. Check amplifier mixer 2A7 by substitution (TM 11-5820-695-12).</li> <li>c. Check tunnel diode amplifier 2A2 by substitution (TM i11 16820-665-12).</li> <li>d. Perform the corrective action given for item No. 13 in this chart</li> </ul>
30	R-1467/GRC-144 carrier alarm trip point not in tolerance as determined by test (para 3-75).	R-1467/GRC-144 carrier alarm adjustment required.	Perform the R-1467/GRC-144 carrier alarm adjustment procedure (para 3-6).
31	Cannot calibrate the R-1467/GRC-144 traffic metering circuit (para 3-64).	Defective component or wire in metering circuit	Remove alarm monitor 2A12 (TM 11-5820-495-12) and check resistance between pin 12 of connector 2A16W-1XA12A and pin 25 of 2A15A2S1B (fig. 5-21). Note that resistance varies smoothly from zero to 5,000 ohms as potentiometer 2A15A2R7 (fig. 8-18) is varied from one extreme to the other. Also check for continuity between pin 25 of 2A16A2S1B and the E2 CAB GRD lug on top of A15.

<i>Item No.</i>	<i>Symptom</i>	<i>Probable trouble</i>	<i>Corrective actions</i>
32	Cannot calibrate the LOCAL OSC POWER section of the R-1467(P)/GRC-144(V) and R-1467(P)A/GRC-144(V) local oscillator power metering circuits (para 3-65).	Defective component or wire in metering circuit.	Remove amplifier-mixer 2A7 and check resistance between pin 8 of connector 2A16XA7 and pin 27 of 2A15A2S1B (fig. 6-21). Note that resistance varies smoothly from zero to 5,000 ohms as potentiometer 2A15A2R5 (fig. 3-18) is varied from one extreme to the other. Also check for continuity between pin 9 of connector 2A16XA7 and pin 27 of 2A15A2S1A.
33	Cannot calibrate the FREQ MIXER CURRENT 1 section of the R-1467(P)/GRC-144(V) and R-1467(P)AGRC-144(V) local oscillator metering circuits (para 3-65)	Defective component or wire in metering circuit.	Remove frequency mixer stage 2A8 and check resistance between pin 9 of connector 2A16W1XA8 and pin 11 of 2A15A2S1A (fig. 5-21). Note that resistance varies smoothly from zero to 50,000 ohms as potentiometer 2A15A2R3 (fig. 3-18) is varied from one extreme to the other. Also check for continuity between pin 11 of 2A15A2S1B and the E2 CAB GRD lug on top of 2A15.
34	Cannot calibrate the FREQ MIXER CURRENT 2 section of the R-1467(P)/GRC-144(V) and R-1467(P)A/GRC-144(V) local oscillator metering circuits (para 3-65)	Defective component or wire in metering circuit.	Remove frequency mixer stage 2A8 and check resistance between pin 9 of connector 2A16W1XA8 and pin 13 of 2A15A2S1A (fig. 5-21). Note that resistance varies smoothly from zero to 50,000 ohms as potentiometer 2A15A2R4 (fig. 3-18) is varied from one extreme to the other. Also check for continuity between pin 13 of 2A15A2S1B and the E2 CAB GRD lug on top of 2A15.
35	Cannot calibrate the MULT-OSC section of the R-1467(P)/GRC-144(V) and R-1467(P)A/GRC-144N(V) local oscillator metering circuits (para 3-65)	Defective component or wire in metering circuit.	Remove frequency multiplier-osc 2A13 and check resistance between pin 9 of connector 2A16W1XA13 and pin 15 of 2A15A2S1B (fig. 5-21). Note that resistance varies smoothly from zero to 5,000 ohms as potentiometer 2A15A2R6 (fig. 3-18) is varied from one extreme to the other. Also check for continuity pin 15 of 2A15A2S1A and the E2 CAB GRD lug on top of 2A15.

3-13. Isolating Troubles in R-1467(P)/GRC-144(V) and R-1467(P)A/GRC-144(V) Primary Power Distribution Circuits

**WARNING**

**115 vac is present in R-1467(P)/GRC-144(V) Do not perform any of the continuity or resistance checks given in this paragraph while the equipment is connected to the primary power source.**

a. Preparation of R-1467(P)/GRC-144(V) and R-1467(P)AGRC-144(V).

(1) Remove power supply 2A1 (para 3-40).

(2) Remove switch 2A15A2S2 protective cover (fig. 3-19) by removing the four nuts and two screws that secure it to meter panel assembly 2A16A2.

(3) Remove electrical frequency synthesizer 2A14 (para 3-49).

b. Procedure.

(1) Refer to the chart (c below). Connect the multimeter leads between the two pins listed in the steps of the sections that were referenced in the troubleshooting chart (para 3-12c). If the troubleshooting chart indicates a section but does

not give a step number, perform all of the steps given in that section starting with step a.

(2) Observe that multimeter indication is within the tolerance specified in the chart for each step. If it is not, refer to the R-1467(P)/GRC-144(V) interconnecting diagram (fig. 5-21) and determine

whether the fault is defective wiring or a defective circuit element.

c. *R-1467(P)/GRC-144(V) Primary Power Distribution Check Chart.*

Section	Step	Connect multimeter leads between		Multimeter indication (ohms)
		pin	and pin	
1	a	2A165AJ5-A	2A15A2S2-4	Less than 1
	b	-B	2A16E2 (CAB GRD)	Less than 1
	c	-C	2A15A2S22	Less than 1
2	a	2A15A2S21	2A15W2-B	Zero
	b	-3	-A	Less than 1
3	a	2A15AS2-1	2A15W2XA14-4	Zero
	b	-1	2A15W2XA14-10	Zero
	c	-3	2A 1A2XDS1-3	2.2K ± 220
	d	-3	2A15W2XA14-5	Zero
	e	-3	2A15W2XA14-9	Zero
4		2A15A2S2-1	2A15A2S2-3	Less than 2
5	a	2A15W2XA1-12	2A15W2XA1-31	Less than 1
	b	-14	-33	Less than 1
	c	-16	-35	Less than 1
	d	-18	-37	Less than 1
	e	-19	2A15E2 (CAB GRD)	Zero

**3-14. Isolating Troubles in R-1467(P)/GRC-144(V) and R-1467(P)/GRC-144(V) DC Power Distribution Circuits**

**WARNING**

**115 vac is present in R-1467/GRC-144. Do not perform any of the continuity or resistance checks given in this paragraph while the equipment is connected to the primary power source.**

a. *Preparation of R-1467(P)/GRC-144(V)*

(1) Remove power supply 2A1 (para 3-40).

(2) Remove components 2A4, 2A5, 2A7, 2A10, 2A11, 2A12, and 2A13 (TM 11-5820-695-12).

(3) Disconnect plug 2A15W2P2 (fig. 3-19) from jack on rear of tunnel diode amplifier 2A2 (fig. 5-21).

b. *Procedure.*

(1) Refer to the chart (c below). Connect the multimeter leads between the two pins of the listed steps of the sections that were referenced in the troubleshooting chart (para 3-12b). If the troubleshooting chart indicates a section but does not give a step number, perform all of the steps given in that section starting with step a.

(2) Observe that multimeter indication is within the tolerance specified in the chart for each step. If it is not, refer to the R-1467(P)/GRC-144(V) interconnecting diagram (fig. 5-21) and determine whether the fault is defective wiring or a defective circuit element.

c. *R-1467(P)/GRC-144(V) DC Power Distribution Check Chart.*

Section	Step	Connect multimeter leads between		Multimeter indication (ohms)
		pin	and pin	
1	a	2A15W2XAA1-1	2A16XA10-1	Less than 1
	b	-1	2A16WIXA13-1	Zero
	c	-20	2A16XA10-2	Less than 1
	d	-20	2A16W1XA132	Zero
2	a	2A15W2XA1-3	2A16XA7-3	Less than 1
	b	-3	2A16XA5-3	Less than 1
	c	-3	2A16XA4-3	Less than 1
	d	-3	2A16W1XA11-3	Less than 1
	e	-22	2A16XA7-4	Less than 1
	f	-22	2A1&W1XA5-4	Less than 1
	g	-22	2A16XA-4	Less than 1
	h	-22	2A16W1XA11-4	Zero

Section	Step	Connect multimeter leads between		Multimeter indication (ohms)
		pin	and pin	
3	i	-4	2A15WZP2-E	Zero
	j	-23	2A15W2P2-F	Zero
4	a	-5	2A16W1XA12B-16	Zero
	b	-24	2A16WX1A12B-17	Zero
	c	-7	2A16W1XA12B-1	Zero
	b	-26	2A16W1XA12B 2	Zero
	c	-8	2A15A2XDS6-G	Zero
	d	2A15W2XA1-27	2A16E2 (CAB GRD)	Zero
	e	-19	2A16E2 (CAB GBD)	Zero

**3-15. Isolating Troubles In Power Supply Chassis Assembly 2A1A5**

*a. Preparation of Power Supply Chassis Assembly 2A1A5.*

- (1) Remove power -supply 2A1 (para 3).
- (2) Remove plug-in components 2A1A1 through 2A1A4 (TM 11482095-12).
- (3) Remove the four screws and associated washers that secure the rear shield (fig. 3-22) to power supply chassis assembly 2A1A5. Remove the rear shield.

*b. Procedure.*

(1) Refer to the chart (c below). Connect the multimeter leads between the two pins of the listed steps of the sections that were referenced in the troubleshooting chart (para 3-12b). If the troubleshooting chart indicates a section but does not give a step number, perform all of the steps given in that section starting with step a.

(2) Observe that multimeter indication is within the tolerance specified in the chart for each step. If it is not, refer to the power supply 2A1 interconnecting diagram (fig. 5-22) and determine whether the fault is defective wiring or a defective circuit element.

*c. Power Supply Chassis Assembly 2A1A5 Checks Chart.*

Section	Step	Connect multimeter leads between		Multimeter indication (ohms)
		pin	and pin	
1	a	2A1AMP-1	2A1A5J1	1.1M ± 55K
	b	-1	2A1A5XA1-7	Zero
	c	-1	2A1A5XDS1-1	470 4??
	d	-1	2A1A5XA1-13	Zero
	e	-12	-14	Less than 1
	f	-20	-8	Zero
	g	-20	2A1A5XDS1-2	Zero
	h	-31	2A1A5XA1-15	Zero
2	a	2A1A6P1-6	2A1A5J2	604K ± 6K
	b	-3	2A1A5P1-4	Zero
	c	-3	2A1A5XA2-5	Zero
	d	-3	2A1A5XDS2-1	220 ± 22
	e	-3	2A1A5XA2-13	Zero
	f	-14	2A1A5XA2-14	Less than 1
	g	-22	2A1A5XDS2-2	Zeao
	h	-22	2A1A6XDS2-8	Zero
	i	-23	-9	Zero
	j	-33	2A1A5A2-15	Zero
3	a	2A1A5P1-5	2A1A5J3	475K ± 4.7K
	b	-5	2A1A5XDS3-1	150 ± 15
	c	-5	2A1A5XAS-8	Zero
	d	-16	-14	Less than 1
	e	-24	-3	Zero
	f	-24	-13	Zero
	g	-24	2A1A5XDS3-2	Zero
	h	-35	2A1A5XA3-15	Zero
4	a	2A1A5P1-7	2A1A5J4	1.1M ± 56K
	b	-7	2A1A5XA4-7	Zero
	e	-7	2A1ASXDS4-1	470 ± 47



Section	Step	Connect multimeter leads between		Multimeter indication (ohms)
		pin	and pin	
	d	-7	2A1A5XA4-13	Zero
	e	-7	2A1A5P1-	Zero
	f	-18	2A1A5XA4-14	Less than 1
	g	-26	2A1A5XA4-8	Zero
	h	-26	2A1A5XD84-2	Zero
	i	-27	2A1A5P1-26	Zero
	j	2A1A5P1-37	2A1A5XA4-15	Zero

**3-16. Isolating Troubles In Plate Assembly 2A16**

*a. Preparation of R-1467/GRC-14.*

(1) Remove components 2A4, 2A6, 2A7, 2A8, 2A10, 2A11, 2A12, and 2A18 (TM 11-5820-95-12).

(2) Remove plug 2A16W1P1 (fig. 8-18) from jack 2A15W2J1 (fig. 8-19).

*b. Procedure.*

(1) Refer to the chart (c below). Connect the multimeter leads between the two pins of the listed steps of sections that were referenced in the

troubleshooting chart (para 8-12b). If the troubleshooting chart indicates a section but does not give a step number, perform all of the steps given in that section starting with step a.

(2) Observe that multimeter indication is within the tolerance specified in the chart for each step. If it is not, refer to the R-4467/GRC-144 interconnecting diagram (fig. 5-21) and determine whether the fault is defective wiring or a defective circuit element.

*c. Pate Assembly 2A18 Checks Chart.*

Section	Step	Connect multimeter leads between		Multimeter indication (ohms)	
		pin	and pin		
1	a	2A16XA7-8	2A16W1P1-C	Less than 1	
	b	-4	-D	Less than 1	
	c	-5	-J	Less than 1	
	d	-8	-T	Less than 1	
	e	-9	-U	Less than 1	
2	a	2A16W1XA8-5	2A16W1P1-J	Zero	
	b	-8	-i	Zero	
	c	-9	-k	Zero	
3	a	2A24XA10-1	2A16W1P1-A	Less than 1	
	b	-2	-B	Less than 1	
	c	-5	-J	Less than 1	
4	a	2A16W1XA5-3	2A16W1P1-C	Less than 1	
	b	-4	-D	Less than 1	
	c	-5	-J	Less than 1	
	d	-6	2A16W1XA5-15	Zero	
	e	-7	2A15W1P1-j	Zero	
	f	-8	-R	Zero	
	g	-9	-P	Zero	
	h	-10	-S	Zero	
	i	-11	2A16W1P1-W	Zero	
	j	-12	2A16W1XA12A-6	Zero	
	k	-14	2A16W1XA12A-7	Zero	
	5	a	2A16W1XA13-1	2A10W1P1-A	Zero
		b	-2	-B	Zero
c		-4	-J	Zero	
d		-9	-N	Zero	
6	a	2A16XA4-3	2A16W1P1-C	Less than 1	
	b	-4	-D	Less than 1	
	c	-5	-J	Less than 1	
7	a	2A16W1XA11-3	2A16W1P1-C	Zero	
	b	-4	-D	Zero	
	c	-5	-J	Zero	
	d	-9	2A16W1XA12A-13	Zero	

Section	Step	Connect multimeter leads between		Multimeter indication (ohms)
		pin	and pin	
8	a	2A16W1XA12A-6	2A16W1P1-J	Zero
	b	-6	2A16W1XA5-12	Zero
	c	-7	2A16WIXAS-14	Zero
	d	-12	2A16W1P1-V	Zero
	e	-18	2A16W1XA11-9	Zero
	f	-17	2A16W1P1-K	Zero
9	a	2A16W1XA12B-1	2A16W1P1-G	Zero
	b	-2	-H	Zero
	c	-5	-J	Zero
	d	-6	-f	Zero
	e	-7	-e	Zero
	f	-8	-b	Zero
	g	-9	-a	Zero
	h	-10	-Z	Zero
	i	-11	-Y	Zero
	j	-14	-d	Zero
	k	-15	-c	Zero
	l	-16	-E	Zero
	m	-17	-F	Zero
	n	-29	-g	Zero
o	-30	-h	Zero	

**3-17. Isolating Troubles In Electrical Equipment Cabinet 2A15**

**WARNING**

**115 vac is present in R-1467(P)/GRC-144(V) Do not perform any of the continuity or resistance checks given in this paragraph while the equipment is connected to the primary power source.**

*a. Preparation of R-1467(P)/GRC-144(V).*

(1) Remove power supply 2A1 (para 3-40).

(2) Remove electrical frequency synthesizer 2A14 (para 3-49).

(3) Disconnect plug 2A15W2P2 (fig. 3-19) from J3 on rear of tunnel diode amplifier 2A2. Disconnect plug 2A16W1P1 (fig. 3-18) from jack 2A15W2J1, (fig. 3-19).

*b. Procedure.*

(1) Refer to the chart (c below). Connect the multimeter leads between the two pins of the listed steps of the sections that were referenced in the troubleshooting chart (para 3-12b). If the troubleshooting chart indicates a section but does not give a step number, perform all of the steps given in that section starting with step a.

(2) Observe that multimeter indication is within the tolerance specified in the chart for each step. If it is not, refer to the R-1467(P)/GRC-144(V) interconnecting diagram (fig. 5-21) and determine whether the fault is defective wiring or a defective circuit element.

*c. Electrical Equipment Cabinet 2A15 Checks Chart.*

Section	Step	Connect multimeter leads between		Multimeter indication (ohms)
		pin	and pin	
1	a	2A15W2J1-A	2A15W2XA1-1	Zero
	b	-B	-20	Zero
	c	-C	-3	Zero
	d	-D	-22	Zero
	e	-E	-5	Zero
	f	-F	-24	Zero
	g	2A15W2J1-G	2A15W2XA1-7	Zero
	h	-H	-26	Zero
	i	-J	2A15E2 (CAB GRD)	Zero
	j	-N	2A15A2S1B-15	Less than 1K
	k	-P	2A15A2S1A-17	Zero
	l	-R	2A15AS1B-17	Zero
	m	-S	2A15AS1B-23	Zero
	n	-T	2A15AS1B-19	Zero
	o	-U	2A15AS1A-21	Zero
	p	-V	2A15AS1B-25	Less than 1K

Section	Step	Connect multimeter leads between		Multimeter indication (ohms)
		pin	and pin	
2	q	-W	2A15A6J3-B	Less than 1
	r	-Y	2A16A2XDS2-C	Zero
	s	-Z	2A15A2XDS2-B	Zero
	t	-a	2A15A2DS2-D	Zero
	u	-b	-B	Zero
	v	-c	2A15A2XDS6-D	Zero
	w	-d	2A15A2XDS6-A	Zero
	x	-e	2A15A6J2-B	Less than 1
	y	-f	2A15A6J2-A	Less than 1
	z	-g	2A15A2XDS6-C	Zero
	aa	2A15W2J1-h	2A15A2XDS6-B	Zero
	ab	-i	2A15A2S1A-11	Less than 50K
	ac	-j	2A15A6J3-A	Less than 1
	ad	-k	2A15A2S1A-13	Less than 50K
	e	2A15W2P2-A	2A15A6J3-A	Zero
	b	-B	2A15A2S2-1	Zero
	c	-C	2A15A2XDS1-2	Zero
	d	-D	-1	Zero
	e	-E	2A1SW2XA-4	Zero
	f	-F	-23	Zero
3	a	2A15W2XA14-A1	2A15A2S1B-9	Zero
	b	-1	2A15A2XDS10-2	Zero
	c	-2	2A15E2 (CAB GRD)	Zero
	d	-6	2A15E2 (CAB GRD)	Zero
	e	-5	2A15AZS2-3	Zero
	f	-4	-1	Zero
	g	-7	2A15W2J1-K	Zero
	h	-9	2A15A2S2-3	Zero
	i	-10	-1	Zero
	4	a	2A15A2J6	2A15A2S1A-29
5	b	2A15A2J6	2A15A2S 1B-1	Zero
5	a	2A15W2XA1-8	2A15A2XDS6-G	Zero
	b	-8	2A16AXDIS10-1	Zero
	c	-8	2A15A2XDS2-G	Zero

**3-18. Indicator, Antenna Alignment ID-1708/GRC Troubleshooting Procedures**

Troubleshooting Indicator, Antenna Align ID-1708/GRC consists of performing continuity checks and checking the calibration accuracy of meter 3M1 (fig. 3-25). Use

the Indicator, Antenna Alignment ID-1708/GRC wiring diagram to perform the continuity checks and refer to paragraph 3-67 for the calibration procedure for meter 3M1. Replacement procedures for parts in Indicator, Antenna Alignment ID-1708/GRC are given in paragraph 3-53.

**3.18.1. Converter Multiplier CV-3633/GRC 144(V) Troubleshooting Chart**

**WARNING**

**115 Vac is present in Converter-Multiplier CV-3633/GRC-144(V). Do not remove or replace parts, nor perform continuity or resistance checks while primary power is applied to Radio Set AN/GRC-144(V)4.**

144(V) troubleshooting chart (b below) supplements the operational checks and corrective measures contained in TM-11-5820-695-12. If the operational checks and corrective measures in below) supplements the operational TM-11-5820-695-12 fail to correct the trouble or indicates that higher category maintenance is required, apply the corrective action in the chart below. To use the chart, read down the Symptom column of the troubleshooting chart until the abnormal symptom or condition is found. Perform the corrective actions indicated in the chart until the abnormal symptom or condition is corrected.

Figure 3-25.1 is a parts location diagram which will aid the maintenance person in locating parts.

- a. *Use of the Chart.* The CV-3633/ GRC-
- b. *Converter-Multiplier CV-3633/GRC-144(V) Troubleshooting Chart.*

<i>Item No.</i>	<i>Symptom</i>	<i>Probable trouble</i>	<i>Corrective actions</i>
1	POWER 1.5 AMP-SLO BLO fuse blows when replaced.	<ul style="list-style-type: none"> <li>a. Defective component or wire in primary power distribution circuits or amplifier-multiplier 3A5.</li> <li>b. Defective electrical equipment chassis 3A7.</li> <li>c. Defective component or wire An amplifier multiplier 3A5.</li> <li>d. Defective amplifier-multiplier heater HR1.</li> </ul>	<ul style="list-style-type: none"> <li>a. Remove amplifier-multiplier 3A5 (TM 11-5820-695-12) from electrical equipment chassis 3A7. Insert replacement fuse and then set POWER ON/OFF switch on status panel 3A8 to ON. If replacement fuse blows, proceed to step b below. Otherwise proceed to c and d below to isolate the fault.</li> <li>b. Perform the CV-3633/GRC-144(V) primary power distribution checks (para 3-18.2c sections 3a, b and c).</li> <li>c. Use the TS-352B/U to check amplifier-multiplier 3A5 wiring.</li> <li>d. Use the TS-352B/U to check its resistance as follows: 3A5P1 pin 1 to pin 2 should be <math>176 \pm 18</math> ohms.</li> </ul>

<i>Item No.</i>	<i>Symptom</i>	<i>Probable trouble</i>	<i>Corrective actions</i>
2	POWER 2 AMP SLO-BLO fuse blows when replaced.	<p>a. Defective component or wire in primary power distribution circuits or power supply 3A6.</p> <p>b. Defective electrical equipment chassis 3A7 or transformer 3A7T1.</p> <p>c. Defective component or wire in power supply 3A6.</p>	<p>a. Remove power supply 3A6 (TM-11-5820-695-12) from electrical equipment chassis 3A7. Insert replacement fuse and then set POWER ON/OFF switch on status panel 3A8 to ON. If replacement fuse blows, proceed to b below. Otherwise proceed to c to isolate the fault.</p> <p>b. Perform the CV-3633/GRC-144(V) primary power distribution checks ( 3-18.2c sections 3a, 4a through 5j.-</p> <p>c. Use the TE-352B/U to check power supply 3A6 wiring.</p>
3	All indicators on STATUS PANEL 3A8 not lighted except FREQUENCY BAND IN USE indicator	<p>a. Defective status panel 3A8 POWER ON/OFF SWITCH.</p> <p>b. Defective status panel connector 3A8J1.</p>	<p>a. Replace status panel power switch 3A8S1 (fig. 5-118).</p> <p>b. Replace status panel connector 3A8J1. Refer to paragraph 3-6 and perform the T-1054(P)A/GRC-144 (V) troubleshooting procedures.</p>
4	FREQUENCY BAND IN USE indicator on STATUS PANEL 3A8 not lighted.	<p>a. T-1054(P)A/GRC-144 POWER ON/OFF switch or primary power distribution circuits.</p> <p>b. Shelter mounted wave-guide switches.</p>	<p>a. Refer to paragraph 3-6 and perform the T-1054(P)A/GRC-144 (V) troubleshooting procedures.</p> <p>b. Use the inter connecting diagrams in TM 11-5820-695-12 and TS-352B/U to check wiring between the wave-guide switches and T-1054(P)A/GRC-144 (v).</p>

<i>Item No.</i>	<i>Symptom</i>	<i>Probable trouble</i>	<i>Corrective actions</i>
5	ALARM SUMMARY indicator on STATUS PANEL 3A8 lighted red and all other indicators green.	<p>a. One of monitored signals out of range: forward power from A5, oscillator power from A2, or reflected power from CR1.</p> <p>b. One of alarm monitor 3A1 monitor circuits improperly calibrated.</p>	<p>a. Determine which signal is defective by performing component test point checks for 3A5TP1 PWR, 3A2TP1 LO PWR, and 3A2TP2 REFL PWR (TM 11-5820-695-12). Replace 3A5, 3A2 or CR1 according to result of check. If all are within range, proceed to b below.</p> <p>b. Perform the threshold alarm adjustment procedure for 3A1 (TM 11-5820-695-12). If defect still present, replace 3A1.</p>
6	AIR FLOW indicator on STATUS PANEL 3A8 lighted red.	<p>a. Inadequate air flow in unit 3.</p> <p>b. Switch 3A7S1 or 3A7S2 defective.</p>	<p>a. Check air flow and blower 2A15B81 according to procedure in TM 11-5820-695-12.</p> <p>b. Use TS-352B/U to check voltages and wiring. Replace either switch if defective.</p>
7	TEMP indicator on STATUS PANEL 3A8 lighted red, and AIR FLOW indicator lighted green.	Amplifier-multiplier 3A5 defective.	Replace 3A5.
8	OSC TEMP indicator on STATUS PANEL 3A8 not lighted.	Oscillator 3A2A3 defective.	Replace converter 3A2.
9	Out of range meter indication obtained for component test point check.	<p>a. Power supply 3A6 defective -</p> <p>b. Defective module.</p>	<p>a. Replace 3A6.</p> <p>b. Replace module corresponding to failed test point check.</p>

**3-18.2. Isolating Troubles in CV-3633/GRC-144(V) Primary Power Distribution Circuits**

**WARNING**

115 vac is present in the CV-3633/GRC-144(V). Do not perform any of the continuity or resistance checks given in this paragraph while the equipment is connected to the primary power source.

a. *Preparation of the CV-3633/GRC-144TV).*

(1) Remove connector plug from Converter-Multiplier CV-3633/GRC-144 (V) J1 AC PWR Connector.

(2) Remove status panel 3A8.

c. *CV-3633/GRC-144(V) Primary Power Distribution Checks.*

(3) Remove the CV-3633/GRC-144(V) connector plug P1 from Receiver, Radio R-1467(P)A/GRC-144(V) J5 AC INPUT connector.

(4) Remove alarm monitor 3A1, converter frequency electronics 3A2, amplifier-multiplier 3A5 and power supply 3A6.

b. *Procedure.*

(1) Refer to the chart (c below) and connect the multimeter leads between the two pins referenced (fig. 5-108).

(2) Observe that multimeter indication is within the tolerance specified in the chart for each step. If it is not, refer to the CV-3633/GRC-144(V) interconnecting diagram (fig. 5-98) and primary power distribution diagram (fig. 2-29).

Section	Step	Connect multimeter leads between		Multimeter indication (ohms)
		pin	and pin	
1	a.	3A7J1-A	3A7P1-A	Zero
	b.	-B	-B	Zero
	c.	-C	-C	Zero
2	a.	3A7P1-A	3A7P2-A1	Zero
	b.	-B	-A3	Zero
	c.	-C	-A4	Zero
3	a.	3A7P2-A5	3A7P2-A8	Less than 1
	b.	-A5	3A7XA5-2	Zero
4	c.	3A7P2-A6	3A7XA5-1	Zero
	a.	3A7XA6A-1	3A7XA6-A3	Zero
	b.	3A7XA6A-2	3A7XA6-A4	Zero
	c.	-7	-10	Zero
	d.	-8	-11	Zero
5	e.	-9	-12	Zero
	a.	3A7XA6A-1	3A7XA6A-2	Less than 1
	b.	-3	-4	Less than 1
	c.	-7	-8	Less than 1
	d.	-10	-11	Less than 1
	e.	-8	-9	Less than 1
	f.	-11	-12	Less than 1
	g.	3A7XA6A-7	3A7XA6A-9	Less than 1.5
	h.	-10	-12	Less than 1.5
	i.	-5	-6	Less than 1.2
j.	-14	-15	Less than 1.2	

Section	Step	Connect multimeter leads between		Multimeter indication (ohms)
		pin	and pin	
6	a.	Chassis E1		Zero
	b.		3A7J1-B	Zero
	c.		3A7P1-B	Zero
	d.		3A7J2-K	Zero
	e.		3A7P2-A3	Zero
	f.		3A7J3-K	Zero
	g.		3A7P3-K	Zero
	h.		3A7XA5-11	Zero
	i.		3A7XA6B-9	Zero
	1-		3A7XA1-4	Zero
	k.		3A7XA2-5 3A7P4-15	Zero

**3-18.3. Isolating Troubles in CV-3633/GRC-144(V) DC Power Distribution Circuits**

**WARNING**

115 vac is present in the CV-3633/GRC-144(V). Do not perform any of the continuity or resistance checks given in this paragraph while the equipment is connected to the primary power source.

*a. Preparation of CV-3633/GRC-144(V).*

(1) Remove connector plug from Converter-Multiplier CV-3633/GRC-144(V) J1 AC PWR connector.

(2) Remove power supply 3A6 and alarm monitor.

(3) Remove electronic frequency converter 3A2 and amplifier-multiplier 3A5.

(4) Remove status panel 3A8.

*b. Procedure*

(1) Refer to the chart (c below). Connect the multimeter leads between the two pins referenced (fig. 5-108).

(2) Observe that multimeter indication is within the tolerance specified in the chart for each step. If it is not, refer to the CV-3633/GRC-144(V) interconnecting diagram (fig. 5-98) and DC power distribution diagram (fig. 3-20) and determine whether the fault is defective wiring or a defective circuit element.



c. CV-3633/GRC-144(V) DC Power Distribution Checks.

Section	Step	Connect multimeter leads between		Multimeter indication (ohms)
		pin	and pin	
1	a.	3A7XA6B-1	3AXA5-5	Zero
	b.		3A7XA1-27	Zero
	c.		3A7XA2-3	Zero
	d.		3AP4-1	Zero
	e.		3A7TB4-3	Zero
	f.		3A7TB4-4	Zero
2	a.	3A7XA6B-2	3A7XA5-6	Zero
	b.		3A7XA1-8	Zero
	c.		3A7XA2-4	Zero
	d.		3A7P4-2	Zero
	e.		3A7TB4-1	Zero
	f.		3A7XA5-3	Zero
3	a.	3A7XA6B-5	3A7XA5-3	Zero
	b.	3A7XA6B-6	3A7XA5-4	Zero

**3-18.4. Isolating Troubles in Electrical Equipment Chassis 3A7.**

**WARNING**

**115 vac is present in CV-3633/GRC-144(V). Do not perform any of the continuity or resistance checks given in this paragraph while the equipment is connected to the primary power source.**

*a. Preparation of CV-3633/GRC-144(V).*

(1) Remove connector plug from Converter-Multiplier CV-3633/GRC-144(V) J1 AC PWR connector.

(2) Remove connector plugs from the CV-3633/GRC-144(V) Equip INTCON connectors J2 and J3.

(3) Remove status panel 3A8.

(4) Remove the CV-3633/GRC-144(V) connector plugs P1 and P3 from Receiver, Radio R-1467(P)A/GRC-144(V) connectors J5 AC POWER INPUT and J2 EQUIPMENT INTERCONNECT respectively.

(5) Remove the CV-3633/GRC-144(V) alarm monitor 3A1, electronic frequency converter 3A2, amplifier multiplier 3A5 and power supply 3A6.

*b. Procedure.*

(1) Refer to the chart (c below). Connect the multimeter leads between the two pins referenced (fig. 5-108).

(2) Observe that multimeter indication is within the tolerance specified in the chart for each step. If it is not, refer to the CV-3633/GRC-144(V) interconnecting diagram (fig. 5-98) and determine whether the fault is defective wiring or a defective circuit element.

c. Electrical Equipment Chassis 3A7 Checks Chart.

Section	Step	Connect multimeter leads between		Multimeter indication (ohms)
		pin	and pin	
1	a.	3A7J2-A	3A7XA1-36	Less than 1
	b.	-A	3A7P4-10	Less than 1
2	a.	3A7J2-E	3A7P4-11	Less than 1
	b.	-E	3A7J2-A	NOTE Place positive multimeter lead on 3A7J2-A Greater than 500 NOTE Place positive multimeter lead on 3A7J2-E
3	c.	-E	3A7J2-A	Less than 1000
	a.	3A7J2-B	3A7XA1-17	Less than 1
	b.	3A7J2-C	3A7XA1-37	Less than 1
	c.	3A7J2-F	3AJ2-V	Less than 1
	d.	3A7J2-F	3A7P4-12	Less than 1
	e.	-G	-13	Less than 1
	f.	3A7J2-H	3A7J2-W	Less than 1
	g.		3A7P4-14	Less than 1
	h.	3A7J2-L	3A7J2-M	Less than 1
	i.	-N	-P	Less than 1
	j.	-R	-S	Less than 1
4	k.	-T	-U	Less than 1
	a.	3A7J3-A	3A7P3-A	Less than 1
5	b.	-B	-B	Less than 1
	a.	3A7XA5-7	3A7XA1-33	Less than 1
	b.	-7	3A7P4-3	Less than 1
6	c.	-8	-4	Less than 1
	d.	-9	3A7XA1-26	Less than 1
	a.	3A7XA1-12	3A7P4-7	Less than 1
	b.	3A7XA1-13	3A7P4-8	Less than 1
	c.	-14	3A7TB4-2	Less than 1
	d.	-16	3A7P4-9	Less than 1
	e.	-25	3A7XA2-8	Less than 1
f.	-32	3A7P4-6	Less than 1	
	g.	3A7XA2-7	-5	Less than 1

## Section III. REPAIRS

**NOTE**

**For all removal and replacement of units listed in the procedures not described below refer to TM-11-5820-695-12.**

**3-19. General Parts Replacement Techniques**

Most parts in AN/GRC-144 Radio Sets are readily accessible and can be replaced without special procedures. The procedures required to remove or replace piece parts and nonrepairable assemblies which are not obvious or require the removal of one or more parts are given in paragraphs 3-20 through 3-27 (Transmitter, Radio T-1054(P)/GRC-144(V) Repairs), 3-38 through 3-52 (Receiver, Radio R-1467 (P)A/GRC-144 Repairs), 3-53 (Indicator, Antenna Alignment ID-1708/GRC Repairs) and 5-53.1 (Converter-Multiplier CV3633/GRC-144(V) Repairs). The following precautions apply when removing, replacing, or repairing parts in AN/GRC-144(V) Radio Set.

**NOTE**

**For Radio Set AN/GRC-144 (V)4, refer to paragraph 3-53.1 and set the Converter-Multiplier CV-3633 /GRC-144(V), status panel 3A8 POWER ON/OFF switch 3A851 to OFF.**

*a.* Before removal or replacement of any part, unless otherwise stated, remove power from the unit using the procedures in paragraph 3-20a or 3-38a. Similarly, restore power to the unit (para 3-20b or 3-38b) after the part has been replaced.

*b.* Exercise care when removing or replacing rigid coaxial cables. Detailed procedures are provided in TM-11-5820695-12 for removal and replacement of rigid coaxial cables.

*c.* Tag all hardware and components during removal procedures for correct identification during replacement procedures. Before a part is unsoldered, note the position of the leads. If the part has several leads, tag each of the-leads, before unsoldering any of them.

*d.* When removing a defective part, be careful not to damage leads or other parts by pulling or pushing them out of the way.

*e.* Whenever replacing a part, install the new part in the same position as the original. Use an exact duplicate whenever possible.

*f.* After a part has been replaced, perform the testing procedures provided in section V of this chapter to check that the equipment is operating properly.

*g.* Use a pencil-type soldering iron with a 25 watt maximum heating capacity. If the iron must be used with ac, use an isolating transformer between the iron and the ac line. Do not use a soldering gun; damaging voltages can be induced in the equipment parts.

*h.* If wiring must be replaced, use leads of the same length and gauge if possible. With the exception of harness cabling, run the leads in the same manner as the original wiring. For harness cabling, cut the old conductor as short as possible without removing it from the harness. Dress the new conductor along the harness and spot tie it to the outside of the harness. Make connections to same terminals used in the original wiring, even where there are alternatives which appear electrically equivalent.

*i.* Make well-soldered connections, using no more solder than is necessary. A carelessly soldered connection may create a new fault and is one of the most difficult, faults to find.

*j.* Do not allow drops of solder to fall into the unit. Do not allow a soldering iron to come into contact with insulation or parts that might be injured by excessive heat.

*k.* Do not disturb the setting of any uncalibrated control without redetermining its proper setting before returning the equipment to service. If any switches are operated, return them to their original positions.

### 3-20. Transmitter, Radio T-1054(P)/GRC144(V) and T-1054(P)A/GRC-144(V) Repairs

Procedures required to remove or replace parts which are not obvious or require special handling are given in paragraph 3-21 through 3-37. Prior to removal or replacement of any part in the T-1054 (P)/GRC-144(V) or T-1054(P)A/GRC-144(V) the procedures for power removal given in paragraph 3-20a unless otherwise stated, must be performed. Procedures for restoring power are given in paragraph 3-20b. Procedures for removal and replacement of components with rigid coaxial cables are covered in TM 11-5820-696-12.

#### a. Remove Power.

(1) Set the POWER ON/OFF switch on meter panel assembly 2A15A2 to OFF (fig. 3-17).

(2) Set the POWER ON/OFF switch on meter panel assembly 1A15A8 to OFF (fig. 3-1).

(3) Disconnect the external ac power source cable from AC POWER INPUT connector 1A15A6J18 located on the top rear section of the electrical equipment cabinet 1A15 (fig. 3-7).

#### b. Restore Power.

(1) Reconnect the external ac power source cable to AC POWER INPUT connector 1A15A6J18 located on top rear section of electrical equipment cabinet 1A15.

(2) Set the POWER ON/OFF switch on meter panel assembly 1A15A8 to ON.

(3) Make the following checks on T-1054(P)/GRC-144(V) :

(a) The 5 AMP SLO-BLO neon fuse indicator on meter panel assembly 1A15A8 is not lighted.

(b) All power supply 1A1 indicator lamps are lighted green.

(c) 5V and 28V indicator lamps on electrical frequency synthesizer 1A14 are lighted green.

(4) Set the POWER ON/OFF switch on meter panel assembly 2A15A2 to on (fig. 3-17).

(5) Make the following checks on R1467/GRC-144:

(a) The SLO-BLO POWER 5 AMP and TDA 1 AMP neon fuse indicators on meter panel assembly 2A15A2 are not lighted.

(b) All power supply 2A1 indicator lamps are lighted green.

(c) 5V and 28V indicator lamps on electrical frequency synthesizer 2A14 are lighted green.

#### NOTE

**Radio communications can normally be established 5 to 10 minutes after AN/GRC-144(V) Radio Sets are turned on if the ambient temperature in the shelter is maintained above +70° Fahrenheit.**

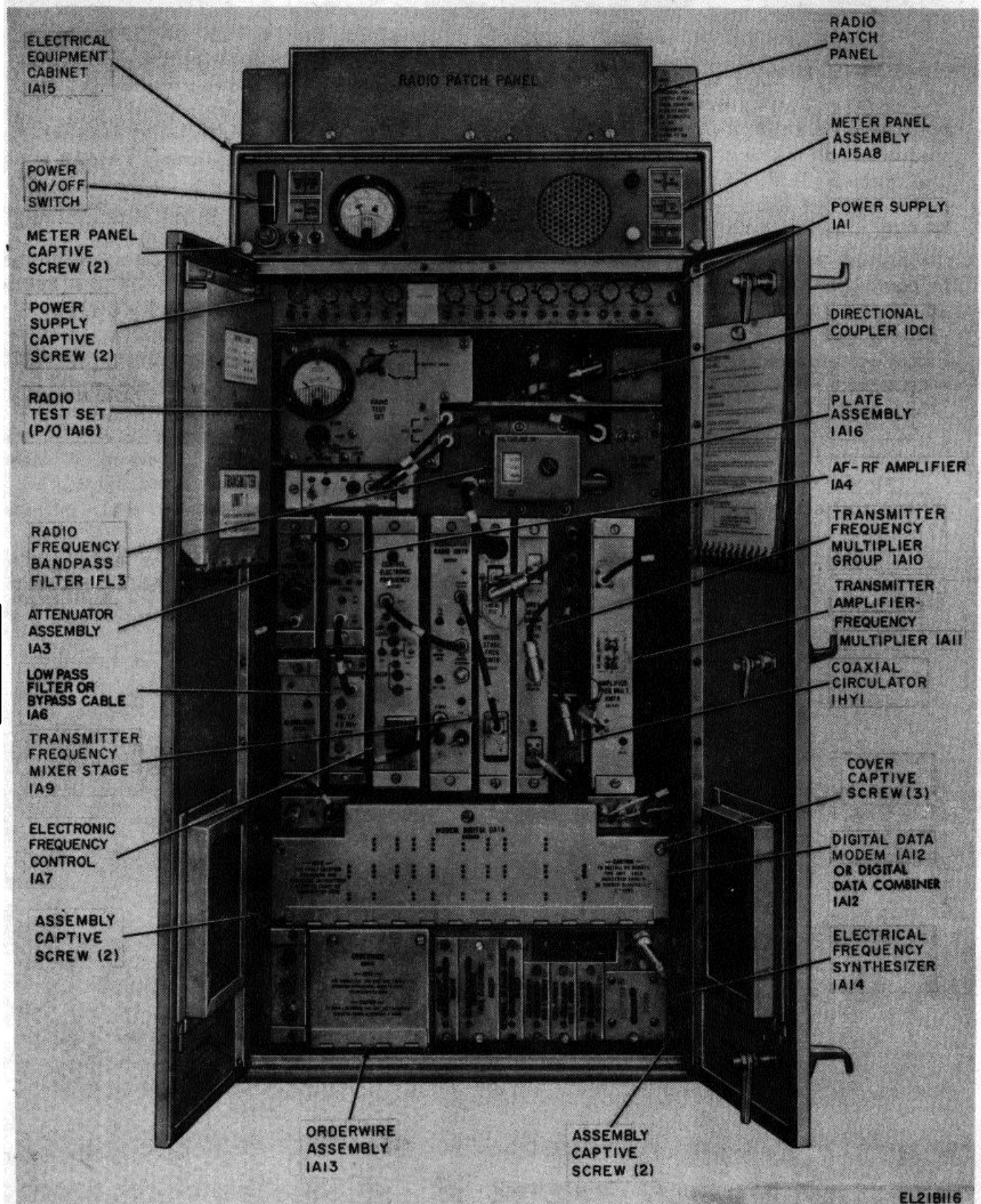


Figure 3-1. Transmitter, Radio T-1054(P)/GRC-144(V) and T-1054(P)/GRC-144(V) parts location.

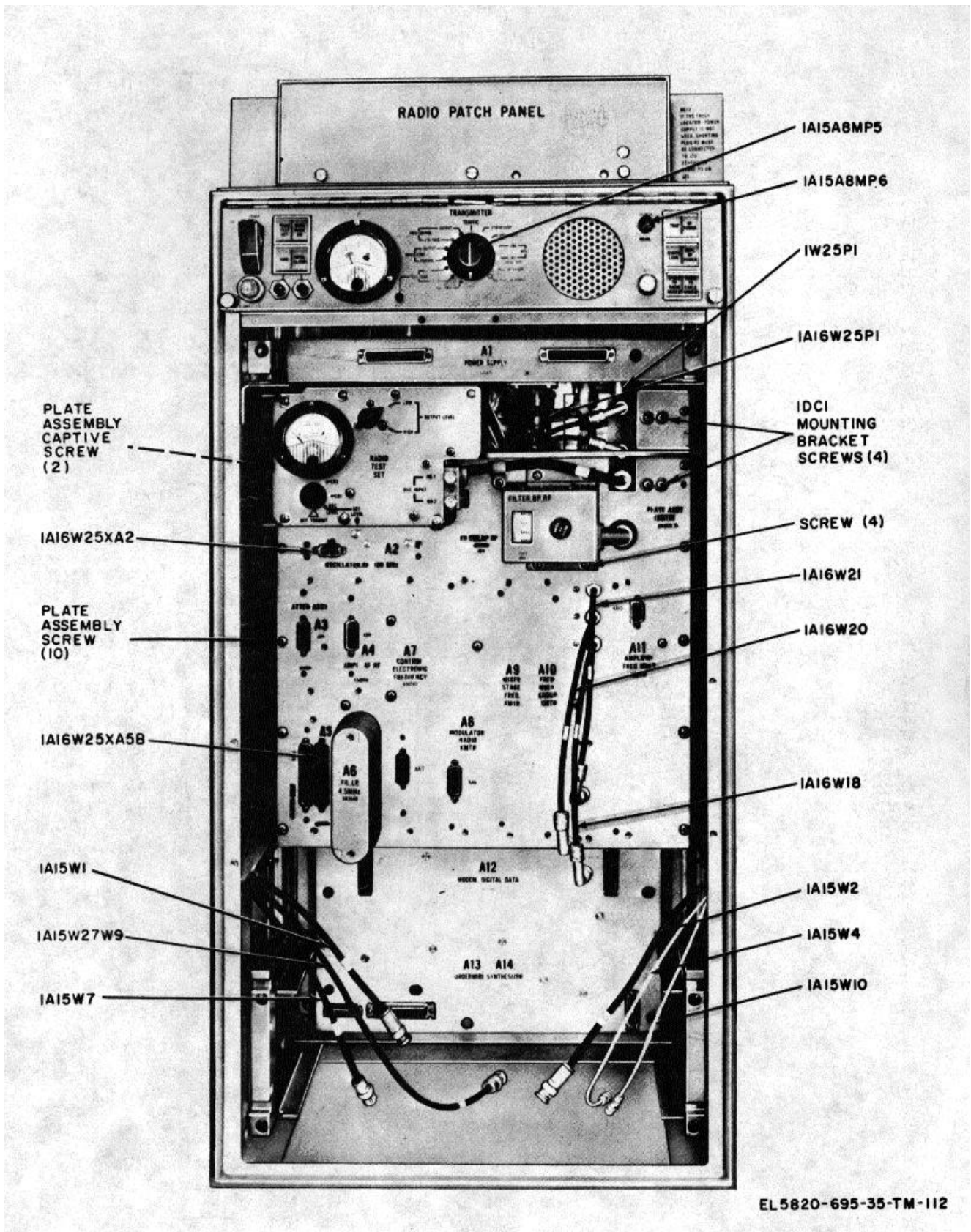
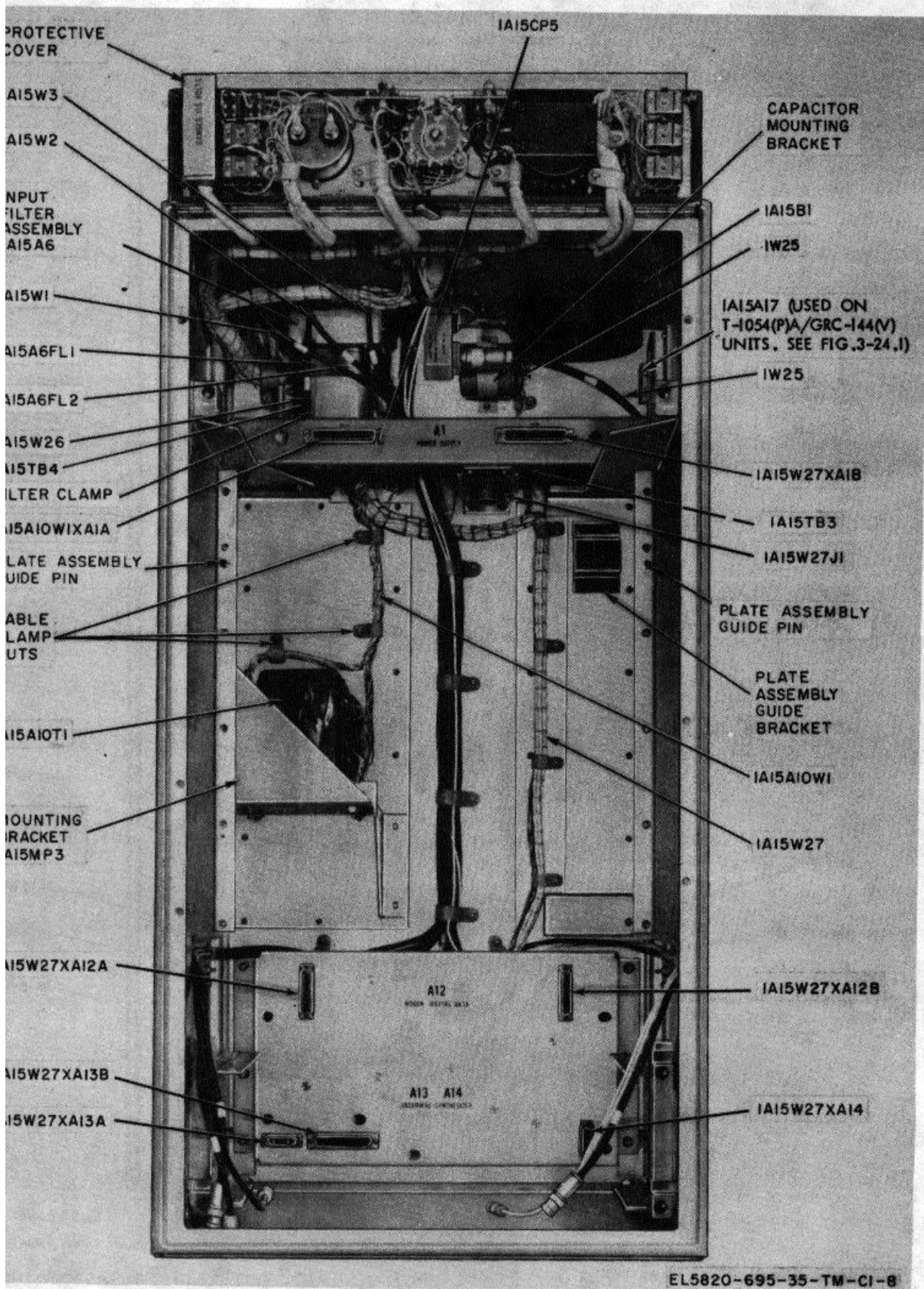


Figure 3-2. Electrical equipment cabinet 1A15, partially disassembled, parts location.





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Figure 3-3. Electrical equipment cabinet 1A15, front view with plate assembly 1A16 removed, parts location.

### 3-20.1 Removal and Replacement of Air Filters

T-1054/GRC-144 is equipped with three air filters, as is equipment R-1467/GRC-144. Two air filters are located inside the electrical equipment cabinet (1A15 or 2A15), one on each of the two doors (Fig. 3-1,3-3.1). A third filter is mounted on top of the cabinet.

a. Door Mounted Air Filters To remove or replace a door mounted air filter proceed as follows:

(1) Lift and turn the three cabinet door latch handles and open the two cabinet doors.

(2) If the air filter is seated in a retaining frame merely slide the filter upward and remove from the frame. If the filter is retained by six captive screws, first loosen the screws and then slide the filter upward to remove (Fig. 3-3.1).

(3) If the air filter is to be cleaned, use a solution of water and detergent. Allow to dry before replacing. (4) Insert cleaned or replacement filter into the retaining frame. If the filter is retained by six captive screws, tighten the screws loosened in (2). (5) Close and latch the two cabinet doors.

b. Cabinet Mounted Air Filters To remove or replace the air filter mounted on top of the electrical equipment cabinet 1A15 (Fig 3-7) or 2A15 (Fig 3-20) proceed as follows.

(1) Set POWER ON-OFF switch on the meter panel assembly 1A15A8 or 2A15A2 to OFF.

(2) Loosen lint, do not remove the facer air filter screws securing the air filter to the top of the electrical equipment cabinet.

(3) Remove air filter.

(4) If the filter is to be cleaned, use a solution of water and detergent. Allow to dry before replacing.

(5) Place the cleaned or replacement filter on top of the electrical equipment cabinet, aligning the four screw holes. Tighten the screws.

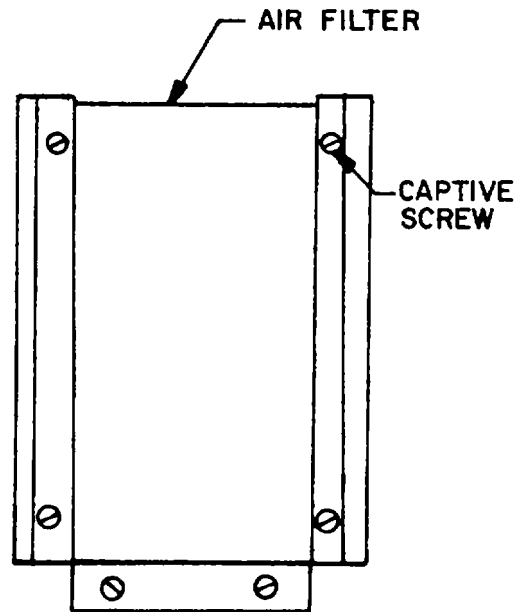


Figure 3-3.1. Door mounted air filter removal.



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**Change 5 3-34.2**

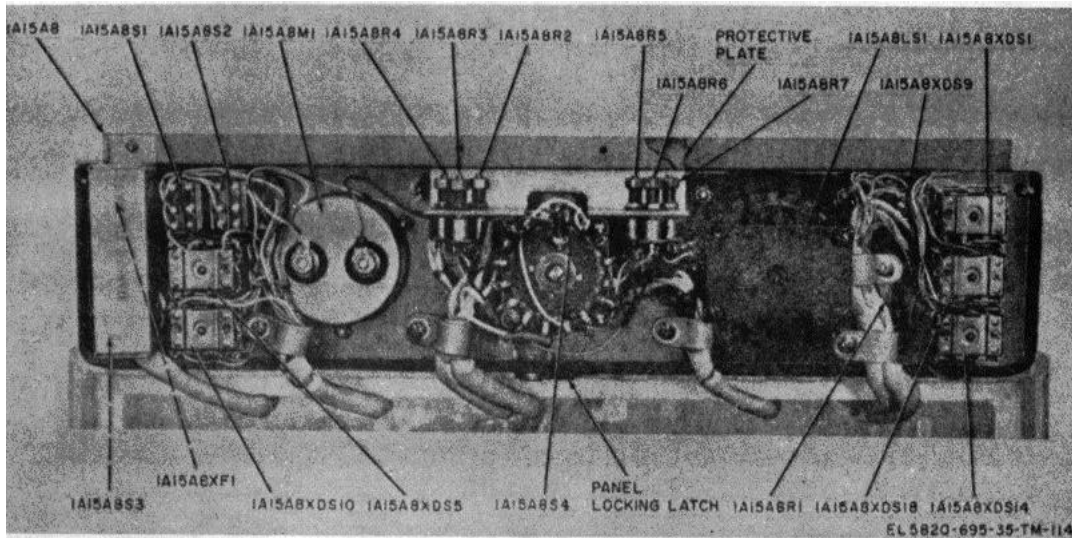


Figure 3-4. Meter panel assembly 1A15A8, rear view, parts location.

**3-21. Replacement of Parts on Meter Panel Assembly 1A15A8 (fig. 3-4)**

Prior to removing and replacing parts on meter panel assembly 1A5A8, perform the procedures listed in paragraph 3-20a to remove equipment power. After a part is replaced, perform the procedures in paragraph 3-20b to restore equipment power.

*a. Replacement of Meter 1A15A8M1.*

(1) *Removal.*

(a) Loosen the two meter panel captive screws (fig. 3-1).

(b) Swing the meter panel assembly 1A15A8 upward and lock it in an upright position by use of the panel locking latch (fig. 3-4).

(c) Remove the two nuts and washers from the meter terminals.

(d) Tag and remove the wire lugs connected to the meter terminals.

(e) Release the meter panel assembly 1A15A8 and position it downward until it is perpendicular to electrical equipment cabinet 1A15. Support or tie meter panel assembly 1A15A8 in the perpendicular position.

(f) Remove and save the three locknuts and screws that secure meter 1A15A8M1 to meter panel assembly 1A15A8.

(g) Remove the meter from the meter panel assembly.

(2) *Replacement.*

(a) Position the new meter 1A15A8M1 in place on meter panel assembly 1A15A8 and align the meter mounting holes with those of the panel assembly.

(b) Secure the meter in place with the three locknuts, screws, and washers removed in step (1) (g) above.

(c) Position the meter panel assembly 1A15A8 upward and lock in position using the panel locking latch.

(d) Remove the two nuts, washers, and shorting bar from the new meter terminals.

(e) Connect the wire lugs removed in step (1)(d) above to their respective meter terminals and fasten lugs to terminals with nuts and washers removed in (1)(c) above.

(f) Place the shorting bar removed from the new meter on the terminal lugs of the old meter and fasten in place with its terminal hardware.

(g) Release the meter panel assembly 1A15A8 and position it downward until it rests against electrical equipment cabinet 1A15.

(h) Secure the meter panel assembly 1A15A8 in place by finger tightening the two meter panel captive screws.

(i) Calibrate transmitter meter 1A15A8M1 (para 3-55).

*b. Replacement of Indicator Light Assembly 1A14A8XDS1, XDS5, XDS10, XDS14, or XDS18 (fig. 3-4).*

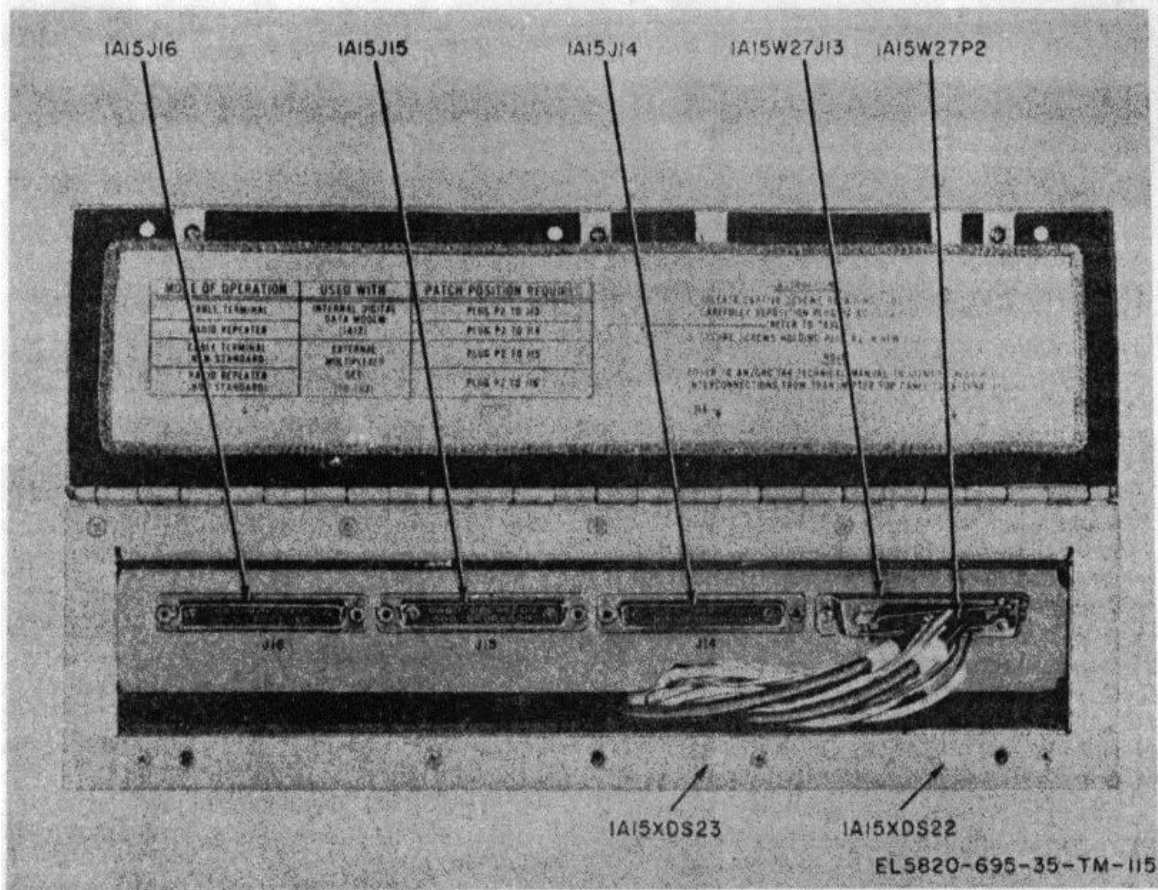


Figure 3-5. Radio patch panel (p/o 1A15).front interior view, parts location

(1) *Removal.*

(a) Using fingernail slots on sides of lens assembly, pull lens assembly out approximately 5/8" (A, fig. 3-8).

(b) Rotate lens assembly 90°.

(c) Push lens inward against lens assembly to release tension on index keys, then pull complete lens assembly out (D, fig. 3-8).

(d) Unscrew two screws (C, fig. 3-8) until the captive nuts reach rear of their travel range releasing housing from cover.

(e) Loosen the two meter panel captive screws (fig. 3-1).

(f) Swing the meter panel in an upright position and lock it in position with the panel locking latch (fig. 3-4).

(g) Tag, unsolder, and remove the wires connected to the indicator light assembly terminals.

(h) Slide the cover off the housing and away from the rear of the panel (view D, fig.3-8).

(i) Release the meter panel assembly 1A15A8 and position it downward until it rests against electrical equipment cabinet 1A16.

(j) Remove the housing from meter panel assembly 1A15A8.

(2) *Replacement.*

(a) Repeat steps (1)(a) through (d) on replacement indicator light assembly.

(b) Remove cover from housing on replacement indicator light assembly (T, fig.6-8).

(c) Insert the housing in position through meter panel assembly 1A15A8, and position the meter panel assembly 1A15A8 in a horizontal position.

(d) Slip cover over housing from rear of meter panel assembly 1A15A8 until cover and housing fit snug against 1A15A8 (D, fig. 3-8).

(e) Solder wires removed in step (1)(g) to terminals on rear of indicator light assembly.

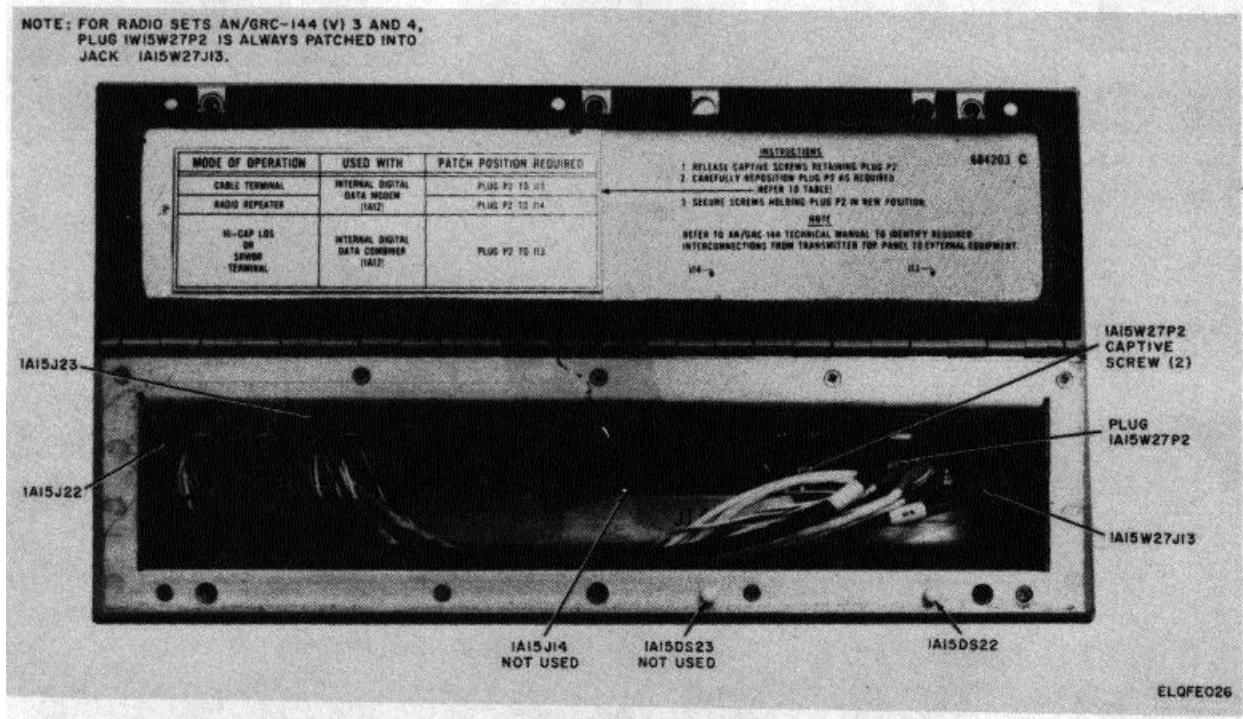


Figure 3-5.1. T-1054(P)/GRC-144(V) radio patch panel (p/o 1A15), front interior view, parts location.



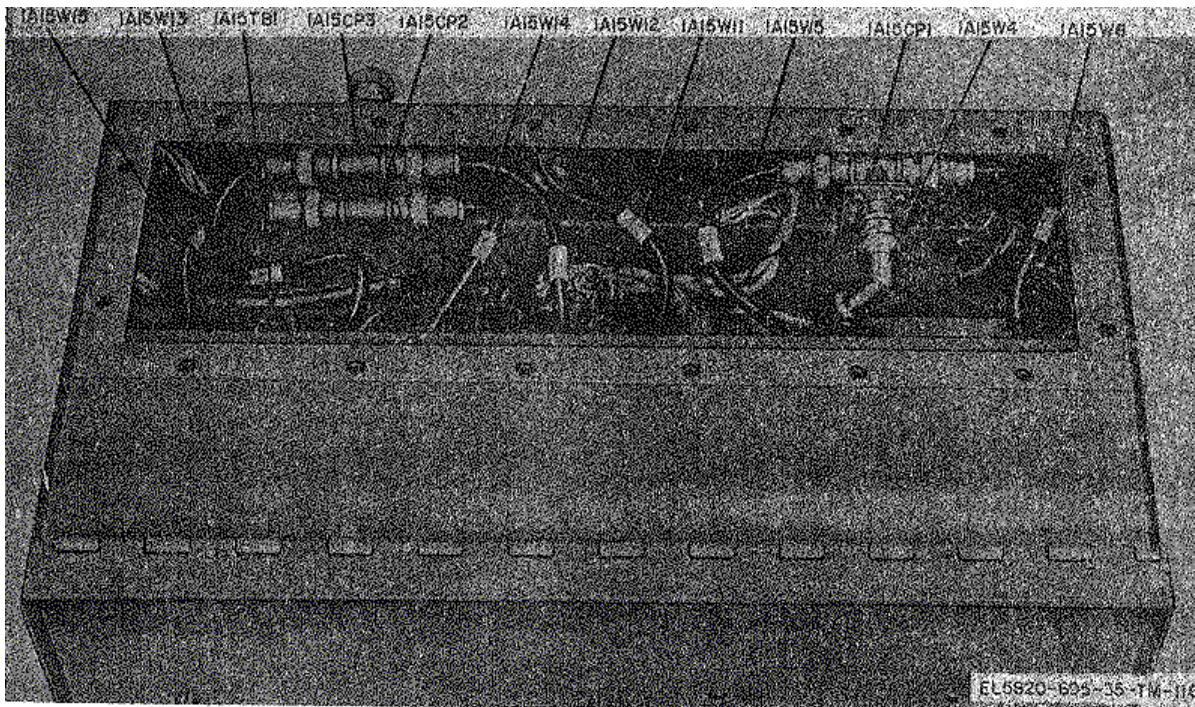


Figure 3-6. Radio patch panel (p/o 1A15), top interior view, part location.

(f) Release meter panel assembly 1A15A8 and position it downward until it rests against electrical equipment cabinet 1A15.

(g) Tighten the two screws from front of 1A15A8 (C, fig. 3-8) to secure the housing to the cover.

(h) Insert the lens assembly into the housing so that the bulb board slot aligns with the bulb board index key (D, fig. 3-8).

(i) Replace the new lens and diffuser with the lens and diffuser of replaced indicator light assembly (B, fig. 3-8).

(j) Rotate lens assembly 90° so that lens and legend index it at top of light, then push lens assembly into housing.

(k) Finger tighten the two meter panel captive screws to secure meter panel assembly 1A15A8.

c. *Replacement of Potentiometer 1A15A8R2 through 1A14A8R7 (fig. 3-4).* To replace a potentiometer, remove equipment power (para 320a), replace the defective potentiometer, restore equipment power (para 3-20b) and then perform the applicable calibration procedure listed in the chart below.

**POTENTIOMETER CALIBRATION**

<i>Potentiometer</i>	<i>Calibration procedure</i>
1A15A8R2, A15A8SR3, 1A15ASR4.	Calibration of T-1054/ and GRC-144 frequency
Potentiometer	Calibration procedure

multiplier metering circuits (para 3-59).

1A16AR5 .....	Calibration of T-1054/ GRC-144 reflected rf power metering circuit (para 385).
1A15A8R6.....	Calibration of T-1054/ GRC-44 rf power metering circuit (para 13-57).
1A15A8R7.....	Calibration of T-1054/ GR-144 traffic metering circuit I(para 3-60).

**3-22. Replacement of Parts in Power Supply Chassis Assembly 1A1A13**  
(fig. 3-9 through 3-11).

To replace any part in power supply chassis assembly 1A1A13; remove power supply 1A1 (a below) and refer to applicable replacement procedure (b through f below) for the part to be replaced. After the part has been replaced, refer to the steps of g below for replacement of power supply 1A1. Parts, located on terminal boards 1A1A13TB1 and 1A1A14TB2 are removed using standard soldering techniques (para 3-19).

a. *Removal of Power Supply 1A1.*

(1) Set the POWER ON/OFF switch on meter panel assembly 1A15A8 to OFF.

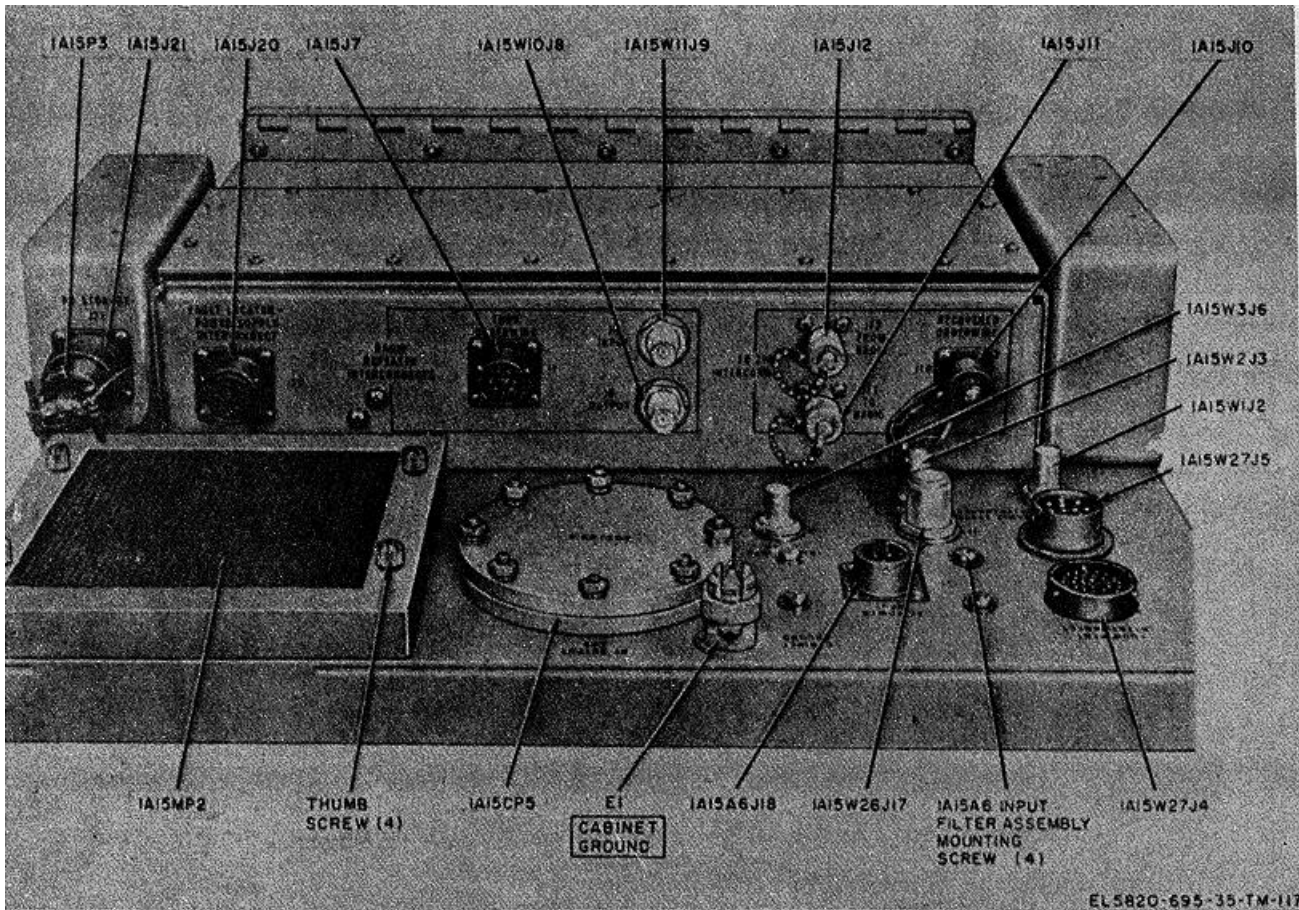


Figure 3-7. Transmitter, Radio T-1054/GRC-144, rear top view, parts location.

(2) Loosen the two meter panel captive screws (fig. 3-J1) on meter panel assembly 1A15A8.

(3) Position the meter panel assembly upward and lock in position by use of the panel locking latch (fig. -4).

(4) Alternately unscrew each power supply captive screw (fig. 3-1) one or two turns each until both captive screws rotate freely.

(5) Slide power supply 1A1 out of electrical equipment cabinet 1A15 approximately 3 inches by grasping the two power supply captive screws and 1A1 bottom cover.

(6) Slide power supply 1A1 forward while tilting downward to prevent damage to meter panel assembly 1A15A8 cables located above power supply 1A1. Continue this removal technique until power supply 1A1 is completely removed from electrical equipment cabinet 1A16.

(7) Loosen the two captive screws that secure 5/6v voltage regulator 1A1A1 to power supply chassis assembly 1A1A13 and then remove 1A1A1 from the chassis.

(8) Repeat step (7) for regulators 1A1A2, 1A1A3, 1A1A4, and 1A1A6 through 1A1A12.

(9) Remove the two screws securing blank panel 1A1A5 and, remove the blank panel.

*b. Removal of Rack Mounted Component Connectors 1A1A13XA1 Through 1A1A13XA4 and 1A1A13XA6 Through 1A1A13XA12 (fig. 3-9)*

(1) Remove the ten screws and associated washers securing the rear shield to power supply chassis assembly 1A1A13.

(2) Tag and unsolder wires connected to component terminals of the connector to be replaced.

(3) Remove the two screws, two nuts, and washers securing component connector to power supply chassis assembly 1A1A1 and remove the connector.

*c. Replacement of Rack Mounted Component Connectors 1A1A3SXA1 Through 1A1A13XA4 and 1A1A13XA6 Through 1A1A13A12 (fig. 3-9).*

(1) Mount replacement component connector in place of removed connector using the two screws, two nuts, and washers removed in step b(3). Do not tighten the two screws and nuts.



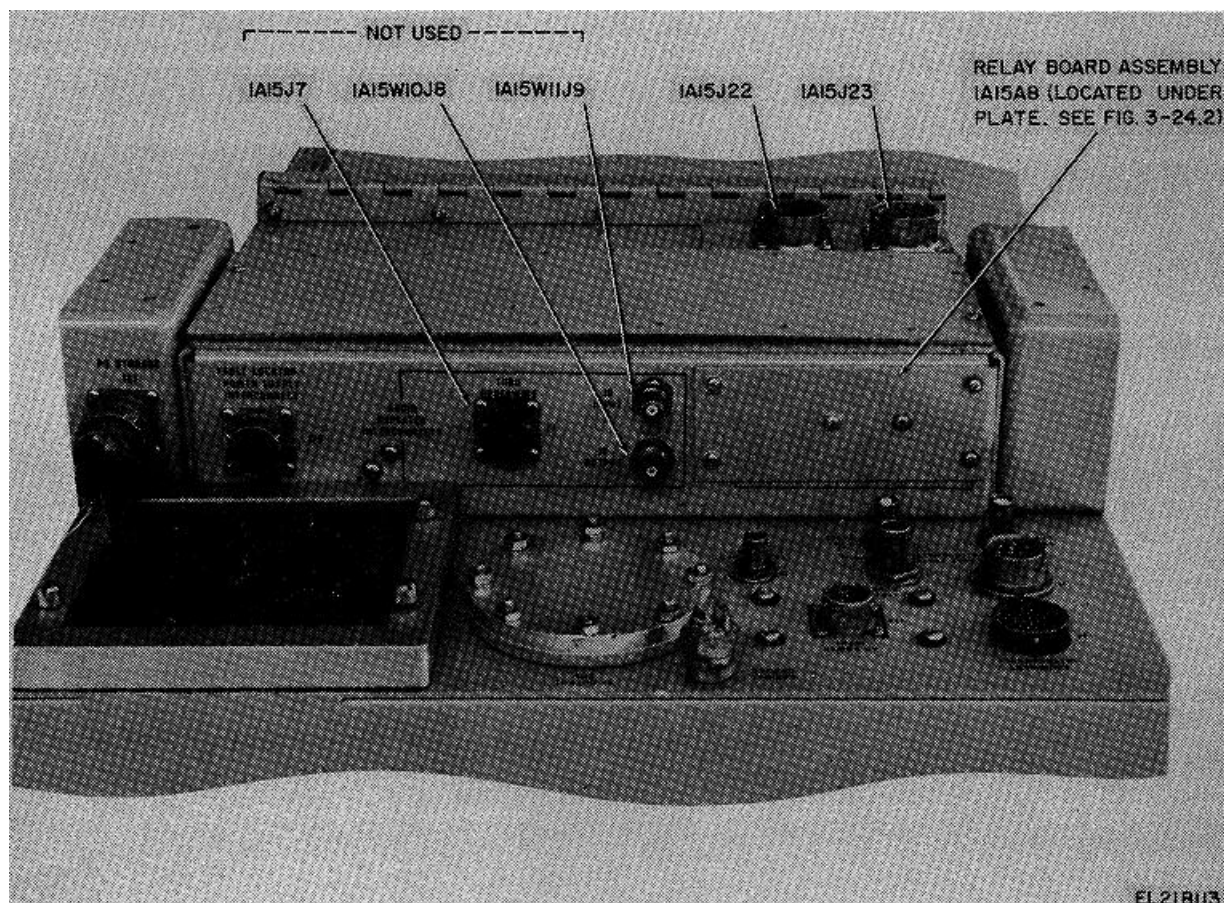
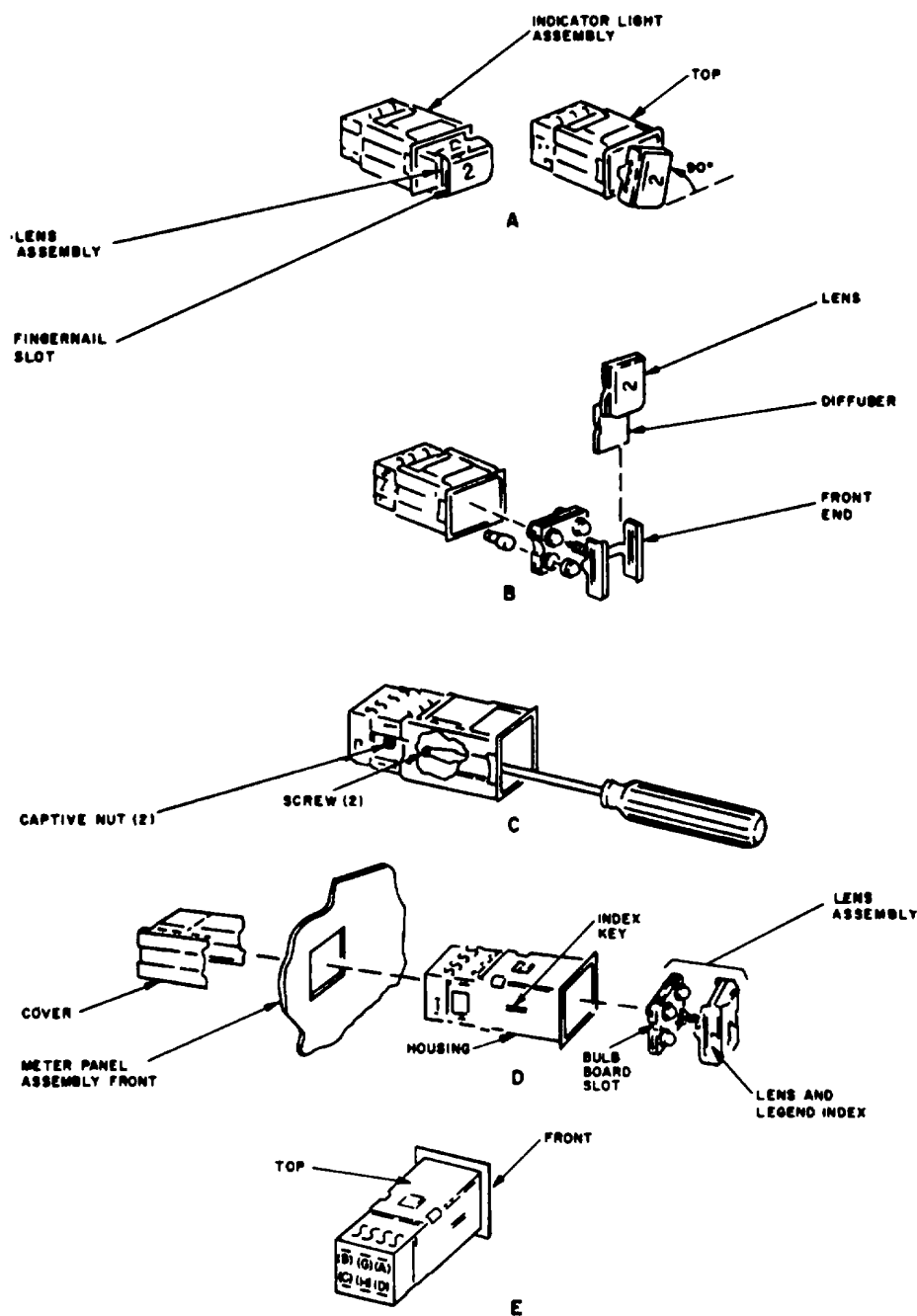


Figure 3-7.1. T-1054(P)A/GRC-144(V) top rear view, interface connectors.

Change 6 3-38.1/(3-38.2 blank)



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**Figure 3-8. Assembly detail, indicator light assemblies, meter panel assembly 1A15A8, typical.**

(2) Insert voltage regulator, used with replaced connector into power supply chassis assembly 1A1A18 and seat its connector into replacement connector. Secure the regulator with its two captive screws.

(3) Tighten the two screws and nuts securing connector to power supply chassis assembly 1A1A18 and then remove the voltage regulator.

(4) Solder wires removed in step b(2) to connector terminals.

(5) Mount and secure the rear shield to power supply chassis assembly 1A1A13 using the ten screws and associated washers removed in step b(l).

*d. Removal of Lamp Sockets 1A1A13XDS1 Through 1A1A13XDS4 and 1A1A13XDS6 Through 1A1A13XDS12 (fig. L-9).*

(1) Turn power supply chassis assembly 1A1A13 upside down and remove the 15 screws.



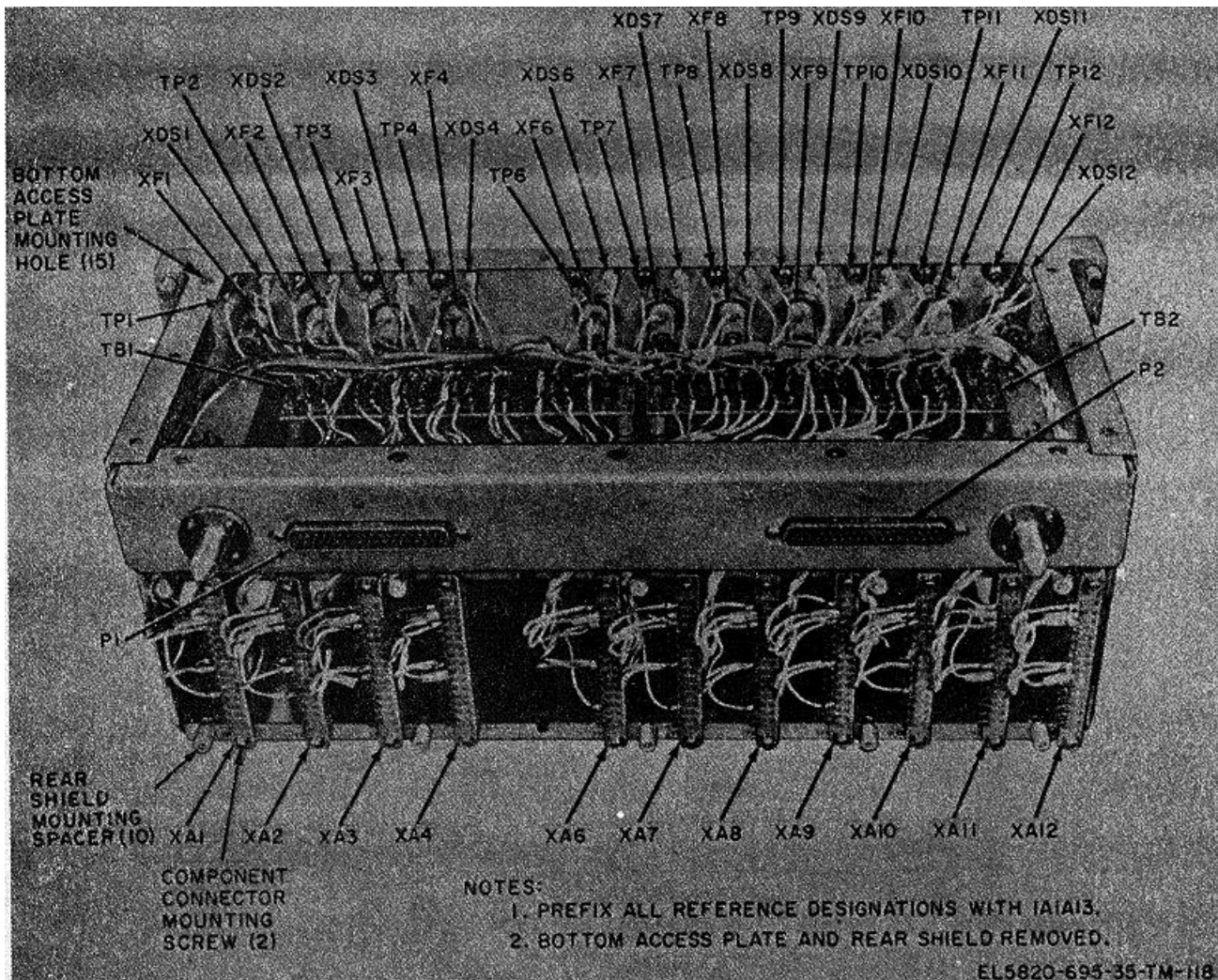


Figure 3-9. Power supply chassis assembly 1A1A13, parts location.

securing bottom access plate to power supply chassis assembly 1A1A13.

(2) Tag and unsolder wires connected to lamp socket being removed.

(3) Force press fitted lamp socket through its mounting hole in power supply chassis assembly 1A1A13 by pressing terminal end toward mounting hole and remove lamp socket from front of power supply chassis assembly 1A1A13.

*e. Replacement of Lamp Sockets 1A1A13XDS1 Through 1A1A13XDS4 and 1A1A13XDS6 Through 1A1A13XDS12 (fig. 3-9).*

(1) Replace lamp socket by forcing terminal end of press fitted lamp socket through front of mounting hole in power supply chassis assembly

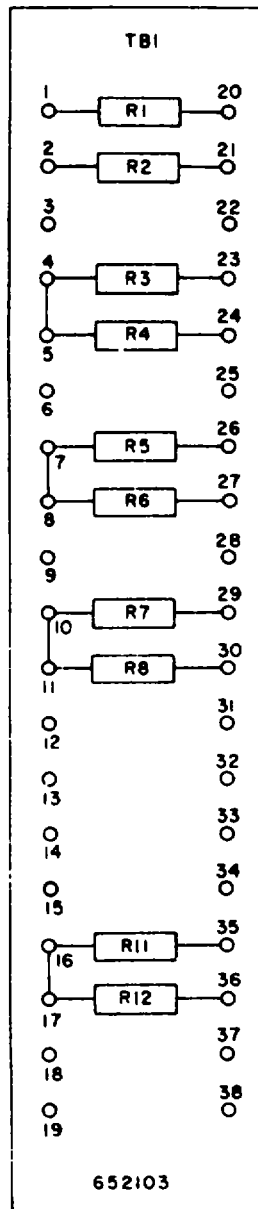
1A1A113 and pressing lamp end until mounted snugly against power supply chassis assembly 1A1A13 frame.

(2) Solder wires removed in step d(2) to lamp socket terminals.

(3) Mount and secure bottom access plate to power supply chassis assembly 1A1A13 using the 15 screws removed in step d(1).

*f. Removal and Replacement of Chassis Mounted Connectors 1A1A13P1 or 1A1A13P2 (fig. 3-9).*

(1) Turn power supply chassis assembly 1A1A13 upside down and, remove the 15 screws securing bottom access plate to power supply chassis assembly 1A1A13.



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NOTE  
PREFIX ALL REFERENCE  
DESIGNATIONS WITH 1A1A13.

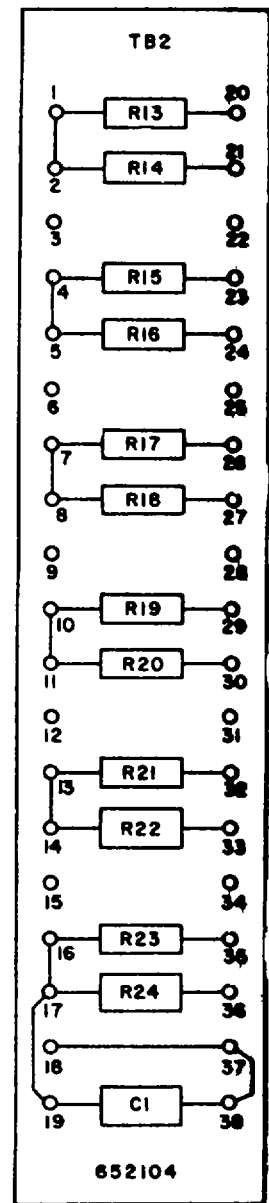
Figure 3-10. Terminal board 1A1A13TB1, top view, part location.

(2) If a connector contact requires replacement refer to the procedures provided in paragraph 3-37 for removal and replacement of connector contact and proceed to step (7).

(3) If the connector requires replacement, remove the two screws, two nuts and washers recurring the connector and ground lug to power apply chassis assembly 1A1A13.

(4) Remove connector from mounting hole and insert replacement connector in mounting hole. Secure the replacement connector and ground lug in position by tightening the two screws two nuts and washers removed in step (3).

(5) Remove a wired connector contact from the removed connector and install in the replaced



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NOTE:  
PREFIX ALL REFERENCE  
DESIGNATIONS WITH 1A1A13.

Figure 3-11. Terminal board 1A1A13TB2, top view, parts location

connector identical contact location. Refer to paragraph 3-37c for connector pin removal and replacement.

(6) Repeat step (5) for each wired connector contact until transfer of all connector contacts is completed.

(7) Mount and secure the bottom access plate to power supply chassis assembly 1A1A13 using the 15 screws removed in step (1).

*g. Replacement of Power Supply 1A1.*

(1) Insert 5/6v voltage regulator 1A1A1 into replacement power supply chassis 1A1A1, aligning printed wiring board with guide rails located on upper and lower portions of power

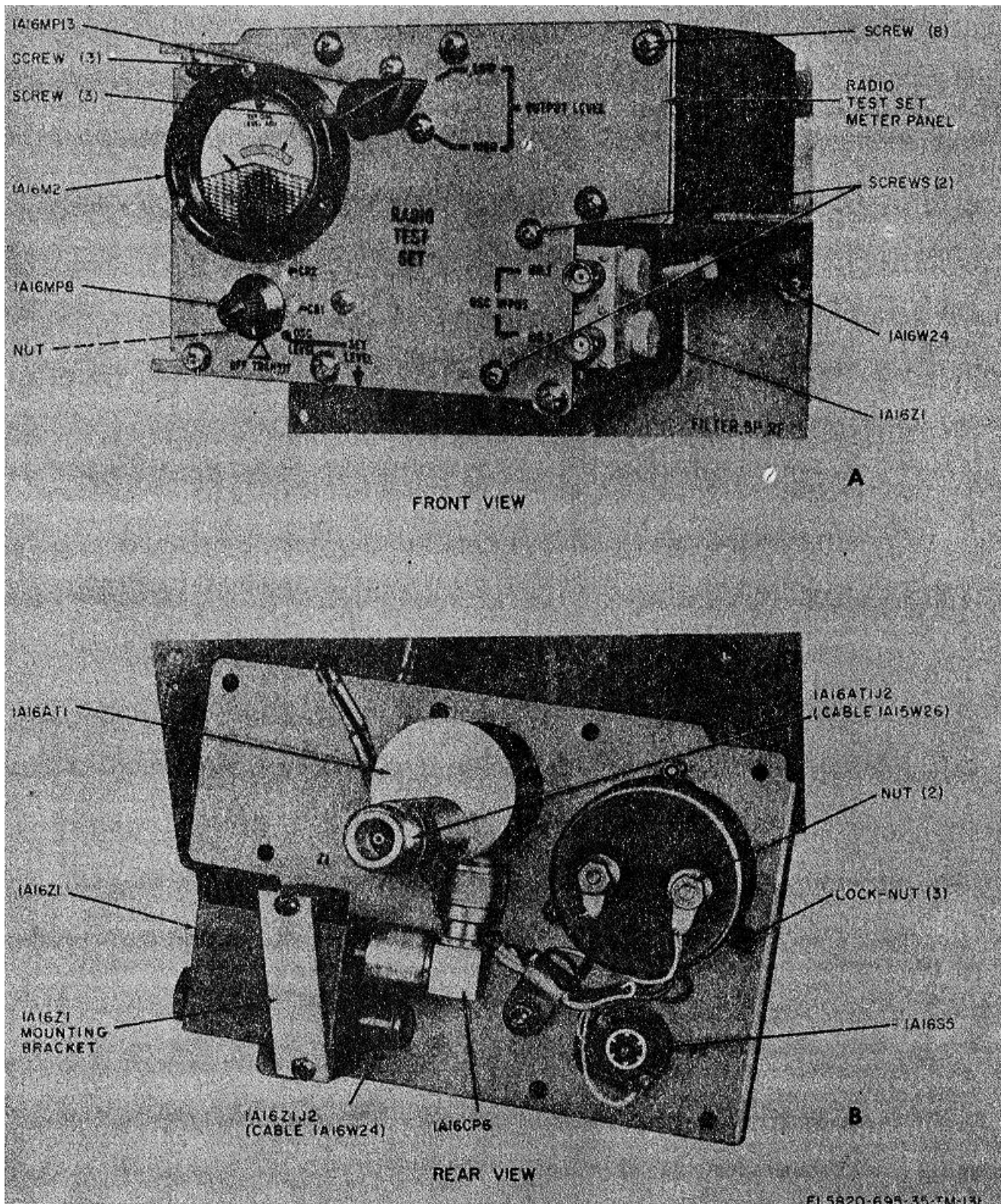


Figure 3-12. Radio test set (p/o 1A16), parts location.

supply chassis assembly 1A1A13. Then slowly push the plug-in component into power supply chassis assembly 1A1A13 until the connectors are mated.

(2) Tighten the two captive screws on 6/6v voltage regulator 1A1A securing the plug-in component to replacement power supply chassis assembly 1A1A13.

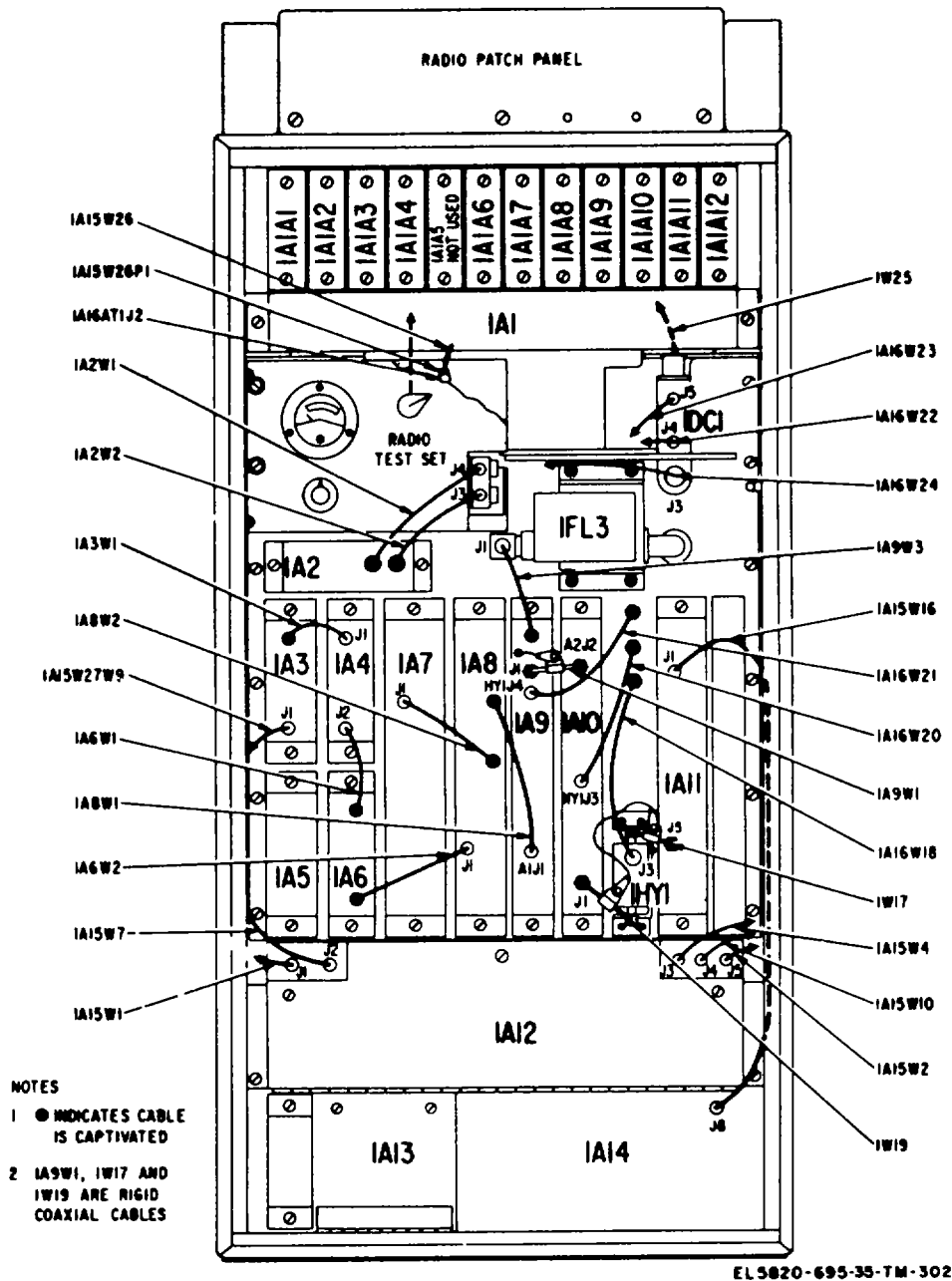


Figure 3-13. Transmitter, Radio T-1054/GRC-144, cable locations

(3) Repeat steps (1) and (2) for regulators 1A1A2, 1A1A3, and 1A1A4.

(4) Mount blank panel A1A5 on power supply chassis assembly 1A1A13 and secure in place using the original mounting hardware.

(5) Repeat steps (1) and (2) for regulators 1A1A6 through 1A1A12.

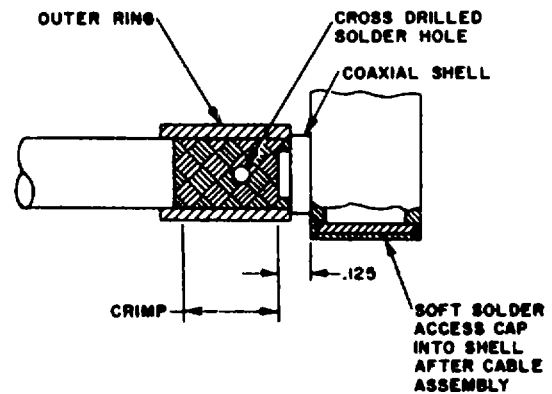
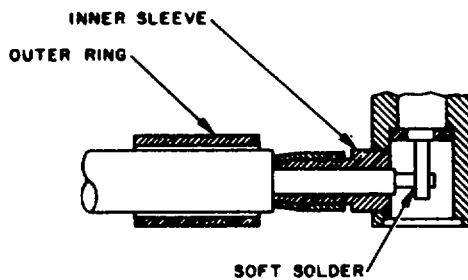
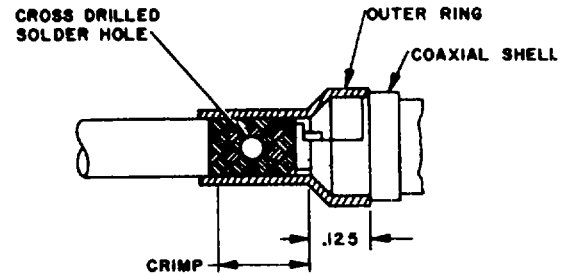
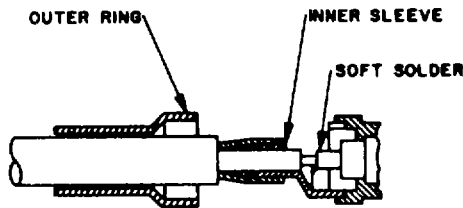
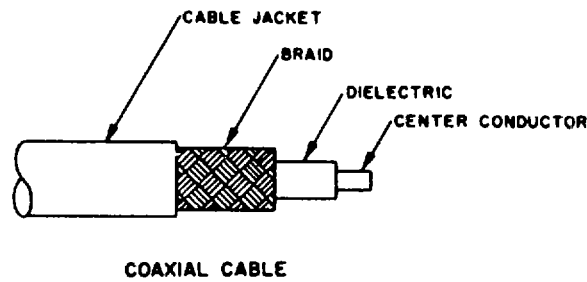
(6) Position power supply 1A1 into its inclosure in electrical equipment cabinet 1A15 with the front end of power supply tilted downward. Slowly slide power supply into the cabinet taking care not to damage meter panel cables.

(7) Tilt the power supply to a level position when approximately 3 inches of the front part of power supply remains out of the inclosure, then push power supply into the cabinet until guide pins and connectors are mated.

(8) Alternately tighten the two power supply captive screws two turns at a time until the power supply is securely fastened to the cabinet.

(9) Release the meter panel assembly 1A15A8 and position it downward until it rests against the cabinet.

(10) Secure meter panel assembly 1A15A8 by tightening the two meter panel captive screws.



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Figure 3-14. Repair detail, rectangular connectors with solder type removable coaxial contacts

(11) Set the POWER ON/OFF switch on meter panel assembly 1A15A8 to ON.

**3-23. Replacement of Vane Axial Fan 1A1581** (fig. 3-3 and 3-4)

*a. Removal.*

(1) Remove power from T-1054/GRC-144 (para 5-20a).

(2) Remove power supply 1A1 (para 8-22& (2) through (6)).

(3) Remove connector 1A15P3 (fig. 8-7) from STORAGE J21 or FAULT LOCATOR POWER SUPPLY INTERCONNECT 20 at top of electrical equipment cabinet 1A15 to provide access to air exhaust filter 1A15MP2.

(4) Loosen the four thumbscrews securing air exhaust filter 1A15MP2 to top of electrical equipment cabinet 1A15 and remove the filter.

(5) While supporting the fan 1A15B1 inside of the cabinet, loosen, but do not remove

NOTE: REFER TO FIGURE 3-13  
 FOR INTERCONNECTING  
 CABLES TO OTHER SUBASSEMBLIES

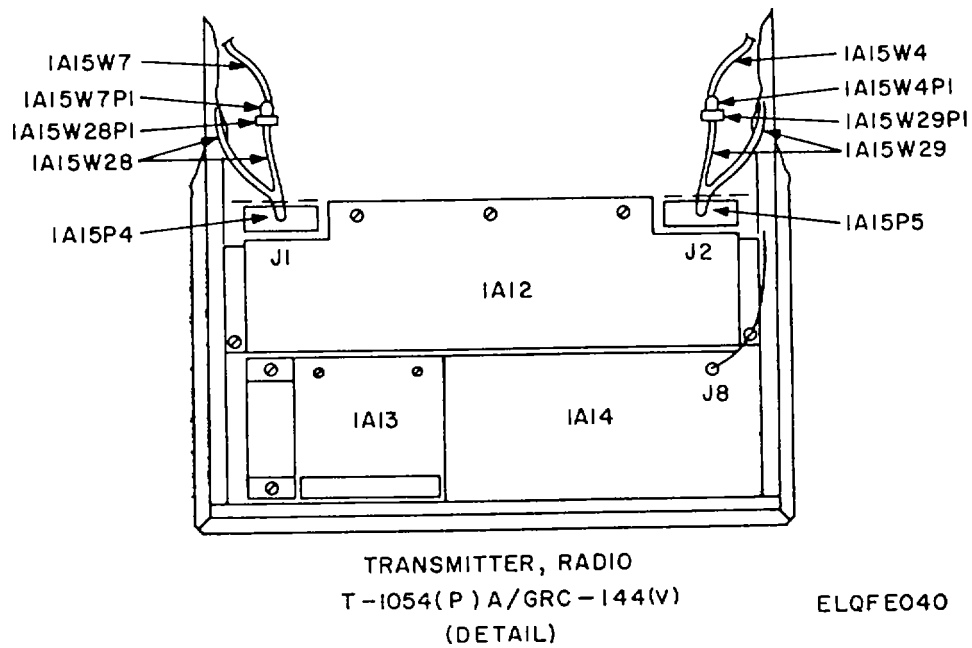


Figure 3-13.1 Transmitter, Radio T-1054(P)A/GRC-144(V)  
 interconnecting cables.



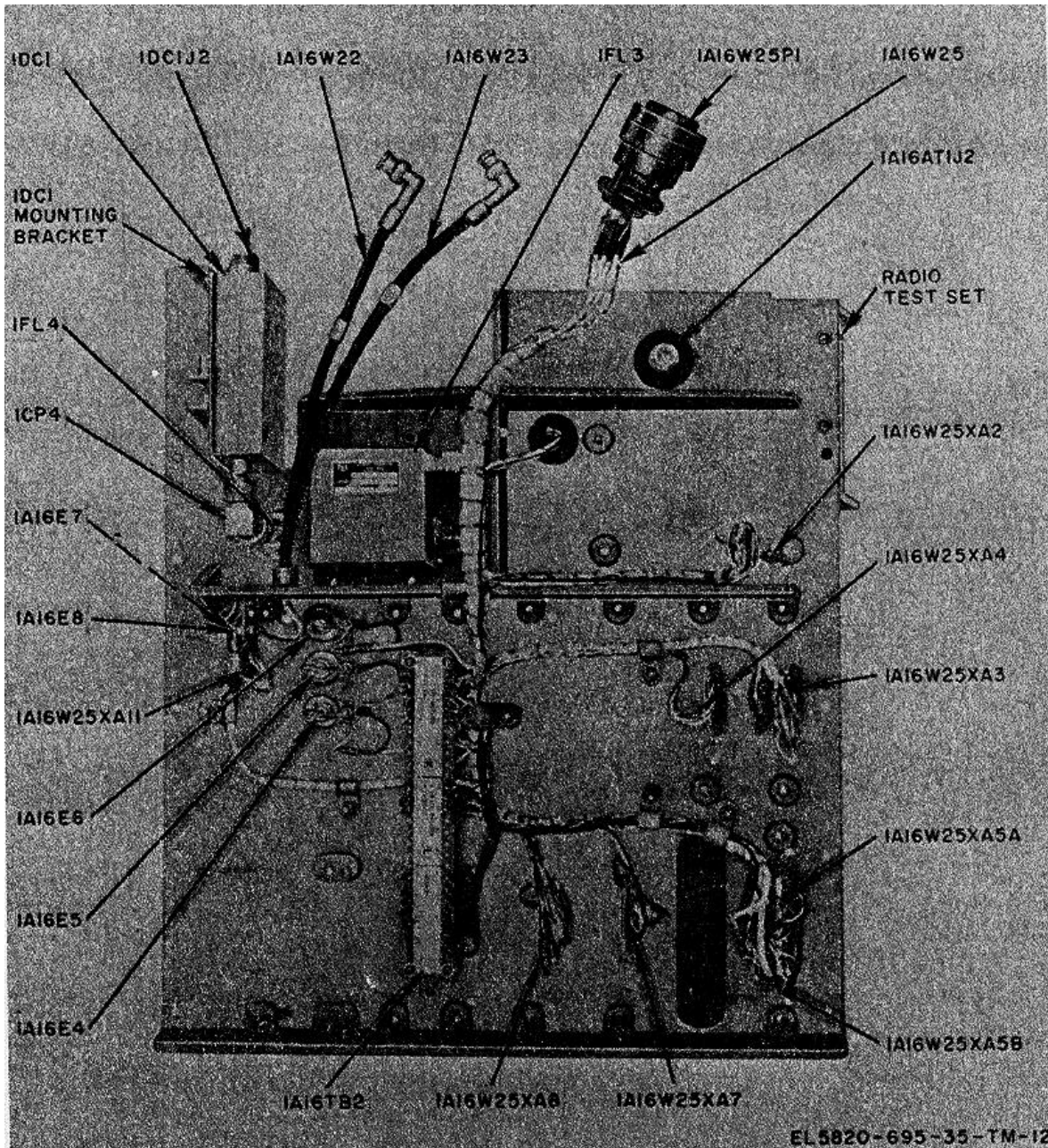


Figure 3-15. Plate assembly 1A16, rear view, parts location.

the four screws securing the fan to the cabinet. Each screw has a synclamp nut which clamps the fan to the cabinet frame.

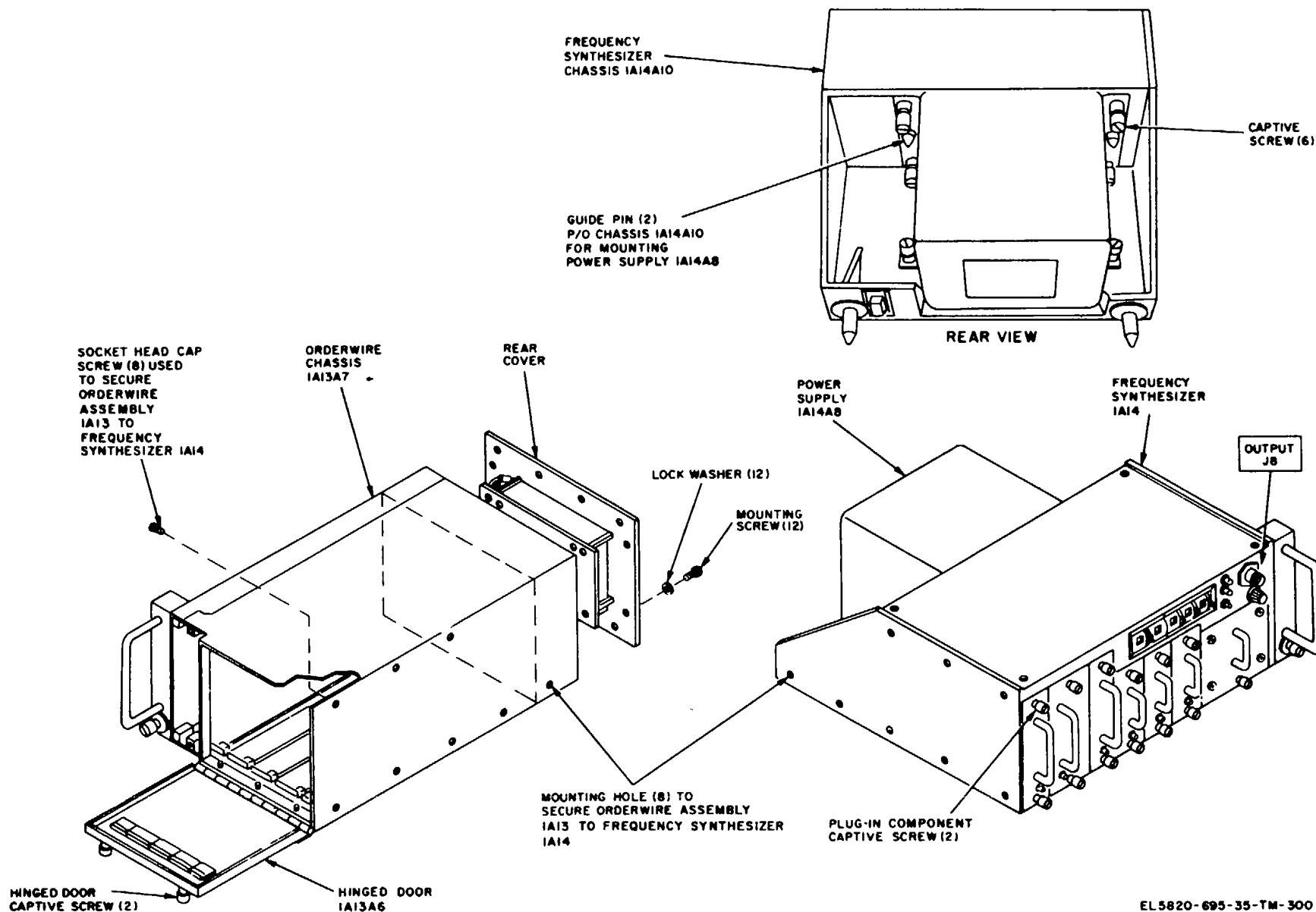
(6) Tilt the fan upward to slide it past the synclamps, then lower the fan into the cabinet

(7) Tag the wires connected to the fan terminals. Remove the three screws that secure the wire lugs to the fan terminals. The lugs are soldered to the tagged wires.

(8) Remove the fan from the cabinet.

*b. Replacement.*

(1) Check that AIR FLOW arrow (printed on side of replacement vane axial fan 1A15B1) is pointing upward, and insert the fan into upper



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Figure 3-16. Disassembly detail, orderwire assembly-electrical frequency synthesizer 1A13/1A14.



right section of electrical equipment cabinet IA15. Connect wire lugs to the fall terminals using the three screws removed in step a(7).

(2) Position the fan against top wall of the cabinet between the four synclamps which clamp the fan to the cabinet frame.

(3) Secure the fan to the cabinet by tightening the four screws still connected to the four synclamps.

(4) Mount air exhaust filter 1A15MP2 to top of the cabinet and tighten the four thumbscrews.

(5) Connect the connector removed in step a(3) to J21 or J20 on electrical equipment cabinet IA15.

(6) Replace power supply 1A1 (para 8-22g (6) through (10)).

(7) Restore power to T-1054/GRC44 (para 3-20b).

### 3-24. Replacement of Capacitor 1 A15C1

(fig. 3-3)

#### a. Removal.

(1) Remove power from T-1054/GRC--144 (para 3-20a).

(2) Remove power supply 1A1 (para 3-22a (2) through (6)).

(3) Remove the two nuts securing capacitor mounting bracket to rear wall of electrical equipment cabinet IA15 and remove the capacitor mounting bracket.

(4) Tag and unsolder the wires connected to capacitor 1A15CL terminals and remove the capacitor.

#### b. Replacement.

(1) Insert replacement capacitor into the cabinet and solder the two capacitor wires removed in step a(4).

(2) Insert capacitor mounting bracket over the replacement capacitor and place the capacitor mounting bracket on the threaded studs on rear wall of the cabinet.

(3) Replace and tighten the two nuts securing capacitor mounting bracket to rear wall of the cabinet.

(4) Replace power supply 1A1 (para 3-22g (6) through (10)).

(5) Restore power to T-1054/GRC-144 (para 3-20b).

**3-25.** Replacement of Terminal Board IA15TB4, Input Filter 1A15A6FL1 or 1A15A6FL2 (fig. 3-3, 3-35 and 3-36)

### WARNING

**115 vac is applied to input filters 1A15A6FL1 and 1A15A6FL2. Be sure that the external ac power cable is disconnected from 1A15A6J18 (fig. 3-7) before performing this procedure.**

#### f. Removal.

(1) Remove power from T-1054/GRC-144 (para 3-20a).

(2) Remove power supply 1A1 (para 3-22a (2) through (6)).

(3) Disconnect cables from connectors 1A15W1J2, 1A15W2J3, 1A15W3J6, and 1A15W26J17 on top of electrical equipment cabinet IA15 (fig. 3-7).

(4) Using a 3/4-inch open end wrench, remove the hex-nut and washers that secure connector 1A15W26J17 to the top of electrical equipment cabinet IA15. Note the position of the washers for replacement.

(5) From inside of electrical equipment cabinet IA15, lower coaxial cable 1A15W26 with attached connector 1A15W26J17 (fig. 3-7).

(6) Using a 5/8-inch open end wrench, remove the hex-nut and washers that secure 1A15W3J6, 1A15W1J2, and 1A15W2J3 (fig. 3-7) to the top of electrical equipment cabinet IA15. Note the position of the washers for replacement.

(7) From inside of electrical equipment IA15, lower coaxial cables 1A15W3, IA15W1, and IA15W2 with attached connectors 1A15W3J6, 1A15W1J2, and 1A15W2J3.

(8) Remove the four screws that secure the filter clamp (fig. 3-3) in place and remove the filter clamp.

(9) Unsolder and remove the four wires connected to terminal board 1A15TB4 (fig. 3-36).

(10) Remove the four 1A15A6 input filter assembly mounting screws and washers (fig. 3-7) from top of electrical equipment cabinet IA15 to release input filter assembly 1A15A6 (fig. 3-3) from electrical equipment cabinet IA15.

(11) From inside the cabinet tag, unsolder, and remove the wire lead attached to ground terminal E2 (located on the right side of the filter assembly).

(12) Position the filter assembly to provide access to the bottom terminals of the filters. Tag, unsolder, and remove the leads attached to the bottom terminals of the filters.

(13) Carefully remove the filter assembly from the cabinet.

(14) On the filter assembly, remove the four screws that secure the cover to the box. Carefully

ease the cover off of the box to provide access to the upper terminal of the filters. Unsolder and remove the lead from the defective filter to be replaced.

(15) Remove the hex-nut that secures the defective filter to the cover and remove the filter.

*b. Replacement.*

(1) Remove the mounting nut from the replacement filter and secure the replacement filter to the filter assembly cover with the mounting nut.

(2) Solder the wire lead removed in step | (a(14) to the upper terminal of replacement filter.

(3) Place the cover on the assembly box being careful that the leads from the filters to connector 1A15A6J18 do not get crimped between the cover and the box. Secure the cover to the box using the four screws removed in step o(14).

(4) Position the filter assembly so that the leads removed from the bottom terminals of the | filters in step a(12) can be resoldered in place. Solder the leads to their respective terminals.

(5) Solder the lead removed in step a(11) to ground terminal E2 on the right side of the filter assembly.

(6) Position the filter assembly to align its mounting holes with the mounting holes in the top of the cabinet. Secure the filter assembly to the cabinet using the four filter assembly mounting screws and washers removed in step a(10) above.

(7) terminal board 1A15TB4 into position and solder the four wires removed in step a (9).

(8) Replace the filter clamp and secure in place using the four screws removed in step n(8).

(9) Reposition cables with attached connectors, lowered in step a[(5) and (7) above, so that the connectors are in position for securing to the top of electrical equipment cabinet 1A15. Secure the connectors with the hex-nuts and washers removed in step a(4) and (6).

(10) Replace power supply 1A1(para 3-22g (6) through (10)).

(11) Connect cables disconnected in a(8) above.

(12) Restore power to T-1054/GRC-144 (para 3-20b).

### 3-26. Replacement of Coaxial Circulator 1A9HY1

(fig 3-1 and 5-71)

*a. Removal.*

(1) Set POWER ON/OFF switch on meter panel assembly 1A15A8 to OFF.

### CAUTION

**Removal of components with rigid coaxial cables must be performed carefully to prevent damage to the rigid coaxial cables.**

(2) Remove transmitter frequency mixer stage IA9 from plate assembly 1A16 (TM 115820-69.512).

(3) Loosen, but do not remove, the screws securing crystal mixer 1A9A1 to the transmitter frequency mixer stage 1A9 enclosure.

(4) Disconnect the mating type TNC connector between coaxial circulator 1A9tY11 and crystal mixer IA9A1.

(5) Slide crystal mixer IA9A11 away from coaxial circulator 1A9HY1 until it is free of the mating TNC connector, then remove crystal mixer 1A9A1 from the transmitter frequency mixer stage 1A9 enclosure.

(6) Remove the four screws and washers securing coaxial circulator IA9HY1 to the transmitter frequency mixer stage 1AS enclosure

(7) Using a 5,'16-inch open end wrench, loosen the nut securing coaxial cable 1A9W2 to the INPUT J1 connector on coaxial circulator IA9HY1.

(8) Carefully slide coaxial circulator 1A9HY1 toward the) bottom of the transmitter frequency mixer stage IA9 enclosure until the connector pin in coaxial cable 1A9W2 is free.

(9) Lift coax: al circulator IA9HY1 for clearance and disconnect coaxial cable 1A9W3 from the OUTPUT J3 connector on coaxial circulator IA9HY1.

(10) Remove coaxial circulator IA9HY1 from the transmitter frequency mixer stage 1A9 enclosure.

*b. Replacement*

(1) Insert replacement coaxial circulator 1A9HY1 into the transmitter frequency mixer stage 1A9 enclosure and connect coaxial cable 1A9W8 to the OUTPUT J3 connector on coaxial circulator IA9HY1.

(2) Carefully mate the connector pin on coaxial cable 1A9U'2 to the INPUT J1 connector on coaxial circulator 1A9HY1 and then tighten the connector nut on coaxial cable 1A9W2.

(3) Install the four screws and washers securing coaxial circulator I A9HY1 to the transmitter frequency mixer stage 1A9 enclosure, but do not tighten the four screws at this time.

(4) Install crystal mixer IA9A1 into the transmitter frequency mixer stage 1A9 enclosure

(5) Connect and tighten the mating type TNC connector between crystal mixer 1A9A1 and coaxial circulator 1A9HY,1.

(6) Tighten the four screws securing coaxial circulator 1A9HY1 to the transmitter frequency mixer stage 1A9 enclosure, then tighten the two screws securing crystal mixer LA9A1 to the transmitter frequency mixer stage 1A9 enclosure.

**CAUTION**

**Removal of components with rigid coaxial cable must be performed carefully to prevent damage to the rigid coaxial cables.**

(7) Reinstall transmitter frequency mixer stage 1A9 on plate assembly 1A16 (TM 115820-69-42).

(8) Set the POWER ON/OFF switch on meter panel assembly 1A15A8 to ON.

(9) Perform the T-1054/GRC-144 frequency multiplier metering circuit calibration procedure (para 3-59).

**3-27. Replacement of Coaxial Circulator 1A10HY1**  
(fig. 8-1 and 5-72)

*a. Removal*

(1) Set the POWER ON/OFF switch on meter panel assembly 1A15A8 to OFF.

**CAUTION**

**Removal of components with rigid coaxial cable must be performed carefully to prevent damage to the rigid coaxial cables.**

(2) Remove transmitter frequency multiplier group IA10 from plate assembly 1A16 (TM 11-5820-69542).

(3) Loosen, but do not remove, the two screws on the rear side of component 1A10 securing transmitter 3rd stage frequency multiplier 1A10A2 to the transmitter frequency multiplier group IA10 enclosure.

(4) Disconnect the mating type TNC connector between coaxial circulator 1A10HY1 and transmitter 3rd stage frequency multiplier IA10HY1 and transmitter 3rd stage frequency multiplier 1A10A2 and remove 1A10A2 from the enclosure.

(5) Loosen the two screws securing transmitter 2nd stage frequency multiplier 1A10A1 to the transmitter frequency multiplier group IA10 enclosure and disconnect the mating type TNC connector between coaxial circulator 1A10HY1 and

transmitter 2nd stage frequency multiplier 1A10A1. Remove 1A10A1 from the enclosure.

(6) Remove the three screws securing coaxial circulator IA10HY1 to the transmitter frequency multiplier group IA10 enclosure and then remove coaxial circulator IA10HY1 from the transmitter frequency multiplier group IA10 enclosure.

*b. Replacement.*

(1) Replace transmitter 2nd stage frequency multiplier 1A10A1 and transmitter 3rd stage frequency multiplier IA10A2 into their respective screw slots on the IA10 enclosure (fig. 5-72). Place replacement coaxial circulator 1A10HY1 on the IA10 enclosure between IA10A1 and 1A10A2. Connect the mating type TNC connector between IA10HY1 and 1A10A1.

(2) Connect the mating type TNC connector between coaxial circulator IA10HY1 and transmitter 3rd stage frequency multiplier 1A10A2.

(3) Replace and tighten the three screws securing coaxial circulator 1A10HY1 to IA10 enclosure.

(4) Tighten the screws securing transmitter 2nd stage frequency multiplier IA10A1 and transmitter 3rd stage frequency multiplier 1A10A2 to IA10 enclosure.

**CAUTION**

**Replacement of components with rigid coaxial cables must be performed carefully to prevent damage to the rigid coaxial cables.**

(5) Reinstall transmitter frequency multiplier group IA10 on plate assembly 1A16 (TM 11-5820-69-12).

(6) Set the POWER ON/OFF switch on meter panel assembly IA15A8 to ON.

(7) Perform the T-1054/GRC-144 frequency multiplier metering circuit calibration procedure (para 3-59).

**3-28. Replacement of Coaxial Circulator 1HY1**  
(fig. 3-1)

*a. Removal.*

(1) Set the POWER ON/OFF switch on meter panel assembly 1A15A8 to OFF.

(2) Disconnect coaxial cable 1A16W18 (fig. 3-13) from coaxial circulator 1HY1 connector DC MONITOR J8.

**CAUTION**

**Removal of rigid coaxial cables must be performed carefully to prevent damage to the rigid coaxial cables.**

(3) Disconnect rigid coaxial cables 1W17 and 1W19 from coaxial circulator 1HY1 (TM 115820-695-12).

(4) Remove the four screws and washers securing the dc monitor bracket, on which coaxial circulator 1HY1 is mounted, to plate assembly 1A16. The remove dc monitor bracket and coaxial circulator 1HY1 from plate assembly 1A16.

(5) Remove the three screws and washers securing coaxial circulator 1HY1 to the dc monitor bracket.

*b. Replacement.*

(1) Mount replacement coaxial circulator 1HY1 on the dc monitor bracket and align the three mounting holes. Then secure coaxial circulator 1HY1 to dc monitor bracket, using the three screws and washers removed in step a(5).

(2) Place dc monitor bracket with coaxial circulator 1HY1 on plate assembly A16 and align the four mounting holes. Then secure dc monitor bracket to plate assembly 1A16 using the four screws and washers removed in step a(4).

**CAUTION**

**Replacement of rigid coaxial cables must be performed carefully to prevent damage to the rigid coaxial cables.**

(3) Connect rigid coaxial cables 1W17 and 1W19 (TM 11-820-696-12).

(4) Connect coaxial cable 1A16W18 to coaxial circulator 1HY1 connector DC MONITOR J3.

(5) Set the POWER ON/OFF switch on meter panel assembly 1A15AS to ON.

(6) Perform the T-1054/GRCJ144 frequency multiplier metering circuit calibration procedure (para 3-59).

**3-28.1. Replacement of Coaxial Isolation 1A1HY1 (fig 3-3.1, 5-27.1)***a. Removal*

(1) Set the POWER ON/OFF switch on meter panel assembly 1 A1 5A8 to OFF.

(2) Remove assembly 1 A1 1 from plate assembly 1 A1 6.

(3) Disconnect RF cables W1 and W2 from J1 and J2 connectors on the isolator assembly.

(4) Loosen and remove the four pan head machine screws which secure the circulator 1 A1 1 enclosure. Remove the isolator assembly.

*b. Replacement*

(1) Align the replacement Isolator assembly with the four screw holes in the 1 A1 1 Enclosure. Replace and tighten the four machine screws, securing the Isolator assembly to the enclosure plate

(2) Reconnect RF cable W1 to connection J1. Reconnect RF cable W2 to connector J2

(3) Reinstall assembly 1A11 on plate assembly 1A16

(4) Set the POWER ON/OFF switch on Meter panel assembly 1 A1 5A8 to ON

**3-29. Replacement of Digital Data Modem Chassis 1A12A12**

(fig. 3-1 and 3-13)

*a. Removal.*

(1) Set the POWER ON/OFF switch on meter panel assembly 1A15A8 to OFF.

(2) Disconnect coaxial cables 1A15W1, 1A15W2, 1A15W4, 1A15W7 and 1A15W10 from digital data modem 1A12.

(3) Loosen the two assembly captive screws securing digital data modem 1A12 to electrical equipment cabinet 1A15 by alternately turning each captive screw two turns at a time until the captive screws turn freely. Withdraw digital data modem 1A12 from electrical equipment cabinet 1A15.

(4) Loosen the three cover captive screws securing the hinged front cover and lower cover.

(5) Using a card extractor carefully remove plug-in components 1A12A2 through 1A12A10 from digital data modem chassis 1A12A12 (TM 11-5820-69-12).

(6) Loosen the two captive screws securing plug-in components 1A12A1 and 1A12A11 to digital data modem chassis 1A12A12.

(7) Using the two loosened captive screws as hand grips, slowly pull 1A12A1 and 1A12A11 from their position in digital data modem chassis 1A12A12.

(8) Close and secure the hinged cover of defective digital data modem chassis 1A12A12 by tightening the three cover captive screws.

*b. Replacement.*

(1) Loosen the three cover captive screws that secure the cover to the replacement digital data modem chassis 1A12A12, and lower the cover.

(2) Carefully insert plug-in components 1A12A1 through 1A12A11, removed in step a(5) through

(7) into their respective positions in 1A12A12 as indicated on the hinged cover of 1A12.

(3) Alternately tighten the two captive screws that secure 1A12A1 and 1A12A11 to 1A12A12.

(4) Close the hinged front cover and tighten the three cover captive screws securing the hinged front cover.

(5) Insert replacement digital data modem 1A12 into electrical equipment cabinet 1A15.

(6) Alternately tighten each assembly captive screw on 1A12AIQ a few turns each. until digital data modem 1A12 is firmly seated in electrical equipment cabinet 1A16.

(7) Reconnect coaxial cables 1A15W1, 1A145W2, 1A15W4, 1A11W7 and 1A16W10 to their proper connector's 1A12A12J1, 1A12A12J5, 1A12A12J3, 1A12A12J2 and 1A12A14J4, respectively, on digital data modem 1A12.

(8) Set the POWER ON/OFF switch on meter panel assembly 1A15A8 to ON.

(9) Perform the T-1054/GRC-144 orderwire level adjustment (TM 11-58209-12). TM 11-5820-695-35

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### 3-29.1. Replacement of Digital Data Combiner IA12 Chassis (fig. 3-1 and 3-1.1)

#### a. Removal.

(1) Set the POWER ON/OFF Switch on meter panel assembly IA15A8 to OFF.

(2) Disconnect cable assemblies IA15W28 and IA15W29 connectors 1A15P4 and IA15P5 from the digital data combiner 1A12.

#### **CAUTION**

**Do not loosen one captive screw completely at one time. Completely loosening one assembly captive screw at a time may damage the digital data combiner.**

(3) Loosen the two assembly captive screws securing digital data combiner 1A12 to electrical equipment cabinet IA15 by alternately turning each captive screw two turns at a time until the captive screw turns freely. Withdraw Digital data combiner 1A12 from electrical equipment cabinet IA15.

(4) Loosen the three cover captive screws securing the hinged front cover and lower cover.

(5) Using a card extractor carefully remove plug-in components IA12A1 through IA12A8 from the digital combiner : hassis.

(6) Remove four screws on rear : over and remove cover.

(7) Remove four screws on bottom of Digital data combiner case.

TM 11-5820-695-35 (8) As viewed from the front, slowly push digital data combiner chassis from its position inside cover.

#### b. Replacement.

(1) Insert replacement digital data combiner IA12 chassis inside cover by carefully pushing chassis into cover at the rear of cover until holes on bottom of cover mate with holes at bottom of chassis.

(2) Secure digital data combiner 1A12 cover and chassis together using four screws at bottom and four screws at rear of cover removed in a(6) and a(7).

(3) Carefully insert plug-in components IA12A1 through IA12A8, removed in a(5) into their respective positions as indicated on the hinged cover of 1A12.

(4) Close the hinged front cover and tighten the three cover captive screws securing the hinged front cover.

(5) Insert replacement digital data combiner into electrical equipment cabinet IA15.

(6) Alternately tighten each assembly captive screw a few turns each until the digital data combiner 1A12 is firmly seated in the electrical equipment cabinet IA15.

(7) Reconnect cable assemblies IA15W28 and IA15W29 connectors 1A15P4 and IA15P5 to digital data combiner jacks J1 and 32 respectively.

(8) Set the POWER ON/OFF switch on meter panel assembly IA15A8 to ON.

**3-30. Replacement of Orderwire Chassis 1A13A7**

(fig. 3-1 and 3-16)

*a. Removal.*

(1) Set the POWER ON/OFF switch on meter panel assembly 1A15A8 to OFF.

(2) Disconnect coaxial cable 1A15W16 (fig. 3-13) from the OUTPUT J8 connector on electrical frequency synthesizer 1A14.

(3) Loosen the two assembly captive screws (fig. 3-1) that secure orderwire-electrical frequency synthesizer 1A1/1A14 to electrical equipment cabinet 1A15 by alternately turning each assembly captive screw two turns at a time until the captive screws rotate freely.

(4) Grasp the two handles on orderwire electrical frequency synthesizer 1A13/1A14 and carefully remove 1A13/1A14 from electrical equipment cabinet 1A15.

(5) Alternately loosen the two captive screws securing plug-in component 1A13A1 to orderwire chassis 1A13A7.

(6) Grasp the component frame around each captive screw and slowly extract 1A13A1 from its position in 1A13A7 (TM 11-5820-69512).

(7) Loosen the two hinged door captive screws (fig. 3-16) securing hinged door 1A13A6 to orderwire chassis 1A13A7 and lower the hinged door.

(8) Using a card extractor, remove plug-in components 1A13A2 through 1A13AS (TM 115820-695-12) from the defective orderwire chassis.

(9) Remove the 12 mounting screws (fig. 316) and lock washers that secure the rear cover to orderwire chassis 1A13A7. Being careful not to damage any of the wires connected to the plug on the rear cover, slide the rear cover away from the orderwire chassis to provide access to the interior of orderwire chassis 1A13A7.

(10) Using a socket head screw key, remove the socket head capscrew on the lower rear right side wall of orderwire chassis 1A13A7 (fig. 316). Replace the rear cover removed in step a(9) and secure with the 12 mounting screws and lock washers.

(11) Using the socket head screw key, remove the remaining seven socket head capscrews that secure orderwire chassis 1A13A7 to electrical equipment chassis 1A14A10. Separate the two chassis.

(12) Close the hinged door of defective orderwire chassis 1A13A7 and tighten the two hinged door captive screws.

*b. Replacement.*

(1) With the hinged door 1A13A6 open, position replacement orderwire chassis 1A13A7 next to the left side of electrical equipment chassis 1A14A10 and align the eight mounting holes on the right side of 1A13A7 with the eight mounting holes on the left side of 1A14A10.

(2) Using seven of the eight socket head capscrews removed in step a (11), secure the two chassis together by inserting and partially tightening the seven socket head capscrews. Do not tighten the seven socket head capscrews at this time.

(3) Insert orderwire-electrical frequency synthesizer 1A1/1A14 into electrical equipment cabinet 1A15. Alternately tighten the two assembly captive screws on 1A1/1A14 two turns at a time, until 1A1/1A14 is firmly seated in electrical equipment cabinet 1A15.

(4) Using a socket head screw key, tighten the seven socket head capscrews on the inner right side of orderwire chassis 1A13A7.

(5) Loosen the two assembly captive screws that secure 1A13/1A14 to electrical equipment cabinet 1A15 by alternately turning each assembly captive screw two turns at a time until the captive screws rotate freely.

(6) Grasp the two handles on 1A13/1A14 and carefully remove 1A13/1A14 from electrical equipment cabinet 1A15.

(7) Remove the 12 mounting screws and lock washers that secure the rear cover to orderwire chassis 1A13A7. Being careful not to damage any of the wires connected to the plug on the rear cover, slide the rear cover away from the orderwire chassis to provide access to the interior of orderwire chassis 1A13A7.

(8) Insert the remaining socket head capscrew, removed in a(10) above, into the inner right side of orderwire chassis 1A13A7 and tighten it using the socket head screw key.

(9) Replace the rear cover removed in step b(7) and secure with the 12 mounting screws and lockwashers.

(10) Insert plug-in component 1A13A1 into its proper position in orderwire chassis 1A13A7 and tighten the two captive screws that secure 1A13A1 to 1A13A7.

(11) Carefully insert plug-in components 1A13A2 through 1A13AS into their proper positions in orderwire chassis 1A13A7 making certain that each plug-in component is properly seated in the guide rails located on the upper and lower portion of orderwire chassis 1A13A7.



(12) Carefully push plug-in components 1A13A2 through 1A13A5 into orderwire chassis 1A13A7 until the outer edge of each plug-in component is flush with the outer edge of the guide rails.

(13) Close the hinged door of orderwire chassis 1A13A7 and tighten the two hinged door captive screws.

(14) Insert orderwire-electrical frequency Synthesizer 1A13/1A14 into electrical equipment cabinet 1A15. Alternately tighten the two A-q n3ly captive screws on 1A13/1A14 two turns at a ;time until 1A13/1A14 is firmly seated in electrical equipment cabinet 1A15.

(15) Reconnect coaxial cable 1A15W16 to ;he OUTPUT J8 connector on electrical frequency synthesizer 1A14.

(16) Set the POWER ON/OFF switch on meter panel assembly 1A15A8 to ON.

### 3-31. Replacement of Electrical Equipment Chassis 1A14A10

(fig. 3-16)

#### a. Removal.

(1) Perform steps (1) through (11) of )paragraph 3-30a.

(2) Remove plug-in components 1A14A1 through 1A14A8 from electrical equipment chassis 1A14A10. (TM 115820-695-12).

#### b. Replacement.

(1) Install plug-in components 1A14A1 through 1A14A8 in replacement electrical equipment chassis 1A14A10 (TM 11-5820-695-12).

(2) Perform steps (1) through (16) of para-raph 330b.

### 3-32. Removal of Plate Assembly 1A16 (fig. 3-1)

#### a. Removal.

(1) Remove power from T-1054(P)/GRC-144(V) or T-1054(P)A/GRC-144(V) (para 3-20a).

(2) Remove power supply 1A1 (para 3-22a (2) through (6)).

#### CAUTION

**Removal of rigid coaxial cables must be performed carefully to prevent damage to the rigid coaxial cables.**

(3) Disconnect rigid coaxial cable 1W17 (TM 11-5820-695-12).

(4) Disconnect the noncaptivated ends of coaxial cables 1A2W1, 1A2W2, 1A3W1, 1A16W27'W9 and 1A15W16 (fig. 3-113).

(5) Loosen the two captive screws securing components 1A2, 1A3, 1A5 and 1A11 to plate assembly 1A16 and remove the componmts.

(6) Disconnect main harness plug LA16W25P1 (fig. 32) from connector 1A15W27J1 (fig. 3-).

(7) Disconnect coaxial cable 1AIW26 from 1A16AT1J2 (fig. 3-13 and 3-15) by unscrewing the knurled portion of type N connector 1A15W26P1.

(8) Disconnect coaxial cable 1W25 from 1DC1J2 (fig. 3-13 and 3-15) by unscrewing the knurled portion of type N connector 1W25P1 (fig. 32).

(9) Using masking tape, fasten coaxial cables 1A15W27W9 and 1A15W16 to the sides of the electrical equipment cabinet 1A15.

(10) Using a long blade screwdriver, loosen the two plate assembly captive screws located between the cabinet wall and left side of the radio test set (fig. 32).

(11) Remove the ten plate assembly screws (four on left side and six on the right side) that secure plate assembly 1A16 to electrical equipment cabinet 1A15 (fig. 3-2).

(12) Slowly pull the plate assembly 1A16 out of the electrical equipment cabinet 1A15.

#### b. Replacement.

(1) Carefully insert plate assembly 1A16 into its approximate position in electrical equipment cabinet 1A15.

(2) Holding the plate assembly in place, connect main harness plug 1A16W25P1 (fig. 315), removed in step a.(6) above to connector 1A56W27J1 (fig. 3-3).

(3) Observing the plate assembly guide pins (fig. 3-) slowly insert plate assembly 1A16 into electrical equipment cabinet 1A15 until it is flush mounted over the guide pins.

(4) Using the ten plate assembly screws and lockwashers removed in step a(1) above, secure plate assembly 1A16 to electrical equipment cabinet 1A15.

(5) Using a long blade screwdriver, tighten the two plate assembly captive screws that were loosened in step a(10) above.

(6) Connect coaxial cable 1A15W26, re moved in step a(7) above, to connector 1A16A1'15J2.

(7) Connect coaxial cable 1W25, removed in step w(8), to connector 1DO1J2.

(8) Using the guide pins, on the rear of components 1A2, 1A3, 1A5 and 1A11, removed in step a(5) above, carefully insert the components into their respective positions on plate

assembly 1A16. Tighten the two captive screws on each component.

(9) Remove the masking tape securing coaxial cables 1A15W27W9 and 1A15W16 to the sides of electrical equipment cabinet LA15.

(10) Reconnect coaxial cables 1A2W1, 1A2W2, 1A3W1, 1A15W27W9, and 1A15W16 to the components (fig. 8-13).

#### CAUTION

**Replacement of rigid coaxial cables must, be performed carefully to prevent damage to the rigid coaxial cables.**

(11) Connect rigid coaxial cable 1W17 between 1HYJI and 1AIJ5 (TM 114820-69612).

(12) Replace power supply 1A1 (para 8-22g (6) through (10)).

(13) Restore power to T-1054(P)/GRC-144(V) or T-1054(P)A/GRC-144(V) (para 3-20b).

### 3-33. Replacement of Parts on or behind Plate

#### Assembly 1A1 6 (fir. 8 and 3-16)

Plate assembly 1A16 must be removed from electrical equipment cabinet 1A15 (para 3-82) to gain access to any of the parts mounted on the rear of plate assembly 1A16 (fig. 315) or to any of the parts mounted on electrical equipment cabinet 1A1S behinds plate assembly 1A16 (fig. 3-8). Procedures are provided for replacement of power transformer 1A15A1OT1 (para 8-4), parts in the radio test set (para -85), and radio frequency bandpass filter 1PO, radio frequency low pass filter 1FIA, elbow adapter 1OP4, or directional coupler LDC1 (para 386). All other parts can be replaced using general replacement techniques (para 3-19).

### 3-34. Replacement of Power Transformer 1A15A1OT1 (fig. 8)

#### a. Removal.

(1) Remove power from T-1054(P)/GRC144(V) or T-1054(P)A/GRC-144(V) (para 3-20a).

(2) Remove plate assembly 1A16 (para 832a).

(3) Remove the three cable clamp nuts securing cable harness 1A15A1OW1 (fig. 8-) to cabinet wall. Do not remove the cable clamps from the cable harness.

(4) Loosen and remove the four screws, four washers and four nuts securing the base of power transformer 1A15A1OT1 to mounting bracket.

(5) Tag and unsolder wires connected to terminals of power transformer 1A16A1OT1.

(6) Exercising care not to put stress on cable harness wiring, remove power transformer 1A15A1OT1 from electrical equipment cabinet 1A15.

#### b. Replacement.

#### CAUTION

**Exercise care while soldering the cable harness leads to the power transformer terminals to prevent damage to the cable harness leads or power transformer terminals.**

(1) Solder wires removed in step a(5) above to correct terminals of replacement power transformer 1A15A1OT1.

(2) Insert the four mounting screws and washers, removed in step a(4) above, into the power transformer base mounting holes and then carefully lower 1A15A1OT1 onto the mounting bracket while aligning the visible mounting screws with the bracket mounting holes.

(3) Replace the four nuts on power transformer 1A15A1OT1 mounting screws and secure 1A15A1OT1 to the mounting bracket by tightening the four nuts firmly.

(4) Position and fasten the three cable clamps on cable harness 1A15A1OW1 with the three cable clamp nuts removed in step a(8).

(5) Replace plate assembly 1A16 (para 882b).

(6) Restore power to T-1054(P)/GRC-144 (V) or T-1054(P)A/GRC-144(V) (para 3-20b).

### 3-35. Replacement of Parts In Radio Test Set (p/o 1A16) (fig. 8-12)

#### a. Removal.

(1) Set the POWER ON/OFF switch on meter panel assembly 1A15A8 to OFF.

(2) Loosen the two set screws securing each selector knob on the radio test set meter panel and remove the selector knobs.

(3) Remove the two screws securing crystal mixer 1A16Z1 mounting bracket to the radio test set meter panel.

(4) Remove the three screws securing variable attenuator 1A16AT1 to rear of the radio test set meter panel.

(5) Remove the eight screws securing the radio test set meter panel to the radio test set enclosure.

(6) Pull the radio test set meter panel away from the radio test set enclosure until it is clear of the shaft on variable attenuator 1A16AT1, then lower the meter panel assembly.

(7) Remove the two self-locking nuts and washers from the meter terminals.

(8) Tag and remove the wire lugs connected to the meter terminals.

(9) Remove and save the three locknuts, washers, and screws securing meter 1A16M2 to the radio test set meter panel, then lift and remove meter 1A16M2.

(10) Tag and unsolder all wires connected to rotary switch 1A16S5.

(11) Remove hex-nut and washer that secures switch 1A16S5 and remove the switch.

(12) Disconnect coaxial cable 1A16W24 from crystal mixer 1A16Z1J2 and cable 1A15W26 from 1A16AT1J2.

(13) Pull variable attenuator 1A16AT1 and crystal mixer 1A16Z1 forward out of radio test set enclosure as a unit.

(14) Disconnect mating type N connectors as required, to separate variable attenuator 1A16AT1 and crystal mixer 1A16Z1 from each other.

*b. Replacement.*

(1) Assemble variable attenuator 1A16AT1 and crystal mixer 1A16Z1 together by reconnecting the mating type N connectors and mount them in the radio test set enclosure by pushing the type N connector on rear of variable attenuator 1A16AT1 through the rubber grommet at the back of the radio test set enclosure.

(2) Rotate knob shafts on variable attenuator 1A16AT1 and rotary switch 1A16S5 completely clockwise.

(3) Connect coaxial cable 1A16W24 to crystal mixer 1A16Z1 (4) Mount meter 1A16M2 to the radio test set meter panel.

(5) Replace and tighten the three screws and locknuts (and lockwashers) securing meter 1A16M2 (6) Remove the two self-locking nuts and washers from the meter terminals, then remove the shorting bar from across the meter terminals.

(7) Connect the wire lugs to meter terminals and secure them with the two self-locking nuts and washers.

(8) Mount rotary switch 1A16S5 on meter panel assembly removed in a(11) above.

(9) Replace and tighten the hex nut and washer securing rotary switch 1A16S5.

(10) Solder switch wires to rotary switch 1A16S5 terminals.

(11) Using a pair of needle nose pliers to hold crystal mixer 1A16Z1 mounting bracket, place the radio test set meter panel on the radio test set enclosure.

(12) Replace and tighten the two screws securing crystal mixer 1A16Z1 mounting bracket.

(13) Replace and tighten the three screws securing variable Attenuator 1A16AT,1.

(14) Replace and tighten the eight screws securing the radio test set meter panel to the radio test set enclosure.

(15) Replace the selector knobs on variable attenuator 1A16AT1 and rotary switch 1A16S5 and tighten the two set screws on each knob.

(16) Connect cable 1A15W26 to 1A16AT1J2. (17) Perform the T-1054(P)/GRC-144(V) and T-1054(P)A/GRC-144(V) radio test set calibration procedure (para 341).

**3-36. Replacement of Radio Frequency Sandpass Filter 1FL3, Radio Frequency Low Pass Filter 1FL4, Elbow Adapter 1CP4, or Directional Coupler 1DC1 (fig. 3-2, 3-13 and 3-15)**

Removal and replacement procedures for any of the following; radio frequency bandpass filter 1FL3, radio frequency low pass filter 1F4IA, elbow adapter 1CP4 or directional coupler 1DC1 require assembly and disassembly of the remaining components. The following procedures detail the steps necessary to remove all three components as a single item which can be further disassembled when removed from T-1054(P)/GRC-144(V) or T-1054(P)A/GRC-144(V).

(1) Remove power from T-1054(P)/GRC-144 (6) or T-1054(P)A/GRC-144(V) (para 3-20ag).

(2) Remove plate assembly 1A16 (para 332a).

(3) Disconnect the following coaxial cables from components mounted on plate assembly 1A16: 1A9W9 from radio frequency bandpass filter 1FL3 connector J1, 1A16W24 from directional coupler 1DC1 connector RF INCIDENT Jo, 1A16W22 from directional coupler 1DO1I connector INCIDENT J4, and 1A16W26 from directional coupler 1DC1 connector REFLECTED J6.

(4) Remove the four screws and washers securing radio frequency bandpass filter 1FL3 to plate assembly 1A16.

(5) Disconnect radio frequency bandpass filter 1FL3 from radio frequency low pass filter 1FL4 by rotating the knurled connector on 1FIA in a clockwise direction. Remove 1FL3 from plate assembly 1A16.

**NOTE**

**If radio frequency bandpass filter 1FL3 is the only component to be replaced; proceed to step b(6) below.**

(6) Disconnect radio frequency low pass filter 1FIA from elbow adapter 1CP4 by rotating the knurled connector on 1FIA in a counterclockwise direction. Remove 1FIA by pulling it through the connector access hole in plate assembly 1A16.

**NOTE**

**If radio frequency low pass filter 1FL4 is the only component to be replaced; proceed to step b(8) below.**

(7) Disconnect elbow adapter 1CP4 from directional coupler 1DC1 by rotating the knurled connector on 1CP4 in a counterclockwise direction. Remove elbow adapter 1CP4.

**NOTE**

**If elbow adapter 1CP4 is the only component to be replaced; proceed to step b(2) below.**

(8) Remove the four screws and washers securing directional coupler IDC1 to 1DC1 mounting bracket.

*b. Replacement.*

(1) Mount directional coupler 1DC1 to 1DC1 mounting bracket and loosely secure 1DC1 in place using the four screws and washers removed in step a(8). Do not tighten the four screws at this time.

(2) Mate the knurled connector on elbow adapter 1OP4 with the connector on the bottom of directional coupler 1DC1 and rotate the knurled connector clockwise two complete turns.

(3) Mate the connector on radio frequency bandpass filter 1FL3 with the knurled connector on radio frequency low pass filter 1FL4A. Tighten the knurled connector.

(4) Insert radio frequency low pass filter 1FL4 through the connector access hole in plate assembly 1A16.

(5) Mate the knurled connector on radio frequency low pass filter 1FAL4 with the connector on elbow adapter 1CP4. Tighten the knurled connectors on 1FIL4A and 1CP4.

(6) Align the mounting holes on radio frequency bandpass filter 1FL3 with the mounting holes

in plate assembly 1A16. If the mounting holes on 1FL3 cannot be aligned with the mounting holes in 1A16, loosen the four IDC1 mounting bracket screws (fig. 3-2) and then align the mounting holes.

(7) Insert and tighten the four screws and washers that secure radio frequency bandpass filter 1FL3 to plate assembly 1A16.

(8) Tighten the four 1DC1 mounting bracket screws if they were loosened in step (6) above.

(9) Tighten the four screws that secure 1DC1 to the IDC1 mounting bracket.

(10) Reconnect coaxial cables 1A9W9 to radio frequency bandpass filter 1FIA, 1A16W24 to directional coupler IDC1 connector RF INCIDENT J3, 1A16W22 to directional coupler LDC1 connector INCIDENT J4, and IAIEW2B to directional coupler 1IDC1 connector REFLECTED J5.

**NOTE**

**If the four 1DC1 mounting bracket screws were loosened in step (6) above; it may be necessary to reposition the plate assembly guide bracket (fig. 68) to permit installation of plate assembly 1A16. If the plate assembly guide bracket must be repositioned, loosen the four screws that secure the guide bracket until the plate assembly guide bracket can be moved up or down but still maintains its position when released, then insert plate assembly 1A1C into position in electrical equipment cabinet 1A16. Remove plate assembly 1A1I and tighten the four screws that secure the plate assembly guide bracket being sure that the guide bracket does not move up or down.**

(11) Replace plate assembly 1A16 (para 832b).

(12) Perform the T-1054(P)/GRV-144V) and T-1054(P)A/GRC-144(V) rf power metering circuit calibration procedure (para 3-57) 3-37. Repair and Replacement of T-1054(P)/ GRC-144(V) and T-1054(P)A/GRC144(V) Connectors (fig. 3-14, 3-26)

a. General. Repair of connectors in T-1054(P)/GRC-144(V) and T-1054(P)A/GRC144(V) requires either: the replacement of the defective connector (solder type nonremoveable contacts), or the replacement of defective connector contacts (crimp or solder type removable contacts). A listing of

T-1054(P)/GRC-144(V) and T-1054(P)A/GRC 144(V) connectors is included in the chart (b below). The chart also includes a listing of the applicable tools (fig. 3-26), a paragraph reference specifying the applicable repair procedure, and a figure reference for identification of the connector.

Repair procedures are covered in c through f below.

b. T-1054(P)/GRC-144(V) and T-1054(P) A/GRC-144(V) Connector Chart.

Connector	Extraction/ insertion tool	Crimping tool	Procedure paragraph	Figure reference
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**NOTE**

**Connectors 1A15J15, 1A15316 and 1A15310 identified with an asterisk are not part of Transmitter, Radio T-1054(P)A/GRC-144(V).**

1A1AP1.....	MS 18278 Size 20/None.....	MS3191-4 with Head.....	3-7 - 3-9	
		Assy W26		
1A1A13P2.....	Same .....	Same .....	3-37c.....	3-9
1A15AIDWIXA1A.....	Same .....	Same .....	3-37c.....	3-3
1A15W27XA1B.....	Same .....	Same .....	3-37c.....	3-3
1A16W27XA2A.....	Same .....	Same .....	3-37c.....	3-3
A1W27XA12B.....	Same .....	Same .....	3-37c.....	3-3
1A15W2tTXA13B.....	Same .....	Same .....	3-37c.....	3-3
1A16W25XA2.....	Same .....	Same .....	3-37c.....	3-15
1A16W25XA13.....	Same .....	Same .....	3-37e.....	3-15
1A16W26XA4.....	Same .....	Same .....	3-37c.....	3-15
IA1625XASA.....	Same .....	Same .....	3-37c.....	3-15
1A16W25XA7.....	Same .....	Same .....	3-37c.....	3-15
1A16W25XA8.....	Same .....	Same .....	3-37c.....	3-15
A16W25XA11.....	Same .....	Same .....	3-37c.....	3-15
1A15W27J13.....	CET-C6B/None .....	None .....	3-37d.....	3-5 and 3-5.1
1A15J14.....	CET-C6B/None .....	None .....	3-37d.....	3-5 and 3-5.1
*1A1S5J15.....	CET-06B/None.....	None .....	3-37d.....	3-6
*1A15J16.....	CET-C6B/None .....	None .....	3-37d.....	3-4
1A15W27P2.....	CET-C6B/None .....	None .....	3-37d.....	3-6 and 3-5.1
1A15W27XA13A.....	CET-COB/None.....	None .....	3-37d.....	3-3
1A16W25XA5B.....	CET-COB/None.....	None .....	3-37d.....	3-15
1A15W7XA14.....	CET-COB/None.....	None .....	3-37d.....	3-3
1A15WV27J1.....	MS4256 R20/A20.....	MS 3191-4 with Head	3-37e.....	3-3
		Assy W1		
1A16W25P1.....	MS24256 RaO/A20.....	MIS 3191-4 with Head.	3-37e.....	3-15
		Assy W1		
1A1A13XA1 through 1A1A13XA4	None required.....	None required.....	3-7f.....	3-9
1A1A13XA6 through IAIA13XA12	None required.....	None required.....	3-37f.....	3-9
1A15A6J18.....	None required.....	None required.....	3-37f.....	3-7
1A15J.....	None required.....	None required.....	3-37f.....	3-7 and 3-7.1
*1A1J10.....	None required.....	None required.....	3-37f.....	3-7
1A16J20.....	None required.....	None required.....	3-37f.....	3-7
1A15P3.....	None required.....	None required.....	3-37f.....	3-7
1A165W27J4.....	None required.....	None required.....	3-37f.....	3-7
1A15W27J5.....	None required.....	None required.....	3-37f.....	3-7

**NOTE**

**The connectors listed below pertain to the T-1054(P)A/GRC-144(V) only.**

1A15322.....	None required.....	None required.....	3-37F.....	3-7.1
1A15J22.....	None required.....	None required.....	3-37F.....	3-7.1
1A15P4-	MS24256 R20/A20	MS3191-4 with	3-37E	3-13.1
		head assy W 1		
1A15P5.....	Same.....	Same.....	3-37E.....	3-13.1

c. *Repair of Rectangular Connectors With Crimp Type Removable Contacts.* This type of connector incorporates crimp type removable contacts. The procedure for extracting contacts is given in (1) below. Replacement of the contact pin requires stripping of the wire to the proper length, crimping of the new contact to the wire and insertion of the contact into the connector using the contact insertion tool. The procedure for stripping, crimping and inserting contacts is given in (2) below.

(1) *Contact extraction.*

(a) Place wire to be removed into the tip of extraction tool MS18278 size 20.

(b) Insert tool tip into contact cavity until tip bottoms against contact shoulder, releasing the retaining clip tines; hold wire against the tool with your finger and withdraw tool and contact from the rear of the connector.

(2) *Contact replacement.*

(a) Strip wire back 3/16 inch.

(b) Insert contact and wire into locator head of crimping tool MS3191-4 with head assembly W25. Use pin contacts 330-5291-000 or socket 031-10007-000 (whichever is applicable).

(c) Squeeze tool handles firmly and completely to insure a proper crimp.

**NOTE**

**Tool will not release unless the crimp indentors in the tool head have been fully actuated.**

(d) Inspect crimp connection, check that crimped area is between the inspection hole and

the extreme rear of the crimp barrel. Bare wire strands should be visible through the inspection hole.

- (e) Insert contact into the connector.
- (f) Reassemble connector hardware.

*d. Repair of Rectangular Connectors With Solder Type Removable Coaxial Contacts (fig. 3-14).* This type of connector incorporates captivated solder pot contacts in combination with snap-in coaxial contacts. The two types of coaxial contacts used, straight coaxial shell and right angle coaxial shell, are removable. The following procedure describes how to extract and insert the two types of coaxial contacts.

(1) *Straight coaxial shell.*

- (a) Extract the defective coaxial contact from the connector using extraction tool CETC6B.
- (b) Unsolder the outer ring from the braid through the cross drilled solder hole and slide outer ring back over the cable jacket.
- (c) Unsolder the coaxial center conductor separating the coaxial cable from the coaxial shell.
- (d) Insert the cable dielectric and center conductor through the next coaxial contact inner sleeve with the braid on outside of sleeve.
- (e) Solder the cable center conductor to the coaxial shell center contact.
- (f) Slide outer ring forward until flush with coaxial shell confining the braid between outer ring and inner sleeve.
- (g) Soft solder the coax shell outer ring to the braid through the cross drilled solder hole.
- (h) Insert replacement straight coaxial shell contact into the connector.

(2) *Right angle coaxial shell.*

- (a) Extract the defective coaxial contact from the connector using extraction tool CETC6B.
- (b) Unsolder the outer ring from the braid through the cross drilled solder hole and slide outer ring back over the cable jacket.
- (c) Unsolder and remove the access cap, and unsolder the coaxial center conductor; separate the coaxial cable from the coaxial shell.
- (d) Insert the cable dielectric and center conductor through the new coaxial contact inner sleeve with the braid on the outside of sleeve.
- (e) Soft solder the cable center conductor to the coaxial shell center contact.
- (f) Slide outer ring forward until flush with coaxial shell confining the braid between outer ring and inner sleeve.

(g) Soft solder the outer ring to the braid through the cross drilled solder hole.

(h) Soft solder (or stake) the cap in place on the connector.

(i) Insert replacement right angle coaxial shell contact into the connector.

*e. Repair of Round Connectors With Crimp Type Removable Contacts.* The military specifications (MS) connectors use MI-C-26482 type hardware. These connectors incorporate crimp style removable contacts. The pin contacts adhere to military standard MS3192 (A20A); the socket contacts adhere to military standard MS3193 (A20A). The following procedure describes how to extract, crimp and insert contacts in the MS type connectors.

**CAUTION**

**Do not rotate or twist the extraction tool in the connector.**

(1) *Contact extraction.* Hold connector securely, pull plunger of extraction tool MS24256R20 back and center tool tube over contact from the front of the insulator. Using moderate pressure, insert tube into contact cavity. Steadily press plunger handle with palm of hand until the contact is released; then, pull contact free from the rear of connector.

(2) *Contact replacement.*

- (a) Strip wire back 3/16 inch.
- (b) Insert stripped wire into contact crimp pot, wire must be visible through inspection hole.
- (c) Cycle the crimping tool once to be sure the indentors are open. Insert the contact and wire into the locator. Squeeze tool handles firmly and completely to insure a proper crimp.

**NOTE**

**Tool will not release unless the crimp indentors in the tool head have been fully actuated.**

- (d) Release crimped contact and wire from tool. Inspect the crimped contact; be certain that the wire is visible through the contact inspection hole.
- (e) Insert the wired contact into the rear of connector insulator. Holding the connector securely, position insertion tool MS24256A20 behind the contact. Butt shoulder in tool against the back of contact in barrel. Push tool straight into contact cavity until contact snaps into position. Assure that contact is locked by pulling lightly on the wire.
- (f) Reassemble connector hardware.

*f. Replacement of Connector With Nonremoveable Contacts.* The individual contacts of these connectors cannot be removed. Therefore, the connector must be replaced when any of the connector contacts or pins, or the connector itself is defective or damaged. Replacement of the connector is accomplished by transferring each lead from the defective connector to the identical terminal contact on the replacement connector. The general information provided in the parts replacement techniques (para 819) should be reviewed before replacing this type of connector. Care should be exercised when unsoldering individual wire leads from the connector terminals to prevent scorching or burning through the insulation of adjacent wire leads. Do not overheat the connector terminal and wire lead which would cause solder to flow upward along the individual strands of wire resulting in a stiff and brittle lead that could easily break or snap when used with the replacement connector.

### **3-38. Receiver, Radio R-1467(P)GRC-144(V) and R-1467(P)A/GRC-144(V) Repairs**

**Procedures required to remove or replace parts which are not obvious or require special handling are given in paragraphs 3-39 through 862.** Prior to removal or replacement of any part in the R-1467(P)/GRC-144(V) or R-1467(P)A/GRC-144 (V) procedures for power removal given in paragraph 3-38a, unless otherwise stated, must be performed. Procedures for restoring power are given in b below. Procedures for removal and replacement of components with rigid coaxial cables are covered in TM 11-5820-695-12.

#### *a. Remove Power.*

(1) Set the POWER ON/OFF switch on meter panel assembly 2A15A2 to OFF (fig. 317).

(2) Set the POWER ON/OFF switch on meter panel assembly 1A46A8 to OFF (fig. 3-1).

(3) Disconnect the external ac power source cable from AC POWER INPUT connector 2A15 A6J5 located on the top rear section of electrical equipment cabinet 2A15 (fig. 3-20).

#### *b. Restore Power.*

(1) Reconnect the external ac power source cable to AC POWER INPUT connector 2A,16A5J5 located on top rear section of electrical equipment cabinet 2A15.

(2) Set the POWER ON/OFF switch on meter panel assembly 1A15A8 to ON.

(3) Make the following checks on T-1054 (P)/GRC-144(V) or T-1054(P)A/GRC-144(V).

(a) The 5 AMP SLO-BLO neon fuse indicator on meter panel assembly LA11A8 is not lighted.

(b) All power supply 1A1 indicator lamps are lighted green.

(c) 6V and 28V indicator lamps on electrical frequency synthesizer 1'A,14 are lighted green.

(4) Set the POWER ON/OFF switch on meter panel assembly 2A15A2 to ON.

(5) Make the following checks on R-1467(P)/GRC-1440V): (a) The SDO-B30 POWER 5 AMP and TDA 1 AMP neon fuse indicators on meter panel assembly 2A15A2 are not lighted.

(b) All power supply 2A1 indicator lamps are lighted green.

(c) '5V and 28V indicator lamps on electrical frequency synthesizer 2A14 are lighted green.

#### **NOTE**

**Radio communications can normally be established 5 to 10 minutes after the AN/GRC-144(V) radio sets are turned on if the ambient temperature in the shelter is maintained above +70 degrees Fahrenheit.**

### **3-39. Replacement of Parts on Meter Panel Assembly 2A15A2 (fig. 3-17 through 3-19)**

Prior to removing and replacing parts on meter panel assembly 2A15A,2, perform the procedures listed in paragraph 3-88a to remove equipment power. After a part is replaced, perform the procedures in paragraph 3-38b to restore equipment power.

#### *a. Replacement of Meter 2A15AIM1 (fig. 3 17 through 3-19).*

##### *(1) Removal.*

(a) Loosen the two meter panel captive screws (fig. 3-17).

(b) Swing the meter panel assembly 2A15A2 upward and lock it in an upright position by use of the panel locking latch (fig. S-19).

(c) Remove the two nuts and washers from the meter terminals.

(d) Tag and remove the wire lugs connected to the meter terminals.

(e) Release the meter panel assembly 2A15A2 and position it downward until it is perpendicular to electrical equipment cabinet 2A15. Support or tie meter panel assembly 2A15A2 in the perpendicular position.



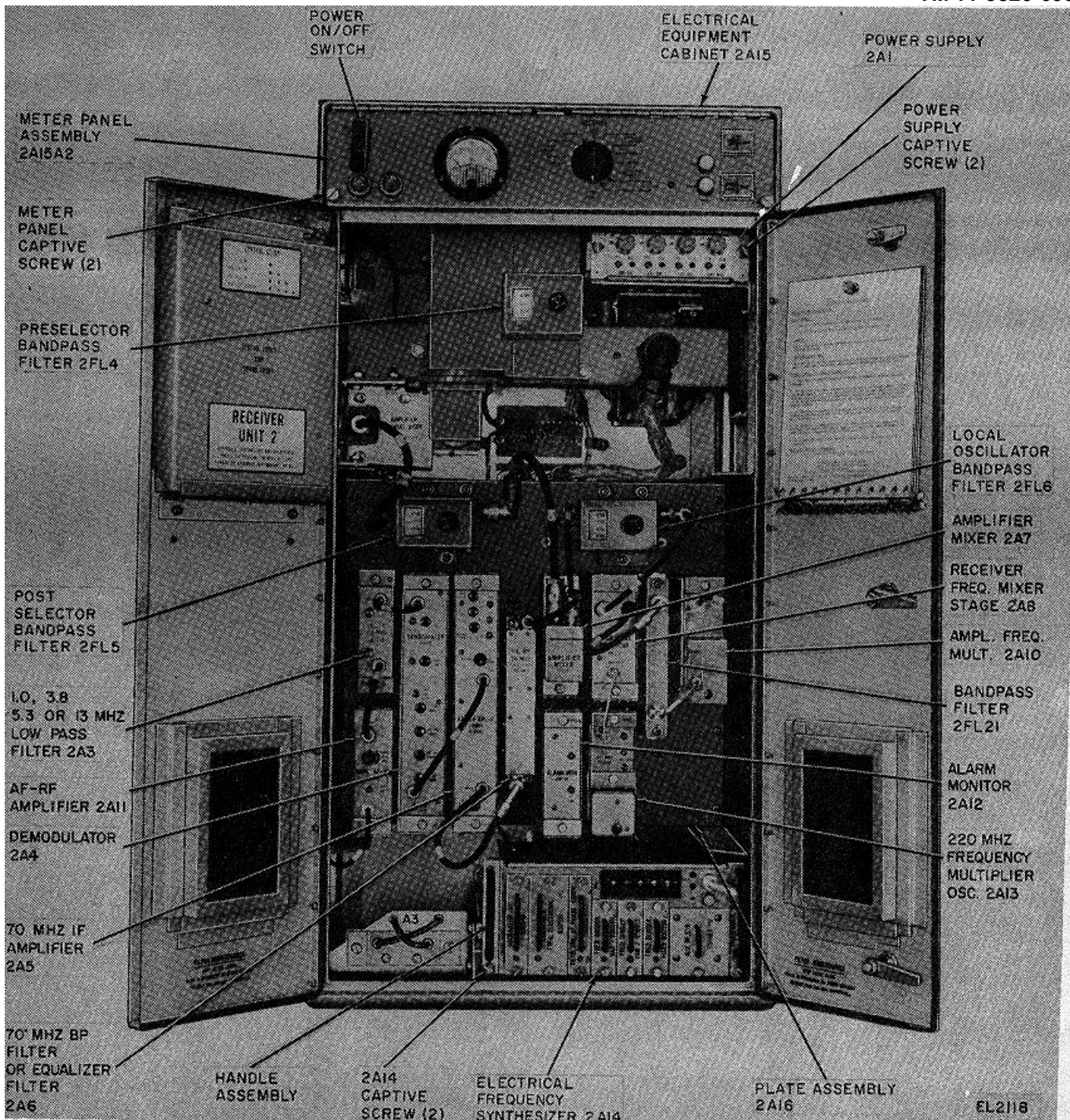


Figure 3-17. Receiver, Radio R-1467(P)/GRC-144(V) and R-1467(P)A/GRC-144(V)

(f) Remove and save the three lock nuts and screws that secure meter 2A15A2M1 to meter panel assembly 2A15A2.

(g) Remove the meter from the meter panel assembly.

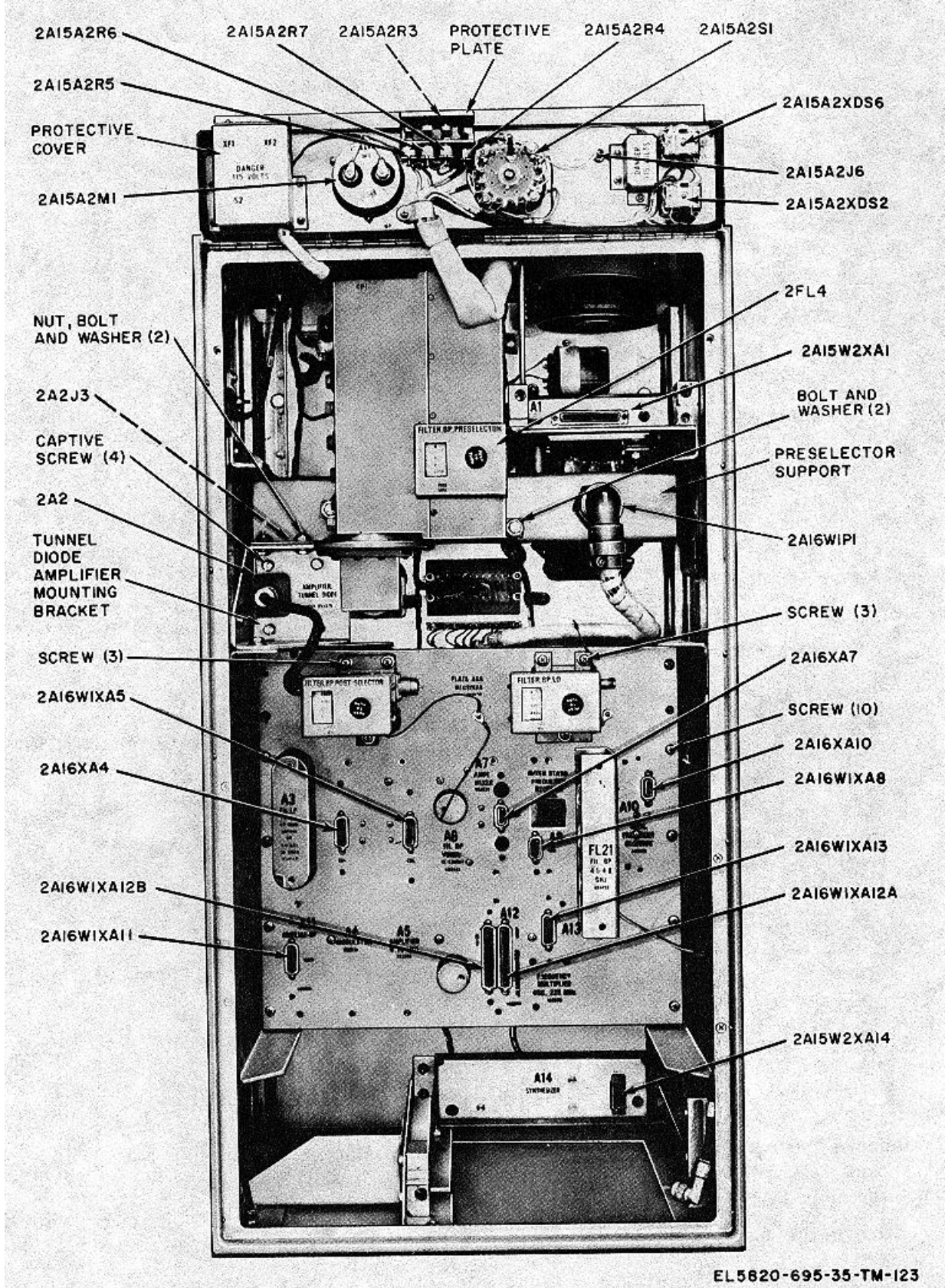
(2) Replacement.

(a) Place new meter 2A15A2M1 in position on front of meter panel assembly 2A15A2 and

align the meter mounting holes with those of the panel assembly.

(b) Secure the meter in place with the three locknuts and screws removed in (1)(f) above.

(c) Position the meter panel assembly 2A15A2 upward and lock in position by use of the panel locking latch.



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Figure 3-18. Electrical equipment cabinet 2A15, partially disassembled, parts location.



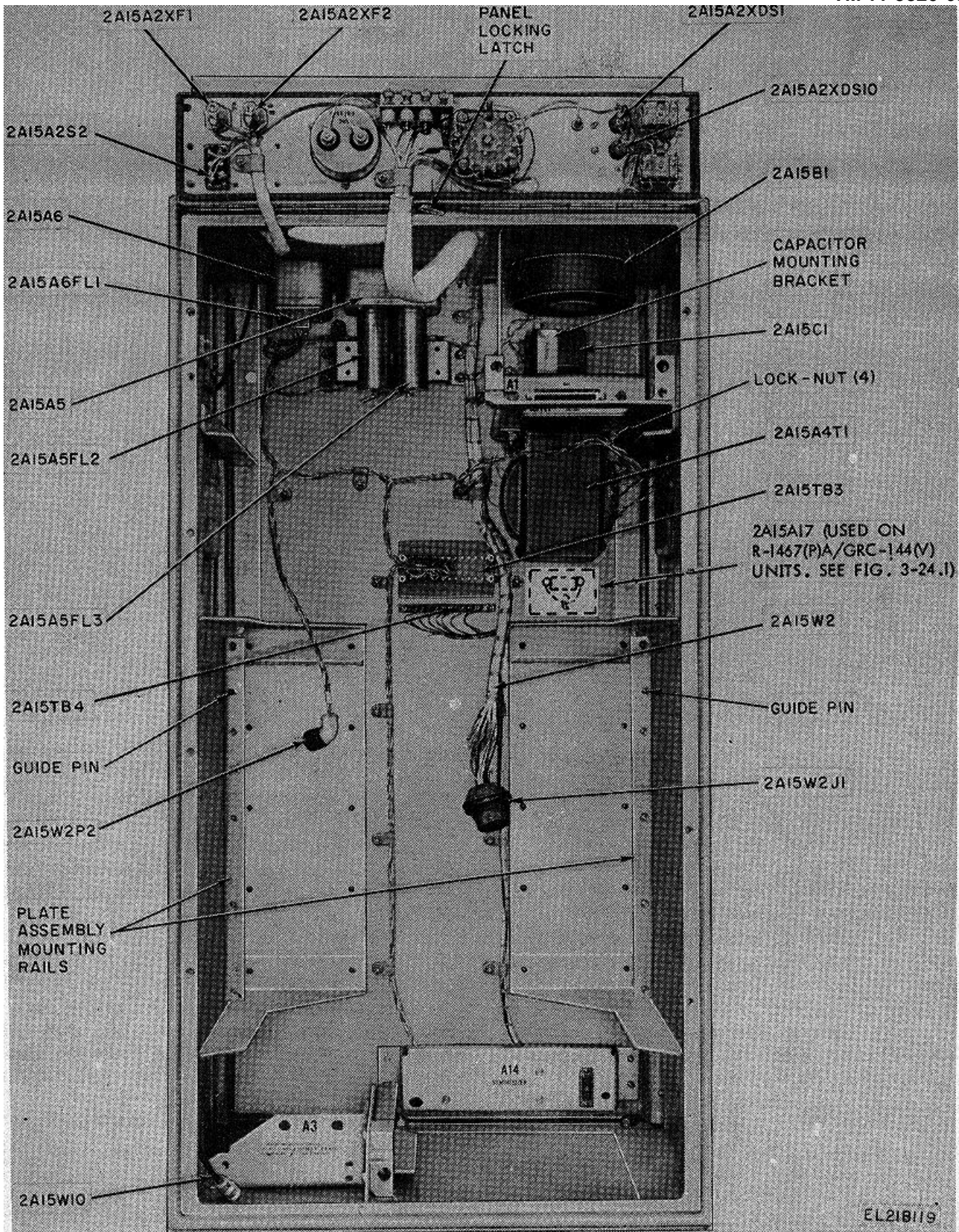
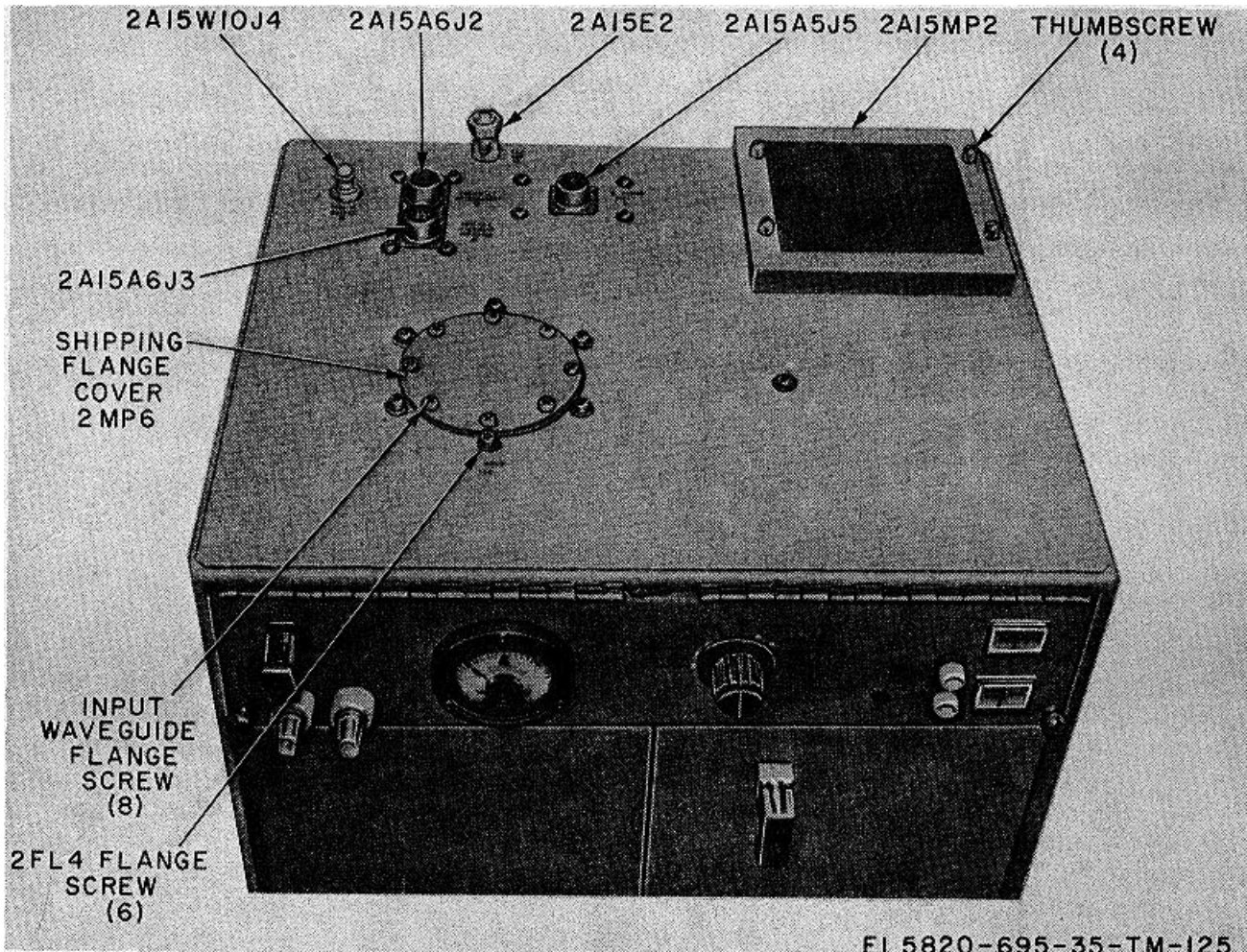


Figure 3-19. Electrical equipment cabinet 2A15 with plate assembly 2A16 removed, parts location.



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**Figure 3-20. Receiver, Radio R-1467/GRC-144, top view, parts location.**

(d) Remove the two nuts, washers, and the shorting bar from the new meter terminals.

(e) Connect the wire lugs removed in step (1) (d) to their respective meter terminals and fasten lugs to terminals with the nuts and washers removed in step (d).

(f) Place the shorting bar removed from the new meter on the terminal lugs of the old meter and fasten in place with its terminal hardware.

(g) Release the meter panel assembly 2A15A2 and position it downward until it rests against electrical equipment cabinet 2A15.

(h) Secure meter panel assembly 2A15A2 in place by finger tightening the two meter panel captive screws.

(i) Calibrate receiver meter 2A15A2M1 (para 3-63).

**b. Replacement of Indicator Light Assembly 2A15A2XDS2 or 2A15A2XDS6 (fig. 3-8 and 3-18).**

(1) **Removal.** Perform steps (1) (a) through (j) of paragraph 3-21b to remove indicator light assembly 2A15A2XDS2 or 2A15A2XDS6.

(2) **Replacement.** Perform steps (2) (a) through (k) of paragraph 3-21b to replace indicator light assembly 2A15A2XDS2 or 2A15A2XDS6.

**c. Replacement of Potentiometer 2A15A2R3 Through 2A15A2R7 (fig. 3-18).** To remove a potentiometer, remove equipment power (para 338a), replace the defective potentiometer, restore equipment power (para 3-8b), and then perform the applicable calibration procedure listed in the chart below.

<b>POTENTIOMETER CALIBRATION</b>	
<i>Potentiometer</i>	<i>Calibration procedure</i>
2A15A2RS, 2A15A2R4, 2A15A2R5, and 2A15A2R6.	Calibration of R-1467/GRC 144 local oscillator metering circuits. (para 3-65).
2A15A2R7 .....	Calibration of R-1467/GRC-144 traffic metering circuit (para 3-64).



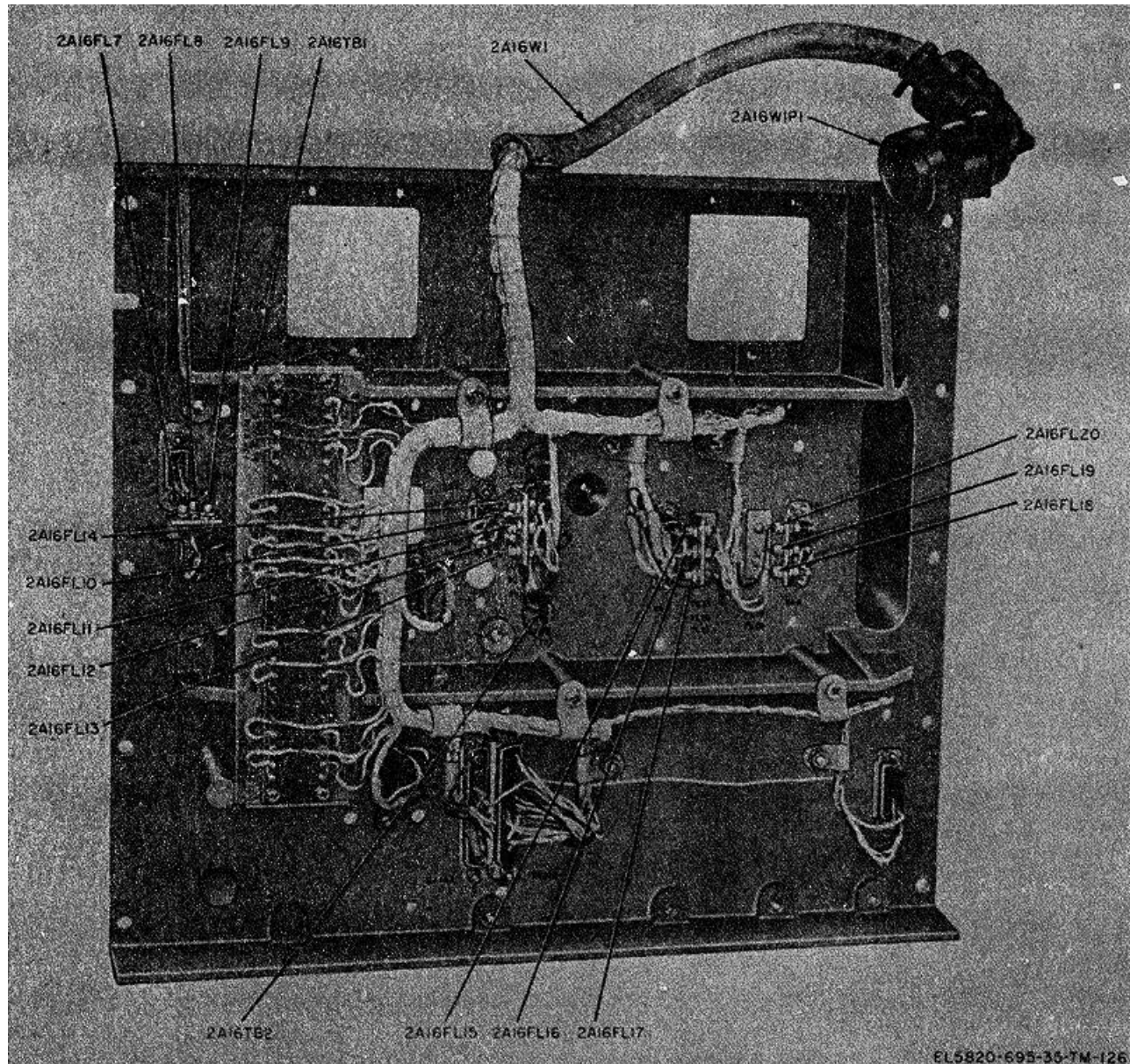


Figure 3-21. Plate assembly 2A16, rear view, parts location.

### 3-40. Replacement of Parts in Power Supply Chassis Assembly 2A1A5

(fig. 3-17, 3-19, 3-22, and 3-23)

To replace any part in power supply chassis assembly 2A1A5, remove power supply 2A1 (a below) and refer to applicable replacement procedure (b through f below) for the part to be replaced. After the part has been replaced, refer to the steps in g below for replacement of power supply 2A1. Parts located on terminal board 2A1A5TB1 are removed using standard soldering techniques (para 3-19).

a. Removal of Power Supply 2--A1 (fig. 3-17).

(1) Set the POWER ON/OFF switch on meter panel assembly 2A15A2 to OFF.

(2) Loosen the two meter panel captive screws on meter panel assembly 2A15A2 (fig. 3817).

(3) Position meter panel assembly upward and lock it in position by use of the panel locking latch (fig. 8-19).

(4) Alternately unscrew each power supply captive screw (fig. 3-17) one or two turns at a time. Repeat this procedure until both captive screws rotate freely.

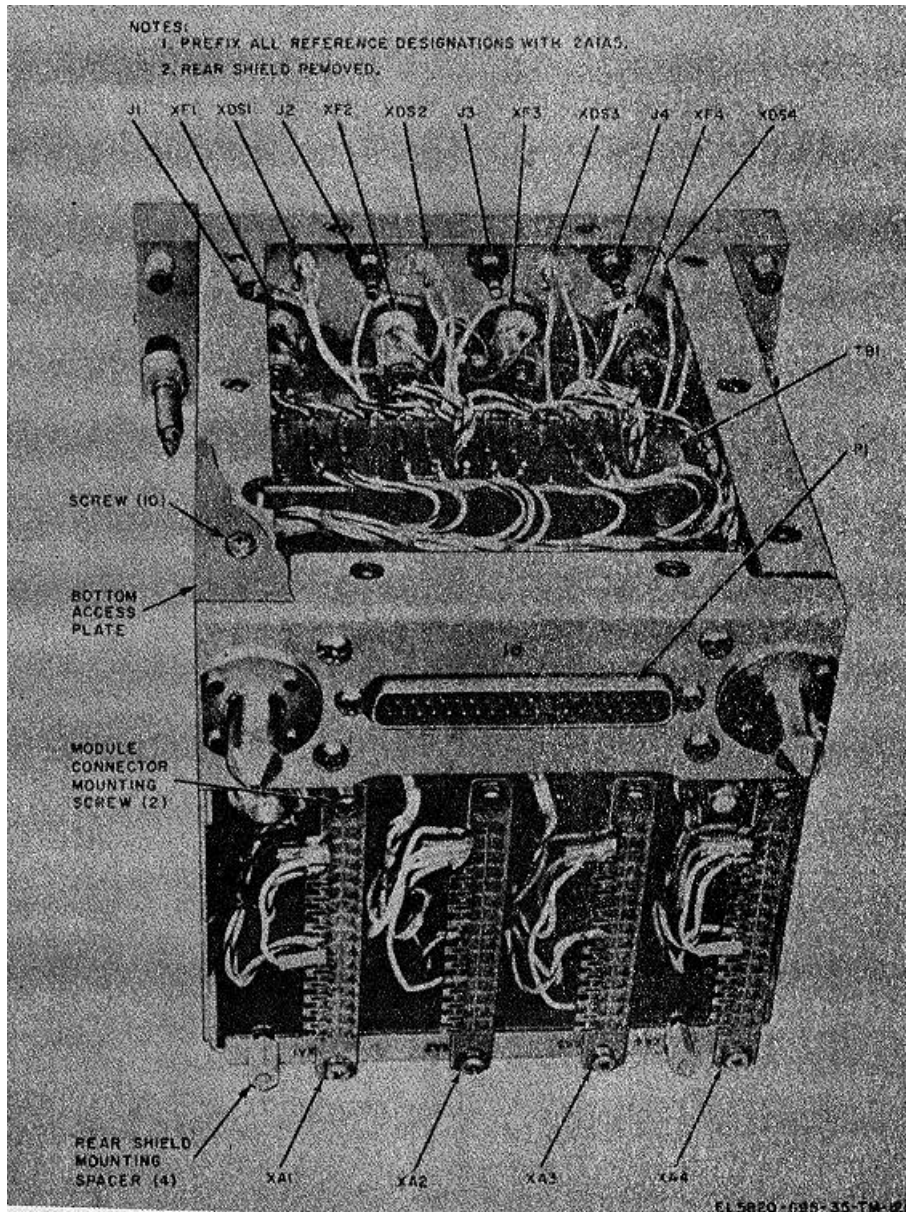


Figure 3-22. Power supply chassis assembly 2A1A5, parts location.

(5) Slide power supply 2A1 out of electrical equipment cabinet 2A15.

(6) Loosen the two captive screws that secure 15/28v voltage regulator 2A1A1 to power supply chassis assembly 2A1A5 and then remove 2A1A1 from the chassis.

(7) Repeat step (6) for regulators 2A1A2, 2A1A4, and 2A1A3.

*b. Removal of Rack Mounted Component Connector 2A1A5XA1 Through BA1A5XA4 (fig. 3-22).*

(1) Remove the four screws and associated washers securing rear shield to power supply chassis assembly 2A1A5.

(2) Tag and unsolder wires connected to component connector terminals of the connector to be replaced.

(3) Remove the two screws, two nut and washers securing component connector to power supply chassis assembly 2A1A5 and remove the connector.

*c. Replacement of Rack Mounted Component Connector 2A1A5XA1 Through 2A1A5XA.(fig. 3-22).*

(1) Mount replacement connector in place of removed connector using the two screws, two nuts and washers removed in step *b*(3). Do not tighten the two screws and nuts.

remove lamp socket from front of power supply chassis assembly 2A1A5.

e. *Replacement of Lamp Socket £AIA6XDS1 through 2AIA5XDS4* (fig. 3-22).

(1) Replace lamp socket by forcing terminal end of press fitted lamp socket through front of mounting hole in power supply chassis assembly 2A1A5 and pressing lamp end until mounted snugly against power supply chassis assembly 2AIA5 frame.

(2) Solder wires removed in step d(2) to lamp socket terminals

(3) Mount and secure the bottom access plate to power supply chassis assembly 2AIA5 using the ten screws removed in step d(l).

f. *Removal and Replacement of Chassis Mounted Connector 2AIA5PI* (fig. 3-22).

(1) Turn power supply chassis assembly 2A1A6 upside down and remove the ten screws securing bottom access plate to power supply chassis assembly 2A1A6.

(2) If a connector contact requires replacement refer to the procedures provided in paragraph 3-52b for removal and replacement of connector contacts and proceed to step (7).

(3) If the connector requires replacement remove the two screws, two nuts and washers securing the connector and ground lug to power supply chassis assembly 2A1A5.

(4) Remove connector from mounting hole and insert replacement connector in mounting hole. Secure the replacement connector and ground lug in place by tightening the two screws, two nuts and washers removed in step (3).

(5) Remove a wired connector contact from the removed connector and install in the replaced connector identical contact location. Refer to paragraph 3-52b for connector pin removal and replacement.

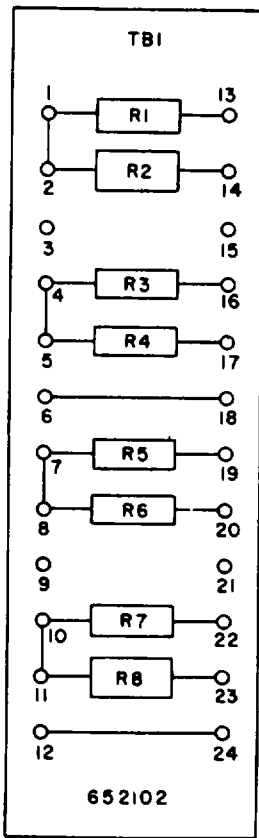
(6) Repeat step (5) for each wired connector contact until transfer of all connector contacts is completed.

(7) Mount and secure the bottom access plate to power supply chassis assembly 2A1A6 using the ten screws removed in step (1).

g. *Replacement of Power Supply 2A1* (fig. 3-17).

(1) Insert 15/28v voltage regulator 2AIA1 into replacement power supply chassis assembly 2A1A5 aligning printed wiring board with guide rails located on upper and lower portions of power supply chassis assembly 2A1A5. Then slowly push the plug-in component into power supply chassis assembly 2A1A6 until the connector are mated.

(2) Tighten the two captive screws on 15/ 28v voltage regulator 2A1A1 securing the plug



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NOTE  
PREFIX ALL REFERENCE  
DESIGNATIONS WITH 2AIA5

Figure 3-23. Terminal board 2A1A5TB1, top view, parts location.

(2) Insert voltage regulator used with replaced connector into power supply chassis assembly 2ALAS and seat its connector into replacement connector. Secure the regulator with its two captive screws.

(3) Tighten the two screws and nuts securing connector to power supply chassis assembly 2A1A6 and then remove the voltage regulator.

(4) Solder wires removed in step b(2) to connector terminals.

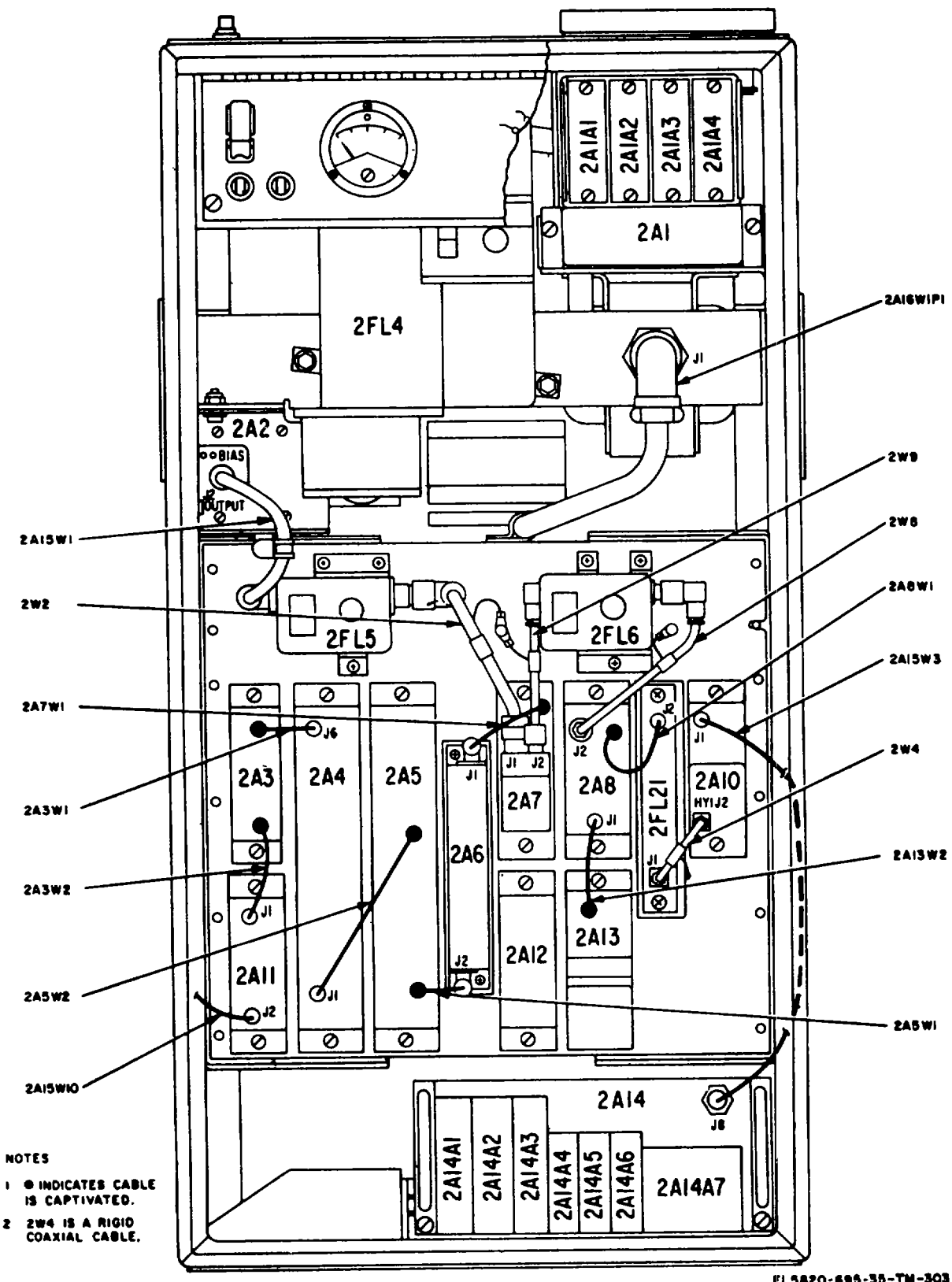
(5) Mount and secure the rear shield to power supply chassis assembly 2A1A5 using the four screws and associated washers removed in step b(1).

d. *Removal of Lamp Socket 2A1A5XDS1 Through 2A1A5XDS4* (fig. 3-22).

(1) Turn power supply chassis assembly 2A1A5 upside down and remove the ten screws securing bottom access plate to power supply chassis assembly 2ALA5.

(2) Tag and unsolder wires connected to lamp socket being removed.

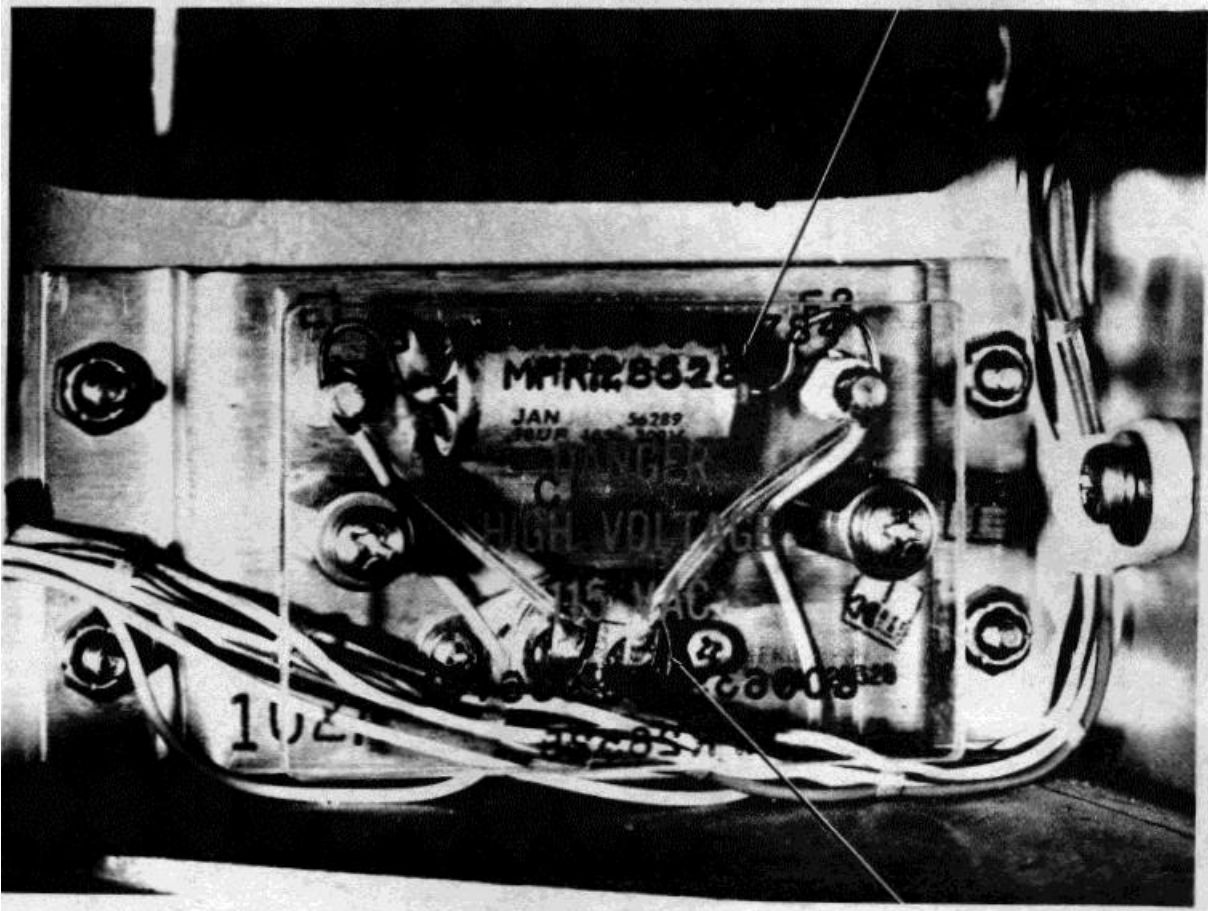
(3) Force press fitted lamp socket through its mounting hole in power supply chassis assembly 2A1A5 by pressing terminal end toward mounting hole and



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Figure 3-24. Receiver, Radio R-1467/GRC-144, cable locations.



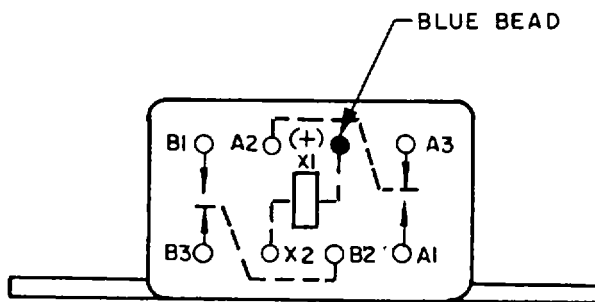


**NOTES:**

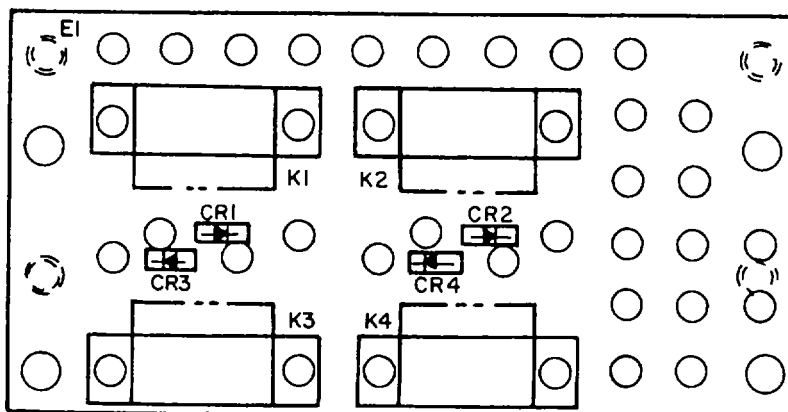
1. THERMOSTATIC SWITCH ASSEMBLIES 1A15A17/2A15A17 ARE USED ON TRANSMITTER, RADIO T-1054(P)/GRC-144(V) AND RECEIVER, RADIO R-1467(P)/GRC-144(V). SEE FIGURE 3-3 FOR LOCATION ON THE T-1054(P)/GRC-144(V) AND FIGURE 3-19 FOR LOCATION ON THE R-1467(P)/GRC-144(V).
2. PARTIAL REFERENCE DESIGNATION ARE SHOWN FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION.

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Figure 3-24.1 Thermostatic Switch Assembly 1A15A17/2A15A17, parts location.



WIRING VIEW OF RELAY



NOTE 1. RELAY BOARD ASSEMBLY 1A15A18 IS USED ON TRANSMITTER,  
 RADIO T-1054(P)A/GRC-144(V)  
 SEE FIGURE 3-7.1 FOR LOCATION ON THE T-1054(P)A/GRC-144(V)

2 PARTIAL REFERENCE DESIGNATION ARE SHOWN FOR COMPLETE  
 DESIGNATIONS, PREFIX WITH UNIT NUMBER AND  
 SUB-ASSEMBLY DESIGNATION

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Figure 3-24.2 Relay Board Assembly 1A15A18, Darts location.

in component to replacement power supply chassis assembly 2A1A5.

(3) Repeat steps (1) and (2) for regulators 2A1A2, 2A1A4, and 2A1A3.

(4) Position and push power supply 2A1 into electrical equipment cabinet 2A15 until guide pins and connectors are mated.

(5) Alternately tighten the two power supply captive screws two turns at a time until power supply 2A1 is securely fastened to electrical equipment cabinet 2A15.

(6) Release meter panel assembly 2A15A2 and position downward until it rests against electrical equipment cabinet 2A15.

(7) Secure meter panel assembly 2A15A2 by tightening the two meter panel captive screws.

(8) Set the POWER ON/OFF switch on meter panel assembly 2A15A2 to ON.

**3-41. Replacement of Vane Axial Fan 2A15B1 (fig. 3-19 and 3-34)**

*a. Removal.*

(1) Remove power from R-1467/GRC-144 (para S-38a).

(2) Remove power supply 2A1 (para 3-40a (2) through (5)).

(3) Loosen the four air filter thumbscrews (fig. 3-20) securing air exhaust filter 2A15MP2 to top of electrical equipment cabinet 2A15 and remove the filter.

(4) While supporting fan 2A15B1 from inside of the cabinet, loosen, but do not remove, the four screws securing the fan to the cabinet. Each screw has a synclamp nut which clamps the fan to the cabinet frame.

(5) Tilt the fan upward to slide it past the synclamps and then lower the fan into the cabinet.

(6) Tag the wires connected to the fan terminals. Remove the three screws that secure the wire lugs to the fan terminals. The lugs are soldered to the tagged wires.

(7) Remove the fan from the cabinet.

*b. Replacement.*

(1) Check that AIR FLOW arrow, printed on side of the replacement fan, is pointing upward, and insert the replacement fan into upper right section of the cabinet. Connect wire lugs to the fan terminals, using the three screws removed in a(6) above.

(2) Position the fan against the top wall of the cabinet between the four synclamps which clamp the fan to the frame of the cabinet.

(3) Secure the fan to the cabinet by tightening the four screws still connected to the four synclamps.

(4) Mount air exhaust filter 2A15MP2 to the top of the cabinet and tighten the four thumbscrews.

(5) Reinstall power supply (para -40g(4) through (7)).

(6) Restore power to R-1467/GRC-144 (para 338b).

**3-42. Replacement of Capacitor 2A15C1 (fig. 3-19)**

*a. Removal.*

(1) Remove power from R-1467/GRC-144 (para 38a).

(2) Remove power supply 2A1 (para 342a(2) through (5)).

(3) Remove the two nuts securing capacitor mounting bracket to rear wall of the cabinet, and remove the capacitor mounting bracket.

(4) Tag and unsolder two wires connected to capacitor 2A15C1 terminals, and remove the capacitor.

*b. Replacement.*

(1) Insert the replacement capacitor into the cabinet and solder the wires removed in a(4) above.

(2) Insert capacitor mounting bracket over the replacement capacitor, and then place the capacitor mounting bracket on the threaded studs on rear wall of the cabinet.

(3) Replace and tighten the two nuts securing the capacitor mounting bracket to rear wall of the cabinet.

(4) Replace power supply 2A1 (para 340 a(4) through (7)).

(5) Restore power to R-1467/GRC-144 (para 3-38b).

**3-43. Replacement of Power Transformer 2A15A4T1 (fig. 3-19)**

*a. Removal.*

(1) Remove power from R-1467/GRC-144 (para 338a).

(2) Loosen the two meter panel captive screws on meter panel assembly 2A15A2 (fig. 3-17)

(3) Position meter panel assembly 2A15A2 upward and lock -it in the upward position by use of the panel locking latch (fig. 3-19).

(4) Disconnect coaxial cable 2A15W1 (fig. 3-24) from the OUTPUT J2 connector on tunnel

diode amplifier 2A2 by rotating the knurled connector on coaxial cable 2A15W1 in a counterclockwise direction.

(5) Loosen the four captive screws (fig. 818) securing tunnel diode amplifier 2A2 to its mounting bracket a few turns each.

(6) Disconnect the knurled connector INPUT J1 on tunnel diode amplifier 2A2 from its mating connector on preselector bandpass filter 2FL4 by rotating the knurled connector clockwise.

(7) Remove the four captive screws securing tunnel diode amplifier 2A2 to its mounting bracket.

(8) Slide tunnel diode amplifier 2A2 back and to the right, then forward being careful not to put stress on the power cable connected to the rear of 2A2.

(9) Disconnect power cable 2A15W2P2 from the POWER J3 connector (locator at the rear of 2A2) by rotating the connector 1/2-turn clockwise (as viewed from front of 2A2) and remove tunnel diode amplifier 2A2 from the cabinet.

(10) Remove eight input waveguide flange screws (fig. 3-20) securing external input waveguide section to waveguide flange on preselector bandpass filter 2FL4.

#### NOTE

**After removing the six screws (step a (11) below); obtain a thin sheet of rigid material about 1/16th inch thick and insert this material between the top of the cabinet and the input waveguide section to support the input waveguide section when preselector bandpass filter 2FL4 is being removed.**

(11) Remove six 2FL4 flange screws (fig. 3-20) securing preselector bandpass filter 2FL4 to the top of electrical equipment cabinet 2A15.

(12) Remove two bolts and washers (fig. 318) securing lower part of preselector bandpass filter 2FL4 to electrical equipment cabinet 2A15 preselector support and remove preselector bandpass filter 2FL4.

(13) Remove 2A16W1P1 from 2A15W2J1 (fig. 318) on electrical equipment cabinet 2A165 preselector support by rotating the knurled connector on 2A16W1P1 counterclockwise.

(14) Remove two nuts, washers and bolts securing tunnel diode amplifier 2A2 mounting bracket to electrical equipment cabinet 2A16 preselector support.

(15) Remove the mounting hex nut

securing connector 2A15W2J1 to preselector support, then remove connector and replace hex nut on connector (fig. 3-19).

(16) Remove two nuts on the left side and two nuts on the right side of preselector support securing preselector support to electrical equipment cabinet 2A15 and remove preselector support.

(17) Remove power supply 2A1 from electrical equipment cabinet 2A15 (para 340(4) and (5)).

(18) Tag, unsolder, and remove the wires connected to power transformer 2A15W4T1 terminals. Care should be taken not to put stress on the cable harness wires.

(19) While supporting power transformer 2A15A4T1, remove the four nuts and washers securing 2A15A4T1 to its mounting bracket and then remove 2A15A4T1 from electrical equipment cabinet 2A15.

#### b. Replacement.

(1) Mount replacement power transformer 2A15A4T1 on its four mounting studs in electrical equipment cabinet 2A15.

(2) While supporting power transformer 2A15A4T1 flush against the transformer mounting bracket, replace and tighten the four nuts and washers securing power transformer 2A15A4T1 in place.

#### CAUTION

**Exercise care while soldering the cable harness leads to the power transformer terminals to prevent damage to the cable harness leads or the power transformer terminals.**

(3) Solder the wires removed in step a(18) to power transformer 2A15A4T1 terminals.

(4) Replace power supply 2A1 (para 340g (4) and (6'5)).

(5) Place preselector support in electrical equipment cabinet 2A15 aligning all mounting holes. Then secure preselector support to electrical equipment cabinet 2A15 using hardware removed in step a(16).

(6) Secure tunnel diode amplifier 2A2 mounting bracket to preselector support using hardware removed in step a(14).

(7) Remove hex-nut from connector 2A15W2J1 and insert through mounting hole on preselector support; then secure connector 2A15W2J1 to mounting bracket with the hex-nut.

(8) Connect 2A16W1P1 to connector 2A15W2J1 on preselector support.

(9) Install preselector bandpass filter 2FL4 in electrical equipment cabinet 2A15, aligning filter mounting holes with mounting holes on preselector support. Then secure preselector bandpass filter 2FL4 to preselector bracket using the two bolts and washers removed in step a(12).

**NOTE**

**After installing preselector bandpass filter 2FL4 remove the thin sheet of rigid material placed on top of cabinet to support the input waveguide section.**

(10) Secure preselector bandpass filter 2FL4 upper flange to top of electrical equipment cabinet 2A15 using the six screws removed in step a (11).

(11) Secure external input waveguide section to preselector bandpass filter 2FL4 using the eight screws removed in step a(10).

(12) Connect the power cable 2A15W2P2 removed in a(9) above to the POWER JS connector (on the rear of the tunnel diode amplifier) by pushing the power cable connector in and rotating it 1/2-turn counterclockwise (as viewed from front of 2A2).

(13) Insert tunnel diode amplifier 2A2 into electrical equipment cabinet 2A15 and rotate tunnel diode amplifier 2A2 in a counterclockwise direction until it can be slid into its mounting bracket.

(14) Tighten the four captive screws on the tunnel diode amplifier mounting bracket until the tunnel diode amplifier 2A2 is loosely held in position by the four captive screws.

(15) Connect and hand tighten the knurled connector INPUT J1 on tunnel diode amplifier 2A2 to its mating connector on preselector bandpass filter 2FL4 by rotating the knurled connector in a counterclockwise direction.

(16) Tighten the four captive screws on the tunnel diode amplifier mounting bracket.

(17) Connect coaxial cable 2A15W1 to the OUTPUT J2 connector on tunnel diode amplifier 2A2.

(18) Release the meter panel assembly 2A15A2 and position it against the cabinet.

(19) Secure meter panel assembly 2A15A2 to electrical equipment cabinet 2A15 with the two meter panel captive screws.

(20) Restore power to R-1467/GRC-144 (para 38b).

### 3-44. Replacement of Preselector Bandpass Filter 2FL4 (fig. 3-17)

*a. Removal.*

(1) Remove power from R-1467/GRC-144 (para 8-88a).

(2) Loosen the two meter panel captive screws on meter panel assembly 2A15A2 (fig. 817).

(3) Position the meter panel assembly upward and lock it in position by using the panel locking latch (fig. 3-19).

(4) Loosen the four captive screws (fig. 818) that secure tunnel diode amplifier 2A2 to its mounting bracket a few turns each.

(5) Disconnect the knurled connector INPUT J1 on tunnel diode amplifier 2A2 from its mating connector on preselector bandpass filter 2FL4 by rotating the knurled connector clockwise.

(6) Remove eight input waveguide flange screws (fig. 3-20) securing external input waveguide section to waveguide flange on preselector bandpass filter 2FL4.

**NOTE**

**After removing the six screws (step a(7) below); obtain a thin sheet of rigid material about 1/16th inch thick and insert this material between the top of the cabinet and the input waveguide section to support the input waveguide section when preselector bandpass filter 2FL4 is being removed.**

(7) Remove six 2FL4 flange screws (fig. 3-20) securing preselector bandpass filter 2FL4 to the top of electrical equipment cabinet 2A15.

(8) Remove two bolts and washers (fig. 818) securing lower part of preselector bandpass filter 2FL4 to electrical equipment cabinet 2A16 preselector support and remove preselector bandpass filter 2FL4.

*b. Replacement.*

(1) Install preselector bandpass filter 2FL4 in electrical equipment cabinet 2A15 aligning filter mounting holes with mounting holes on preselector support. Then secure preselector bandpass filter 2FL4 to preselector bracket using the two bolts and washers removed in step a(8).

**NOTE**

**After installing preselector bandpass filter 2FL4 remove the thin sheet of rigid material placed on top of cabinet to support the input waveguide section.**

(2) Secure preselector bandpass filter 2FL4 upper flange to top of electrical equipment cabinet 2A15 using the six screws removed in step (7).

(3) Secure external input waveguide section to preselector bandpass filter 2FL4 using the eight screws removed-in step a(6).

(4) Connect and hand tighten the knurled connector INPUT J1 on tunnel diode amplifier 2A2 to its mating connector on preselector bandpass filter 2FL4 by rotating the knurled connector in a counterclockwise direction (as viewed from front of 2A2).

(5) Tighten the four captive screws on tunnel diode amplifier mounting bracket.

(6) Release the meter panel assembly 2A15A2 and position it downward against electrical equipment cabinet 2A16.

(7) Secure meter panel assembly 2A15A2 with the two meter panel captive screws.

(8) Restore power to R-1467/GRC-144 (para 88b).

(9) Perform the R-1467/GRC-144 local oscillator metering circuits calibration procedure (para - 65).

### 3-45. Replacement of Post Selector Bandpass Filter 2FL5 (fig. 8-17)

#### a. Removal

(1) Set the POWER ON/OFF switch on meter panel assembly 2A15A2 to OFF.

(2) Disconnect coaxial cable 2W2 (fig. S24) from connector 2FL6J1.

(3) Disconnect coaxial cable 2A15W1 from connector 2FL6J2.

(4) Remove the three screws (fig. 8-18) and flat washers that secure post selector bandpass filter 2FL5 to plate assembly 2A16. Carefully withdraw 2FL5 from the Cabinet.

#### b. Replacement.

(1) Install replacement post selector bandpass filter 2FL6 in electrical equipment cabinet 2A165, aligning the three filter mounting holes with the mounting holes on plate assembly 2A16. Secure 2FL5 to the plate assembly using the three screws and flat washers removed in a(4) above.

(2) Connect coaxial cable 2A15W1 to connector 2FL5J2.

(3) Connect coaxial cable 2W2 to connector 2FL6J1.

(4) Set the POWER ON/OFF switch on meter panel assembly 2A15A2 to ON.

(5) Perform the R-1467/GRC-144 local

oscillator metering circuits calibration procedure (para 3-65)

### 3-46. Replacement of Local Oscillator Bandpass Filter 2FL6 (fig. 3-17)

#### a. Removal.

(1) Set the POWER ON/OFF switch on meter panel assembly 2A15A2 to OFF.

(2) Disconnect coaxial cable 2W9 (fig. 824) from connector 2FL6J1.

(3) Disconnect coaxial cable 2W8 from connector 2FL6J2.

(4) Remove the three screws (fig. 8-18) and flat washers that secure local oscillator bandpass filter 2FL6 to plate assembly 2A16. Care fully withdraw 2FL6 from the cabinet.

#### b. Replacement.

(1) Install replacement local oscillator bandpass filter 2FL6 in electrical equipment cabinet 2A15, aligning the three filter mounting holes with the mounting holes on plate assembly 2A16. Secure 2FL6 to the plate assembly using the three screws and washers removed in step a(4) above.

(2) Connect coaxial cable 2W9 to connector 2FL6J1.

(3) Connect coaxial cable 2W8 to connector 2FL6J2.

(4) Set the POWER ON/OFF switch on meter panel assembly 2A15A2 to ON.

(5) Perform the R-1467/GRC-144 local oscillator metering circuits calibration -procedure (para 8-65).

### 3-47. Replacement of Low Pass Filter 2A15A6FL1 (fig. 8-19)

#### a. Removal.

(1) Remove power from R-1467/GRC-144 (para 888a).

(2) Perform steps (2) through (8) of paragraph 8-44a.

(3) Tag, unsolder, and remove the wires connected to the bottom terminals of low pass filter 2A15A6FL1 (fig. 8-19).

(4) Remove the six screws and washers securing the filter to low pass filter assembly 2A15A6. Then lower the filter from the filter assembly exposing the filter upper terminals.

(6) Tag, unsolder, and remove the wires connected to the upper terminals of the filter and remove the filter from the cabinet.

*b. Replacement.*

(1) Position replacement low pass filter 2A15A6FL1 close to low pass filter assembly 2A15A6 and solder the wires removed in step d(6) to the upper terminals of the filter.

(2) Carefully insert the filter into filter assembly and secure in place using the six screws and washers removed in step a(4).

(3) Solder the wires removed in step a(3) to their respective bottom terminals on the filter.

(4) Perform steps (1) through (8) of paragraph 3-44b.

**3-48. Replacement of Input Filter 2A15A5FL2 or 2A15A5FL3 (fig. 3-19)**

**WARNING**

**115 vac is applied to input filters 2A15A5FL2 and 2A15A5FL3. Be sure that the external ac. power cable is disconnected from 2A15A5J5 (fig. 3-20) before performing this procedure.**

(1) Remove power from R-1467(P)/GRC144(V) or R-1467(P)/A/GRC-144(V) (para 3-38a).

(2) Perform steps (2) through (8) of paragraph 3-44a.

(3) Remove the four screws securing filter clamp in place (fig. 3-35) and remove the filter clamp.

(4) Remove the four screws and washers on top of electrical equipment cabinet 2A15 releasing filter assembly 2A15A5 from electrical equipment cabinet 2A16.

(5) From inside the cabinet, tag, unsolder, and remove the wire connected to ground lug EI on right side of the filter assembly.

(6) Tag, unsolder, and remove the leads connected to bottom terminals of the filters.

(7) Carefully remove the filter assembly from the cabinet 2A15.

(8) Remove four screws securing the filter assembly cover to the filter assembly box. Carefully ease cover off box providing access to the top terminals of the filters. Unsolder and remove lead from the filter being removed.

(9) For the filter being replaced, remove the hex-nut securing the filter to the cover and then remove the filter.

*b. Replacement.*

(1) Remove the hex-nut from the replacement filter, and use the hex-nut to secure the

replacement filter to the filter assembly cover.

(2) Place the filter cover close to the filter assembly box and solder the wire lead removed in step a(8) to the filter top terminal.

(3) Place the filter cover on the filter box, checking that the leads from the filters are not crimped. Secure the filter cover to the filter box by replacing and tightening the four screws removed in step M(8).

(4) Position the filter assembly in the cabinet so that ground lug EI is on the right side of the filter assembly. Solder the leads removed in step a(6) to each input filter terminal.

(5) Solder the lead removed in step a(6) to ground lug EI on right side of the filter assembly.

(6) Position and lift the filter assembly, aligning the mounting holes with the cabinet mounting holes. Secure the filter assembly to the cabinet using the four screws and washers removed in a(4) above.

(7) Replace the filter clamp and secure in place using the four screws removed in step a(3).

(8) Perform steps (1) through (8) of paragraph 3-44b.

**3-49. Replacement of Electrical Equipment Chassis 2A14A10 (fig. 3-17)**

*a. Removal.*

(1) Set the POWER ON/OFF switch on meter panel assembly 2A15A2 to OFF.

(2) Disconnect coaxial cable 2A15W3 from electrical equipment chassis 2A14A10 front panel connector OUTPUT J8 (fig. 3-24).

(3) Loosen the two 2A14 captive screws (fig. 3-17) by alternately turning each captive screw two turns at a time until the captive screws rotate freely. Withdraw electrical frequency synthesizer 2A14 from electrical equipment cabinet 2A15.

(4) Loosen and remove the two screws securing the left side handle assembly to electrical equipment chassis 2A14A10.

(5) Remove plug-in components 2A14A1 through 2A14A8 from electrical frequency synthesizer 2A14 (TM 11-820-695-12).

*b. Replacement.*

(1) Insert plug-in components 2A14A1 through 2A14A8 into replacement electrical equipment chassis (TM 11-5820-695-12).

(2) Install the left side handle assembly on replacement electrical equipment chassis 2A14A10 and secure in place using the two screws removed in step a(4).

(3) Slide replacement electrical frequency synthesizer 2A14 into the cabinet, aligning the mounting guide pins with the mounting holes in the cabinet. Carefully push electrical frequency synthesizer 2A14 into the cabinet until connectors are mated.

(4) Alternately tighten the two 2A14 captive screws securing the synthesizer to the cabinet.

(5) Reconnect coaxial cable 2A15W3 to electrical frequency synthesizer 2A14 front panel connector OUTPUT J8.

(6) Set the POWER ON/OFF switch on meter panel assembly 2A15A2 to ON.

**3-50. Removal of Plate Assembly 2A16(fig. 3-17)**

*a. Removal/.*

(1) Remove power from R-1467(P)/GRC144(V) or R-1467(P)A/GRC-144(V) (para 3-38a)

(2) Disconnect the following coaxial cables (fig. 324): 2A16W1 from postselector bandpass filter 2FL5 connector J2. 2A15W3 from electrical frequency synthesizer 2A14 connector output J8 end amplifier-frequency multiplier 2A10 connector J1, and 2A15W10 from af-rf amplifier 2A11 connector J2.

(3) Disconnect plug 2A16W1P1 (fig. 3-18) from connector 2A15W2J1.

(4) Remove the ten screws (fig. 3-18) securing plate assembly 2A16 to electrical equipment cabinet 2A15.

(5) Carefully withdraw plate assembly 2A16 from electrical equipment cabinet 2A15.

*b. Reassembly.*

(1) Mount plate assembly 2A16 to its mounting rails in electrical equipment cabinet 2A15.

(2) Replace and tighten the ten screws removed in step a(3).

(3) Connect plug 2A16W1P1 to connector 2A15W2J1.

(4) Connect the following coaxial cables: 2A15W1 to postselector bandpass filter 2FL6 connector J1, 2A15W3 to electrical frequency synthesizer 2A14 connector output J8 and amplifier frequency multiplier 2A10 connector J2, and 2A15W10 to af-rf amplifier 2A11 connector J2.

(5) Restore power to R-1467(P)/GRC144(V) or R-1467(P)A/GRC-144(V) (para 3-38b).

**3-51. Replacement of Parts on or behind Plate Assembly 2A16 (fig. 3-21)**

Plate Assembly 2A16 must be removed from electrical equipment cabinet 2A15 (para 3-50a) to gain access to any of the parts mounted on the rear of plate assembly 2A16 (fig. 3-21). All of the parts mounted on the rear of plate assembly 2A16 can be replaced using general parts replacement techniques (para 3-19).

**3-52. Repair and Replacement of R-1467(P)/ GRC-144(V) and R-1467(P)A/GRC-144(V)**

*a. General.* Repair of connectors in R-1467(P)/GRC-144(V) or R-1467(P)A/GRC144(V) requires either the replacement of the defective connector (solder type nonremovable contacts) or the replacement of defective connector contacts (crimp or solder type removable contacts). A listing of the R-1467(P)/GRC-144(V) and R-1467 (P)A/GRC-144(V) connectors is included in the chart below. The chart also includes a listing of applicable tools (fig. 3-26), a paragraph reference specifying the applicable repair procedure, and a figure reference for identification of the connector.

*b. R-1467(P)/GRC-144(V) and R-1467(P) A/GRC-144(V) Connector Chart*

<i>Connector</i>	<i>Extraction/ insertion tool</i>	<i>Crimping tool</i>	<i>Procedure paragraph</i>	<i>Figure reference</i>
2A1A5P1 .....	MS 18278 size 20/none.....	MS 3191-4 with Head.....	3-37c.....	3-9
2A15W2XA1.....	Same.....	Same.....	3-37c.....	3-18
2A16W1XA5.....	Same.....	Same.....	3-37c.....	3-18
2A16W1XA8.....	Same.....	Same.....	3-37c.....	3-18
2A16W1XA11.....	Same.....	Same.....	3-37c.....	3-18
2A16W1XA12B.....	Same.....	Same.....	3-37c.....	3-18
2A16W1XA13.....	Same.....	Same.....	3-37c.....	3-18
2A6XA4.....	Same.....	Same.....	3-37c.....	3-18
2A16XA7.....	Same.....	Same.....	3-37c.....	3-18
2A16XA10.....	Same.....	Same.....	3-37c.....	3-18
2A15W2XA14.....	CET-C6B/None.....	None.....	3-37d.....	3-18
2A16W1XA12A.....	CET-C6B/None.....	None.....	3-37d.....	3-18
2A15W2J1.....	MS 24256 R20/A20.....	MS3191-4 with Head.....	3-37e	

Assy W1



<b>Connector</b>	<b>Extraction/ insertion tool</b>	<b>Crimping tool</b>	<b>Procedure paragraph</b>	<b>Figure reference</b>
2A16W1P1.....	Same.....	Same.....	3-37e.....	3-18
2A1A5XA1 through 2A1A5XA4.....	None required.....	None required.....	3-37f.....	3-22
2A15A5J5.....	None required.....	None required.....	3-37f.....	3-20
2A15A6J2.....	None required.....	None required.....	3-37f.....	3-20
2A15A6J3.....	None required.....	None required.....	3-37f.....	3-20
2A15A6P2.....	None required.....	None required.....	3-37f.....	3-19

**3-53. Indicator, Antenna Alignment ID-1708/GRC Repairs (fig. 3-25)**

With the exception of meter 3M,1, all parts contained within the Indicator, Antenna Alignment ID-1708/GRC are removed using the general parts replacement techniques described in paragraph 3-19.

*a. Removal of meter 3M1.*

- (1) Remove the 12 screws securing the meter panel to the chassis inclosure.
- (2) Lift and rotate meter panel over on its wiring side.
- (3) Remove the self-locking nuts and washers from the meter terminals.
- (4) Tag and remove the wire lugs connected to the meter terminals.
- (5) Loosen the three lock nuts and screws that secure meter 3M41 to the meter panel.
- (6) Lift the meter panel and remove the three locknuts, washers, and screws holding meter 3M1 to the meter panel, then lift and remove meter 3M1.

*b. Replacement of 3M1.*

- (1) Install new meter 3M1 in position on front portion of the meter panel.
- (2) Align meter mounting holes with meter panel mounting holes and place the three screws removed in step a(6) through the aligned holes.
- (3) Secure the meter 3M1 to the meter panel using the three washers and locknuts removed in step a(7).
- (4) Remove the two self-locking nuts and washers from the meter terminals, then remove the shorting bar from the meter terminals.
- (5) Connect the wire lugs removed in a(4) above, to their respective meter terminals and fasten lugs to meter terminals with hardware removed in step a(3).
- (6) Place the shorting bar removed from new meter across the terminals of the damaged meter and secure in place.
- (7) Mount meter panel on the chassis inclosure and secure by replacing and tightening the 12 screws removed in step a(1).
- (8) Calibrate meter 3M1 (para 3-67).

**3-54 Removal and Replacement of Air Filters.**

The removal and replacement of the three air filters in equipment R-1467/GRC-144 is identical to the procedure described in paragraph 3-20.1.

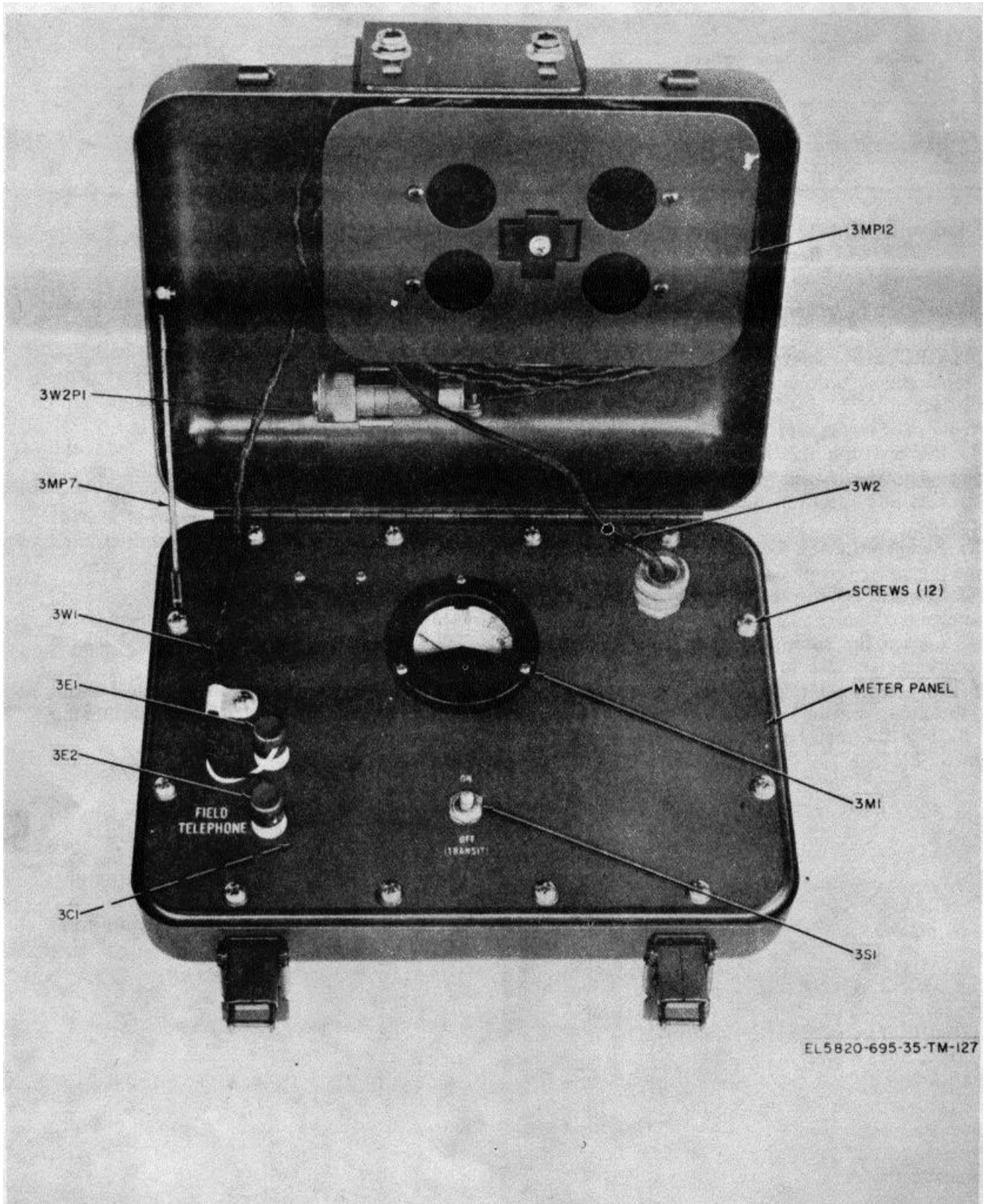


Figure 3-25. Indicator, Antenna Alignment ID-1708, Parts Location.

**3-53.1. Special Tools List and Fabrication**

- a. Tool. Allen wrench (special).
- b. Fabrication. Cut 7/64 Allen wrench to the prescribed dimensions given in figure 3-24.3.

**3-53.2 Converter-Multiplier Assembly CV-3633/GRC-144(V)**

Procedures required to remove or replace parts which are not obvious or require special handling are given in paragraphs 3-53.3 through 3-53.6. Prior to removal or replacement of any part in the CV-3633/ GRC-144(V), the procedures for power removal given in paragraph 3-53.2a, unless otherwise stated, must be performed. Procedures for restoring power are given in b below.

a. Remove Power.

(1) Place switches, waveguide to the TO LOAD (TEST), 5 GHz TEST (TO LOAD) or 15 GHz TEST (TO LOAD) positions.

(2) On the T-1054(P)A/GRC-144(V) set the POWER ON-OFF switch on meter panel assembly 1A15A8 to OFF.

(3) Set Converter-Multiplier CV-3633/GRC-144(V), status panel 3A8 POWER ON-OFF switch 3A8S1 to OFF.

(4) On the R-1467(P)A/GRC-144(V) set the POWER ON-OFF switch on meter panel assembly 2A15A2 to OFF.

(5) Disconnect the external ac power source cable from connector 3A7J1 AC POWER located on the left section of the electrical equipment chassis 3A7, when viewed from front.

b. Restore Power.

(1) Reconnect the external ac power source cable to AC POWER connector 3A7J1.

(2) Restore power to Transmitter, Radio T-1054(P)A/GRC-144(V) in accordance with the procedures in paragraph 3-20b.

(3) Restore power to the receiver, radio in accordance with the procedures given in paragraph 3-38b.

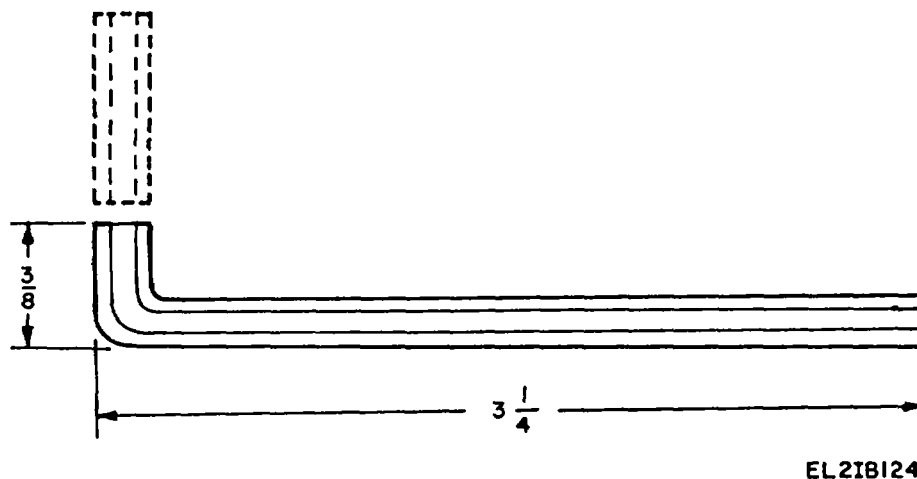


Figure 3-24.3. Fabricated allen wrench dimensions.

(4) Set the status panel 3A8 POWER ON/OFF switch 3A8S1 to ON.

(5) Make the following checks on the CV-3633/GRC-144(V).

(a) The 2 AMP and 1.5 AMP neon indicators on status panel 3A8 (fig. 3-9.2) are not lighted.

(b) Press the PRESS TO TEST OSC TEMP pushbutton switch 3A8DS1 to check that the lamp operates. The OSC TEMP indicator should illuminate within 30 minutes after turning equipment on.

**NOTE**

**Radio communications can normally be established 5 to 10 minutes after the AN/GRC-144(V)4 has been turned on if the ambient temperature in the shelter is maintained above +70 degrees Fahrenheit.**

**3-53.3. Replacement of Reflected Power Detector 3A7CR1 (fig. 5-108)**

**a. Removal.**

(1) Set the POWER ON/OFF switch on the status panel 3A8 to OFF.

(2) Remove alarm monitor 3A1 and converter frequency electronics 3A2.

(3) Carefully remove SMA connector from left end of detector.

(4) Loosen hex nut that secures detector 3A7CR1 to electrical equipment chassis 3A7 plastic loop clamp.

(5) Carefully remove SMA connector from right end of detector, then remove detector.

**b. Replacement.**

(1) Replace new detector loosely in position in plastic loop clamp and connect SMA connector to right end.

(2) Tighten key nut to secure detector in plastic loop clamp, but do not over tighten.

(3) Connect SMA connector to left end of detector.

(4) Replace alarm monitor 3A1 and converter frequency electronics 3A2.

(5) Set the T-1054(P)A/GRC-144(V) and R-1467(P)A/GRC-144(V) POWER ON/OFF switches to OFF.

(6) Set the POWER ON/OFF switch on the status panel 3A8 to ON.

(7) Perform the CV-3633/GRC-144(V) reflected power alarm threshold test and calibration procedure (para 3-77).

**3-53.4. Replacement of Directional Coupler 3A7DC1 (fig. 5-108)**

**a. Removal.**

(1) Set the T-1054(P)A/GRC-144(V) and R-1467(P)A/GRC-144(V) POWER ON/OFF switches to OFF.

(2) Set the POWER ON/OFF switch on the status panel 3A8 to OFF.

(3) Remove the CV-3633/GRC-144(V) from the R-1467(P)A/GRC-144(V) cabinet.

(4) Remove screws that secure top cover of electrical equipment chassis 3A7 (fig. 5-108, top view with cover removed).

(5) Loosen SMA connector at right end of detector 3A7CR1, then carefully remove SMA connector from directional coupler 3A7DC1.

(6) Remove eight hex socket head screws, flat washers and lockwashers that secure directional coupler 3A7DC1 to waveguide assembly W3 and W4. Remove directional coupler 3A7DC1, and two gasket "O" rings.

**b. Replacement.**

(1) Replace directional coupler 3A7DC1, two gasket "O" rings, and secure with eight hex socket head screws, flat washers, and lockwashers.

(2) Carefully connect SMA connector to directional coupler 3A7DC1, and tighten left end. Tighten SMA connector at right end of detector.

(3) Secure top cover to electrical equipment chassis 3A7.

(4) Replace the CV-3633/GRC-144(V) on the R-1467(P)A/GRC-144(V) cabinet.

(5) Set the T-1054(P)A/GRC-144(V) and R-1467(P)A/GRC-144(V) POWER ON/OFF switches to ON.

(6) Set the POWER ON/OFF switch on the status panel 3A8 to ON.

(7) Perform the AN/GRC-144(V)4 output power test (para 3-76) and reflected power alarm threshold test and calibration procedure (para 3-79).

**3-53.5. Replacement of Bandpass filters 3A3 and 3A4 (fig. 5-108)**

**a. Removal.**

(1) Set the T-1054(P)A/GRC-144(V) and R-1467(P)A/GRC-144(V) POWER ON/OFF switches to OFF.

(2) Set the POWER ON/OFF switch on the status panel 3A8 to OFF.

(3) Remove the CV-3633/GRC-144(V)

from the R-1467(P)A/GRC-144(V) cabinet.

**NOTE**

**If BP filter 3A3 requires replacement remove converter frequency electronics 3A2 and alarm monitor 3A1. If BP filter 3A4 requires replacement remove amplifier-multiplier 3A5 and power supply 3A6.**

(4) Remove screws that secure top corner of electrical equipment chassis 3A7 (fig. 5-108, top view with cover removed).

(5) Use the fabricated Allen wrench and loosen two screws that secure BP filter 3A3 input waveguide flange to waveguide twist W2.

(6) To remove BP filter 3A4, use fabricated Allen wrench and loosen two screws that secure BP filter 3A4 output waveguide flange to waveguide twist W6.

(7) Remove screws lockwashers and flat washers from rear of BP filter 3A3 or 3A4.

(8) Loosen front mounting screws of BP filter 3A3 or 3A4 and remove filter, and gasket "O" ring.

**b. Replacement.**

**NOTE**

**Check that BP filter guide pins mate with respective holes in waveguide twist. If guide pins do not mate properly, remove guide pins from BP filter and replace them in their proper mating hole.**

(1) Replace BP filter 3A3 or 3A4 into their respective slots and align rear waveguide flanges with waveguide twists W2 or W6 respectively.

(2) Secure BP filter in place with front mounting screws.

(3) Handtighten BP filter and waveguide twist together with two hex socket head screws, lockwashers, and flat washers.

(4) Tighten but do not overtighten BP filter and waveguide twist together.

(5) Secure top cover to electrical equipment chassis 3A7.

(6) Replace alarm monitor 3A1 and converter frequency electronics 3A2 or amplifier-multiplier 3A5 and power supply 3A6.

(7) Replace the CV-3633/GRC-144(V) or the R-1467(P)A/GRC-144(V) cabinet.

(8) Set the T-1054(P)A/GRC-144(V) and R-1467(P)A/GRC-144(V) POWER ON/OFF switches to ON.

(9) Set the POWER ON/OFF switch on the status panel 3A8 to ON.

**NOTE**

**If BP filter was replaced perform the CV-3633/GRC144(V) receive section conversion loss test. If BP filter 3A4 was replaced perform the AN/GRC144(V) output power test.**

(10) Perform the CV-3633/GRC-144(V) receive section conversion loss test (para 3-79) or AN/GRC-144(V)4 output power test (para 3-76).

**3-53.6. Replacement of Diplexer Circulator 3A7HY1 (fig. 5-108)**

a. Removal.

(1) Set the T-1054(P)A/GRC-144(V) 3rd R-1467(P)A/GRC-144(V) POWER ON/OFF switches to OFF.

(2) Set the POWER ON/OFF switch on the status panel 3A8 to OFF.

(3) Remove the CV-3633/GRC-144(V) from the R-1467(P)A/GRC-144(V) cabinet.

(4) Remove screws that secure top cover of electrical equipment chassis 3A7 (fig. 5-108, top view with cover removed).

(5) Remove alarm monitor 3A1, converter frequency electronics 3A2, amplifier-multiplier 3A5, power supply 3A6, and BP filters 3A3 and 3A4.

(6) Remove waveguide assembly W3 support nuts and screws.

(7) Remove four hex socket head screws, flat washers, and lockwashers that secure waveguide assembly W3 to directional coupler 3A7DC1.

(8) Remove four hex socket head screws, flat washers and lockwashers that secure other end of waveguide assembly W3 to diplexer circulator 3A7HY1 and remove waveguide assembly W3 and gasket "O" rings.

(9) Remove diplexer circulator 3A7HY1 from LH and RH diplexer supports and remove waveguide twist W2 and W6 and gasket "O" rings from diplexer circulator.

b. Replacement.

(1) Secure waveguide twist W2 and W6 and gasket "O" rings to diplexer circulator 3A7HY1 with eight screws, flat washers and lockwashers.

(2) Replace diplexer circulator 3A7HY1 on LH and RH diplexer supports.

(3) Secure waveguide assembly W3 and gasket "O" ring to diplexer circulator 3A7HY1 with four screws, flat washers and lockwashers.

(4) Secure other end of waveguide assembly W3 and gasket "O" ring to directional coupler 3A7DC1 with four hex head socket screws, flat washers and lockwashers and replace assembly support screws and nuts.

(5) Replace BP filters 3A4 and 3A5, with gasket "O" rings into their respective slots and align input or output waveguide flanges with waveguide twist W2 and W6.

(6) Handtighten BP filters and waveguide twists together with four screws, flat washers, and lockwashers.

(7) Tighten but do not overtighten BP filters and waveguide twists together.

(8) Replace BP filters 3A3 and 3A4.

(9) Replace alarm monitor 3A1 converter frequency electronics 3A2, amplifier-multiplier 3A5, and power supply 3A6.

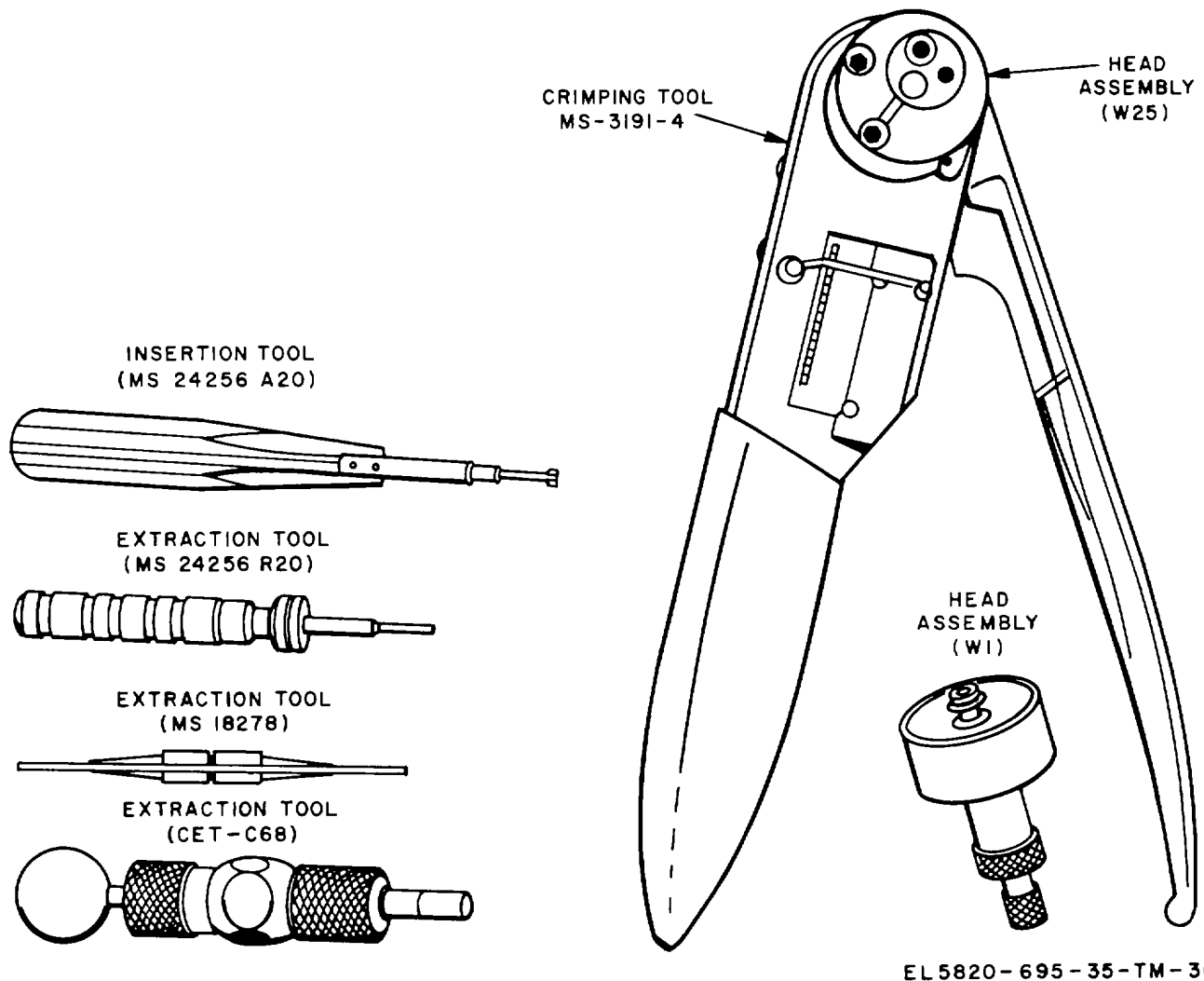
(10) Secure top cover to electrical equipment chassis 3A7.

(11) Replace the CV-3633/GRC-144(V) on the R-1467(P)A/GRC-144(V) cabinet.

(12) Set the T-1054(P)A/GRC-144(V) and R-1467(P)A/GRC-144(V) POWER ON/OFF switches to ON.

(13) Set the POWER ON/OFF switch or the status panel 3A8 to ON.

(14) Perform the CV-3633/GRC-144 receive section conversion loss test (para 3-79) and AN/GRC-144(V)4 output power test (para 3-76).



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Figure 3-26. AN/GRC-144 connector repair tools.

**Section IV. CALIBRATION AND ADJUSTMENT**

**3-54. General**

a. This section contains procedures for calibrating and adjusting the T-1054 (P)/GRC -144(V), T -1054 (P)A/GRC -144 V, R-1467(P)/GRC-144(V), and R-1467(P)A/ GRC-144(V). The calibration procedures are performed at periodic maintenance intervals (para 3-3) to maintain calibration accuracy of the transmitters and receivers metering circuits, or when troubleshooting indicates that calibration is required. The adjustment procedures are performed when troubleshooting indicates that an adjustment is required.

b. All of the procedures contained in this section assume that the AN/GRC144(V) is turned on and connected for normal operation at the start of each procedure. If trouble is encountered during performance of a procedure, or if the indications specified in the

procedure are not obtained, refer to the troubleshooting charts (para 3-) for corrective action.

**3-55. Calibration of Transmitter Meter 1A15A8M1**

- a. Set POWER ON/OFF switch 1A15A8S3 on meter panel assembly 1A15A8 (fig. 3-1) to OFF.
- b. Turn meter selector switch 1A15A8S4 on meter panel assembly 1A15A8 to OFF (TRANSIT).
- c. Using a screwdriver, adjust the screw on the front of meter 1A15A8M1 for a zero meter indication.
- d. Turn meter selector switch 1A15A8S4 on meter panel assembly 1A15A8 to TEST LEAD (+).



e. Turn Test Set, Electrical Meter TS-656/U on and allow a 5-minute warmup period.

f. On the TS-656/U, set the FUNCTION switch to DIR CUR, the CURRENT switch to 100 MICRO-AMP, and turn the DECREASE/ INCREASE control counterclockwise until mechanical stop is reached.

g. Connect the red test lead supplied with TS656/U between the DIR CUR terminal on TS656/U and the TEST LEAD jack on meter panel assembly 1A15A8.

h. Connect the black test lead supplied with TS-656/U between the COMMON terminal on TS-656/U and the EI CABINET GROUND lug on top of electrical equipment cabinet 1A15 (fig. 3-7).

i. On TS-656/U, hold the TEST switch in TEST (up) position and turn the DECREASE/ INCREASE control in INCREASE direction (clockwise) until meter 1A15A8M1 indicates 150.

j. With the TEST switch on TS-656/U in the up position, the meter on TS-656/U should indicate  $37.5 \pm 1.5$  microamperes. If it does not, replace meter 1A15A8M1 (para 321a) and repeat the calibration procedure.

k. Turn the TS-656/U off and disconnect the test leads.

l. Set POWER ON/OFF switch 1A15A8S3 on meter panel assembly 1A15A8 to ON.

### 3-56. Calibration of Transmitter Meter 1A16M2

a. Set POWER ON/OFF switch 1A15A8S3 on meter panel assembly 1A15A8 (fig. 3-1) to OFF.

b. Turn meter switch 1A16S5 on the radio test set meter panel to OFF (TRANSIT).

c. Using a screwdriver, adjust the screw on front of meter 1A16M2 (fig. 3-12) for a zero meter indication (a zero meter indication is obtained when the meter pointer rests on the thin black line located to the left of the yellow meter band).

d. Disconnect cables 1A2W1 and 1A2W2 and remove 100 MHz oscillator 1A2.

e. Set radio test set switch 1A16S5 to the OSC LEVEL position.

f. Turn Test Set, Electrical Meter TS-66/U on and allow a 5-minute warmup period.

g. On the TS--656/U, set the FUNCTION switch to DIR CUR, the CURRENT switch to 100 MICRO-AMP, and turn the DECREASE/ INCREASE control counterclockwise until mechanical stop is reached.

h. Connect a test lead between the DIR CUR terminal on TS-656/U and pin 5 of 100 MHz oscillator

connector 1A16W25XA2 (fig. 3-2 and 5-15(1)).

i. Connect a test lead between the COMMON terminal on T-6/U and pin 9 of 100 MHz oscillator connector 1A16W25XA2.

j. On TS-656/U, hold the TEST switch in TEST (up) position and turn the DECREASE/ INCREASE control in INCREASE direction (clockwise) until indication on meter 1A16M2 reaches SET OSC LEVEL ADJ.

k. With the TEST switch on TS-656/U in the up position, the meter on TS-656/U should indicate 40 +2.0 microamperes. If it does not, replace meter 1A16M2 (para 3-35) and repeat the calibration procedure.

l. Turn the TS-656/U off and disconnect the test leads.

m. Reinstall component 1A2 and connect cables 1A2W1 and 1A2W2.

n. Turn meter switch 1A16S5 on the radio test set meter panel to OFF (TRANSIT).

o. Set the POWER ON/OFF switch 1A15A8S3 on meter panel assembly 1A15A8 to ON.

### 3-57. Calibration of T-1054(P)/GRC-I44(V) Reflected RF Power Metering Circuit

a. Turn on Test Set, Radio Frequency Power AN/USM-161 and allow a 30-minute warmup period.

b. Calculate the calibration plate correction factors of the CN-845/USM-161 and CG-2514/U (fig. 3-29) for a 4800 MHz input. Algebraically add the correction factors noting the plus or minus sign.

c. Calibrate the AN/: USM-16,1 using the procedure given in TM 11 49812.

d. On the AN/USM-161, set BIAS-READ switch to REAM, turn the POWER RANGE switch to 10 MW +10 DBM, set the COMP ATTENUATOR dial to the value recorded in step b above, and set the POWER indicator dial for a dial scale indication of .75 on the outermost scale.

e. Set Switch, Waveguide SA-1679/GRC to the TO LOAD (TEST) position.

f. Record the T-1054(P)/GRC-144(V) operating frequency and then set the controls on electrical frequency synthesizer 1A14 to 4800.0 MHz.

g. If the RF POWER indicator on meter panel assembly 1A14A8 is not lighted red, adjust the PUSH TO TURN knob on radio frequency bandpass filter 1FL3 until it lights red.

h. Remove Dummy Load, Electrical DA-41/ GRC from Adapter, Waveguide UG-1883/GRC and connect the test equipment in figure 3-29.

i. Adjust the PUSH TO TURN control on radio frequency bandpass filter 1FL3 until a null is obtained on AN/USM-161 NULL INDICATOR meter.

j. Turn the meter selector switch 1A15A8S4 on meter panel assembly 1A15A8 to RF POWER.

k. Remove the protective plate over the potentiometer bracket and adjust potentiometer 1A15A8R6, figure 34. If a meter indication of 60 cannot be obtained, refer to the troubleshooting chart (item No. 69, para 386b) for corrective action upon completion of this procedure.

l. Reset the controls on radio frequency bandpass filter 1FL3 and electrical frequency synthesizer 1A14 to the original operating frequency recorded in step f.

m. Set Switch, Waveguide SA-1679/GRC to the TO ANT. (NORM-AL) position.

n. Connect Dummy Load, Electrical DA-541/ GRC to Adapter, Waveguide UG-1883/GRC.

o. Turn off the AN/USM-161 and disconnect the test equipment.

### **3-58. Calibration of T-1054(P)/GRC-144(V) Reflected RF Power Metering Circuit**

a. Turn on Test Set, Radio Frequency Power AN/USM-161 and allow a 30-minute warmup period.

b. Calculate the calibration plate correction factors of the two CN-845/USM-161's and the CG-2514/U (fig. 3-29) for a 4800 MHz input. Algebraically add the correction factors noting the plus or minus sign and record.

c. Calibrate the AN-/USM-161 using the procedures given in TM 11-6625-498-12.

d. On the AN/USM-161, set the BIAS-READ switch to READ, turn the POWER RANGE switch to 3.0 MW +6 DPM, set the COMP ATTENUATOR dial to the value recorded in step b above, and set the POWER indicator dial for a dial scale indication of 1.6 on the center scale.

e. Set Switch, Waveguide SA-16789/GRC to the TO LOAD (TEST) position.

f. Record the T-1054/GRC-144 operating frequency and then set the controls on electrical frequency synthesizer 1A14 to 4800.0 MHz.

g. If the RF POWER indicator on meter panel assembly 1A15A8 is not lighted red, adjust the PUSH TO TURN knob on radio frequency bandpass filter 1FL3 until it lights red.

h. Remove Dummy Load, Electrical DA-641/ GRC from Adapter, Waveguide UG-1883/GRC and connect the test equipment as shown in figure 3-29.

i. Adjust the PUSH TO TURN control on radio frequency bandpass filter 1FL3 until a null is obtained on AN/USM-161 NULL INDICATOR meter.

j. Set Switch, Waveguide SA-1679/GRC to the TO ANT. (NORMAL) position.

k. Turn the AN/USM-161 off and disconnect cable assembly CG-2514/U from Adapter, Waveguide UG-1883/GRC.

l. Connect the 3 db attenuator and type N short (fig. 3-29) to Adapter, Waveguide UG-1883/GRC.

m. Set Switch, Waveguide SA-1679/GRC to the TO LOAD (TEST) position.

n. Turn meter selector switch 1A15A8S4 on meter panel assembly 1A15A8 to REFL RF POWER.

o. Remove the protective plate over the potentiometer bracket and adjust potentiometer 1A15A8R5 (fig. 3-4) for a 1A15A8M1 meter indication of 20. If a meter indication of 20 cannot be obtained, refer to the troubleshooting chart (item No. 40, para 3-6b) for corrective action upon completion of this procedure.

p. Set the controls on electrical frequency synthesizer 1A14 and radio frequency bandpass filter 1FL3 to the original operating frequency recorded in step f.

q. Set Switch, Waveguide SA-1679/GRC to the TO ANT. (NORMAL) position.

r. Disconnect the 3 db attenuator and type N short from Adapter, Waveguide UG-1883/GRC.

s. Connect Dummy Load, Electrical DA-541/ GRC to Adapter, Waveguide UG-1883/GRC.

### **3-59. Calibration of T-1054(P)/GRC-144(V) and T-1054(P)/GRC-144(V) Frequency Multiplier Metering Circuits.**

#### **NOTE**

**Do not calibrate any of the T-1054(P)/GRC-144(V) frequency multiplier metering circuits when the T-1054(P)/GRC-144(V) output power is less than 150 milliwatts. If the output power level is not known, use the T-1054(P)/GRC-144(V) output power test (para 3-72) to determine it.**

To calibrate any of the T-1054/GRC-144 frequency multiplier metering circuits, turn meter selector switch 1A15A8S4 (fig. 3-4) to the circuit to be calibrated and observe the indication on meter 1A15A8M1. If meter indication is not 100, remove the protective plate over the potentiometer

bracket and adjust the associated potentiometer (listed below) for a 1A15A8M1 meter indication of 100. If a meter indication of 100 cannot be obtained, refer to the troubleshooting chart (para 3-6b, items Nos. 41 through 43) for corrective action.

<i>Circuit to be calibrated</i>	<i>Potentiometer (fig. 3-4)</i>
APL-MULT .....	1A15A8R4
2ND MULT .....	1A15A8R3
3RD MULT (LOCAL OSC).....	1A15A8R2

**3-60. Calibration of T-1054(P)/GRC-144(V) and T-1054(P)/GRC-144(V) Traffic Metering Circuit**

- a. Set POWER ON/OFF switch 1A15A8S3 on meter panel assembly 1A15A8 to OFF.
- b. Remove alarm monitor 1A5 from plate assembly 1A16 (TM 11-5820-695-12).
- c. Turn Test Set, Radio Frequency Power AN/USM-161 on and allow a 6-minute warmup period.
- d. On the TS-656/U, set the FUNCTION switch to 'DIR CUR, turn the CURRENT switch to 100 MICRO-AMP, and turn the DECREASE/ INCREASE control counterclockwise until mechanical stop is reached.
- e. Install the connector adapter (part of MK-1207/GRC) on connector 1A16W25XA5B (fig. 3-2).
- f. Connect red test lead supplied with TS656/U between the DIR OUR terminal on TS656/U and red test jack on the connector adapter.
- g. Connect the black test lead supplied with TS-656/U between the COMMON terminal on TS-656/U and black test jack on the connector adapter.
- h. Turn the meter selector switch 1A15A8S4 on meter panel assembly 1A15A8 to TRAFFIC and remove the protective plate over potentiometer bracket (fig. 3-4).
- i. On TS-656/U, hold the TEST switch in TEST (up) position and turn the DECREASE/ INCREASE control in INCREASE direction (clockwise) until a reading of 50 microamperes is observed on TS-656/U meter.
- j. Adjust potentiometer 1A15A8R7 (fig. 3-4) for a 1A15A8M1 meter indication of 90. If a meter indication of 90 cannot be obtained, refer to the troubleshooting chart (para 3-6b, item No. 38) for corrective action upon completion of this procedure.
- k. Release the TEST switch on TS-656/U.
- l. Turn the TS-656/U off and remove the connector adapter from connector 1A16W25XA5B.
- m. Reinstall alarm monitor 1A5 on plate assembly 1A16 (TM 11-5820-695-12).

n. Set POWER ON/OFF switch 1A15A8S4 on meter panel assembly 1A15A8 to ON.

**3-61. Calibration of T-1054(P)/GRC-144(V) and T-1054(FP)/GRC-144(V) Radio Test Set**

**NOTE**

**Before performing the calibration procedures below, perform the R-1467(P)/ GRC-144(V) if gain and carrier alarm test (para 3-75).**

- a. Turn Test Set, Radio Frequency Power AN/USM-161 and Signal Generator AN/URM-52B and allow a 30-minute warmup period.
- b. After the warmup period, calibrate the AN/USM-161 using the procedures given in TM 116625-498-12 and calibrate the AN/URM-52B at 4700 MHz using the procedures given in TM 11-6625-214-10.
- c. Connect the equipment as shown in figure 3-32.
- d. On the AN/USM-161, set the BIAS-REAR switch to READ, turn the POWER RANGE switch to 3.0 MW +5 DBM, turn the COMP ATTENUATOR dial to 0, and turn the POWER indicator dial for a dial scale indication of 1.0 on the center scale.
- e. Adjust the OUTPUT ATTEN control on the AN/URM-52B for a null on the AN/ USM-161 NULL INDICATOR meter.
- f. Adjust the POWER SET control on the AN/URM-52B for an index indication of 0 dbm on the OUTPUT ATTEN dial.
- g. Turn off the AN/USM-161 and disconnect RF cable CG-92D/U from Adapter, UG-29B/U (fig. 332).
- h. Set the OUTPUT ATTEN control on AN/URM-52B for a dial scale indication of -71 dbm.
- i. Set Switch, Waveguide SA-1679/GRC to the TO) LOAD (TEST) position.
- j. Disconnect the antenna waveguide from the rf entry panel on the external shelter wall.
- k. Disconnect the coaxial cable connected to Coupler, Directional CU-1890/GRC.
- l. Connect the equipment as shown in figure 3-33.
- m. Record the R-1467(P)/GRC-144(V) operating frequency.
- n. On R-1467(P)/GRC-144() set the preselector bandpass filter 2FL4, post selector bandpass filter 2FL5, local oscillator bandpass filter 2FL6, and electrical frequency synthesizer 2A14 controls to 4700 MHz.

o. On R-1467(P)/GRC-144(V) turn the AGC SEL switch on 70 MHz intermediate frequency amplifier 2A5 to TEST and turn meter selector switch 2A15A2S1 on meter panel assembly 2A15A2 to CARRIER (IF).

p. Remove the dust cover from the ATTEN ADJ control on Coupler, Directional CU-1890/ GRC and, using a screwdriver, turn the ATTEN ADJ control clockwise until mechanical stop is reached.

**NOTE**

**If meter 2A15A2M1 is off scale, reduce the POWER SET control on AN/URM-52B for an on scale meter reading. After performing step 'g, increase POWER SET control for a dial scale indication of -71 dbm.**

q. Fine tune the SIGNAL FREQUENCY control on AN/URM-52B for a peak indication on meter 2A15A2M1.

r. Remove the green cap from the IF GAIN control on 70 MHz intermediate frequency amplifier 2A5 and, using the tuning tool, adjust the IF GAIN control until an indication of 150 is observed on 2A15A2M1. If a meter indication of 150 cannot be obtained, replace the following components one at a time until a meter indication of 150 is obtained: 70 MHz intermediate frequency amplifier 2A6, amplifier mixer 2A7, and tunnel diode amplifier 2A2. Replace the green cap over the IF GAIN control on 2A5.

s. Turn off AN/URM-52B and disconnect RF cable CG-92D/U from Coupler, Directional CU-1890/GRC (fig. 3-W).

t. Connect tile coaxial cable removed in step k to Coupler, Directional CU-1890/GRC.

u. Using a screwdriver, turn the ATTEN ADJ control on Coupler, Directional CU-1890/GRC counterclockwise until mechanical stop is reached.

v. Record the T-1054(P)/GRC -144(V) operating frequency.

w. On T-1054(P)/GRC-144(V), set controls on radio frequency bandpass filter 1FL3 and electrical frequency synthesizer 1A14 controls to 4800 MHz.

x. Turn the OUTPUT LEVEL switch on the radio test set to LOW.

y. Set the ON/OFF switch on 100 MHz radio frequency oscillator 1A2 to ON.

z. Set the meter switch on the radio test set to CR1. The *radio* test set meter indication shall be in or to the right of the yellow band.

aa. Set the meter switch on the radio test set to CR2. The radio test set meter indication shall be in or to the right of the yellow band.

ab. Set the meter switch on the radio test set to OSC LEVEL and adjust the LEVEL ADJ control on 100 MHz radio frequency oscillator 1A2 for a set OSC LEVEL ADJ indication on the radio test set meter.

ac. Using a screwdriver, turn the ATTEN ADJ control on Coupler, Directional CU-1890/ GRC in a clockwise direction until meter 2A15A2M1 on meter panel assembly 2A15A2 indicates 150.

ad. Replace the dust cover on Coupler, Directional CU-1890/GRC ATTEN ADJ control.

ae. Set the ON/OFF switch on 100 MHz radio frequency oscillator 1A2 to OFF.

af. Set the AGC SEL switch on 70 MHz intermediate frequency amplifier 2A5 to DIV OFF.

ag. Reconnect the antenna waveguide to the rf entry panel on the external shelter wall.

ah. Reset the controls on T-1054(P)/GRC-144(V) and R-1467(P)/GRC-144(V) to the original operating frequencies.

ai. Set Switch, Waveguide SA-1679/GRC to the TO ANTENNA (NORMAL) position.

**3-62. T-1654(P)/GRC-144V) and T-1054(P)/ GRC-144(V) Modulator Frequency Adjustment**

a. Turn on Counter Electronic, Digital Readout AM/USM-207 and allow a 1-minute warmup period.

b. On the AN/USM-207, set the controls as follows:

- (1) SENSITIVITY switch to PLUG-IN.
- (2) FUNCTION switch to FREQ.
- (3) Time base switch to GATE TIME (SEC<sup>-1</sup>) -10<sup>2</sup>.
- (4) Upper and lower converter attenuator switches to 100V MAX.
- (5) DIRECT-HETERODYNE switch to HETERODYNE.
- (6) Mixing frequency selector switch to 100.
- (7) DISPLAY control to desired display time.

c. Disconnect coaxial cable 1A6W2 from the J1 connector on radio transmitter modulator 1A8.

d. Disconnect coaxial cable 1A8W1 from the A1J1 connector on transmitter frequency mixer stage 1A9.

e. Connect the equipment as shown in view A, figure 3-28. Note that the Tee connector is also connected to A1J1 on 1A9.

f. Observe the LEVEL METER on AN/USM-207. If it reads in the green zone, proceed to step h below. Otherwise, proceed to step g below.

g. Alternately set the upper and lower converter attenuator switches on AN/USM-207 to the left, one position at a time, until LEVEL METER indication is in the green zone.

h. On the front of radio transmitter modulator 1A8, remove the blue caps on switch S1 and capacitor C15. Press switch S1 and hold it depressed while performing step i below.

i. Using the tuning tool, adjust capacitor C15 (clockwise to reduce frequency; counterclockwise to increase frequency) for a 50 MHz +5 kHz digital display on AN/USM-207.

j. Release switch S1. Digital display on AN/USM-207 shall be 50 MHz +20 kHz. If it is not, repeat steps h and i. If repeated attempts to adjust the modulator frequency within 50 MHz +20 kHz fails, refer to the troubleshooting chart (para 3-b, item No. 35) for corrective action.

k. Replace the blue caps removed in step h.

l. Turn off the AN/USM-207 and disconnect the test equipment.

m. Connect coaxial cable 1A6W2 to the J1 connector on radio transmitter modulator 1A8.

n. Connect coaxial cable 1A8W1 to the A1J1 connector on transmitter frequency mixer stage 1A9.

### 3-63. Calibration of Receiver Meter 2A15A2M1

a. Set POWER ON/OFF switch 2A15A2M1 on meter panel assembly 2A15A2 to OFF.

b. Turn meter selector switch 2A15A2S1 on meter panel assembly 2A15A2 to OFF (TRANSIT).

c. Using a screwdriver, adjust the screw on the front of meter 2A15A2M1 for a zero meter indication.

d. Turn meter selector switch 2A15A2S1 on meter panel assembly 2A15A2 to TEST LEAD (+).

e. Turn Test Set, Electrical Meter TS-56/U on and allow a 5-minute warmup period.

f. On the T656/U, set the FUNCTION switch to DIR OUR, the CURRENT switch to 100 MICRO-AMP, and turn the DECREASE/INCREASE control counterclockwise until mechanical stop is reached.

g. Connect the red test lead supplied with TS-66/U between the DIR CUR terminal on T656/U and the TEST LEAD jack on meter panel assembly 2A15A2.

h. Connect the black test lead supplied with TS-656/U between the COMMON terminal on TS-656/U and the E2 CAB GRD lug on top of electrical equipment

cabinet 2A15 (fig. 3-20).

i. On TS-656/U, hold the TEST switch in TEST (up) position and turn the DECREASE/INCREASE control in INCREASE direction (clockwise) until meter 2A15A2M1 indicates 200.

j. With the TEST switch on TS-656/U in the up position, the TS-656/U meter should indicate 60 +e.0 microamperes. If it does not, replace meter 2A15A2M1 (para 3-39) and repeat the calibration procedure.

k. Turn the TS456/U off and disconnect the test leads.

l. Set POWER ON/OFF switch 2A15A2S2 on meter panel assembly 2A15A2 to ON.

### 3-64. Calibration of R-1467(P)/GRC-144 (V) and R-1467(P)/GRC-144(V) Traffic Metering Circuit

a. Set POWER ON/OFF switch 2A15A2S2 on meter panel assembly 2A15A2 to OFF.

b. Remove alarm monitor 2A12 from plate assembly 2A16 (TM 11-5820-695-12).

c. Turn Test Set, Electrical Meter TS-656/U on and allow a 5-minute warmup period.

d. On the TS-656/U, set the FUNCTION switch to DIR CUR, the CURRENT switch to 100 MICRO-AMP, and turn the DECREASE/ INCREASE control fully counterclockwise until mechanical stop is reached.

e. Connect the connector adapter (part of MK-1207/GRC) to connector 2A16WIXA12A (fig. 3-18).

f. Connect the red test lead supplied with TS656/U between the DIR CUR terminal on TS656/U and the red test jack on the connector adapter.

g. Connect the black test lead supplied with TS-656/U between the COMMON terminal on TS-656/U and the black test jack on the connector adapter.

h. Turn meter selector switch 2A15A2S1 on meter panel assembly 2A15A2 to TRAFFIC.

i. On TS-656/U, hold the TEST switch in TEST (up) position and turn the DECREASE/INCREASE control in INCREASE direction (clockwise) until a reading of 50 microamperes is observed on TS-656/U meter.

j. Remove the protective plate over the potentiometer bracket and adjust potentiometer 2A15A2R7 (fig. 3-18) for a 2A15M1 meter indication of 100. If a meter indication of 100 cannot be obtained, refer to the troubleshooting chart

(para 3-12b, item No. 81) for corrective action upon completion of this procedure.

k. Turn the TS-656/U off and remove the connector adapter from connector 2A16WIXA12A.

l. Reinstall alarm monitor 2A12 on plate assembly 2A16 (TM 11-820-695-12).

m. Set POWER ON/OFF switch 2A15A2S1 on meter panel assembly 2A15A2S1 to ON.

**3-65. Calibration of R-1467(P)/GRC-144(V) and R-1467(P)/GRC-144(V) Local Oscillator Metering Circuits**

a. Turn Test Set, Radio Frequency Power AN/USM-161 and Signal Generator AN/URM-2B on and allow a 30-minute warmup period.

b. After the warmup period, calibrate the AN/USM-161 using the procedures given in TM 11-6625-498-12 and calibrate the AN/URM-52B at 4700 MHz using the procedures given in TM 11-6625-214-10.

c. Connect the equipment as shown in figure 3-32.

d. On the AN/USM-161, set the BIAS-READ switch to READ, turn the POWER RANGE switch to 3.0 MW +5 DBM, turn the COMP ATTENUATOR dial to 0, and turn the POWER indicator dial for a dial scale indication of 1.0 on the center scale.

e. Adjust the OUTPUT ATTEN control on the AN/URM-2B for a null indication on the AN/USM-161 NULL INDICATOR meter.

f. Adjust the POWER SET control on the AN/URM-2B for an index indication of 0 dbm on the OUTPUT ATTEN dial.

g. Turn the AN/USM-161 off and disconnect RF Cable CG-92D/U from Adapter UG-29B/U (fig. 5-2).

h. Set the OUTPUT ATTEN control on AN/URM-52B for a dial scale indication of -6 dbm.

i. Record the R-1467(P)/GRC-144(V) operating frequency.

j. On R-1467(P)/GRC-144(V), set local oscillator bandpass filter 2FL6 and electrical frequency synthesizer 2A14 controls to 4700 MHz.

k. Disconnect coaxial cable 2W9 (fig. 324) from local oscillator bandpass filter 2FL6, l. Connect the equipment as shown in figure 3-27.

m. Turn meter selector switch 2A15A2S1 on meter panel assembly 2A15A2 to LOCAL OSC POWER.

i. Fine tune the SIGNAL FREQUENCY control on AN/URM-2B for a peak indication on meter 2A165A2M1.

o. Remove the protective plate over the potentiometer bracket, and adjust potentiometer 2A15A2R5 (fig. 3-18) for a 2A15A2M1 meter indication of 30. If a meter indication cannot be obtained, refer to the troubleshooting chart (para 6-12b, item No. 3) for corrective action. Do not continue this procedure.

p. Disconnect the test equipment from coaxial cable 2W9.

q. Connect coaxial cable 2W9 to local oscillator bandpass filter 2FL6.

r. Turn the AN/URM-2B off.

**NOTE**

**Do not calibrate any of the following R-1467(P)/GRC-144(V) local oscillator metering circuits if the LOCAL OSC POWER metering circuit (step o above) could not be adjusted to obtain a 2A15A2M1 meter indication of 30.**

s. To calibrate any of the following R-1467(P)/GRC-144(V) local oscillator metering circuits, turn meter selector switch 2A15A2S1 (fig. 3-18) to the circuit to be calibrated and observe the indication on meter 2A15A2M1. If meter indication is not 100, remove the protective plate over the potentiometer bracket and adjust the associated potentiometer (listed below) for a 2A15A2M1 meter indication of 100. If a meter indication of 100 cannot be obtained, refer to the troubleshooting chart (para 3-12b, item No. 33 through 36) for corrective action.

<i>Circuit to be calibrated</i>	<i>Potentiometer (fig. 3-4)</i>
FREQ MIXER CURRENT 1.....	2A15A2R3
FREQ MIXER CURRENT 2.....	2A15A2R4
MULT-OSC.....	2A15A2R6

t. On R-1467/GRC-144, reset the controls on 2FL6 and 2A14 to the operating frequency recorded in step i.

**3-66. R-1467(P)/GRC-144(V) and R-1467 (P)/GRC-144(V) Carrier Alarm Adjustment**

**NOTE**

**Performing this procedure will affect the calibration of the T-1054(P)/GRC-144(V) radio test set. Therefore, perform the radio test set calibration procedure given in paragraph -61 upon completion of the following procedure.**

a. Turn Test Set, Radio Frequency Power AN/USM-161 and Signal Generator AN/URM-52B ON and allow a 30-minute warmup period.

b. After the warmup period, calibrate the AN/USM-161 using the procedures given in TM 11-6625-498-12 and calibrate the AN/URM-52B at 4700 MHz using the procedures given in TM 11-6625-214-10.

c. Connect the equipment as shown in figure 3-32.

d. On the AN/USM-161, set the BIAS-READ switch to READ, turn the POWER RANGE switch to 3.0 MW +5 DBM, turn the COMP ATTENUATOR dial to 0, and turn the POWER indicator dial for a dial scale indication of 1.0 on the center scale.

e. Adjust the OUTPUT ATTEN control on the AN/URM-52B for a null indication on the AN/USM-161 NULL INDICATOR meter.

f. Adjust the POWER SET control on the AN/URM-52B for an index indication of 0 dbm on the OUTPUT ATTEN dial.

g. Turn the AN/USM-161 off and disconnect RF cable CG-92D/U from Adapter UG-29B/U (fig. 3432).

h. Set the OUTPUT ATTEN control on AN/URM-52B for a dial scale indication of -71 dbm.

i. Set Switch, Waveguide SA-1679/GRC to the TO LOAD (TEST) position.

j. Disconnect the antenna waveguide from the rf entry panel on the external shelter wall.

k. Disconnect the coaxial cable connected to Coupler, Directional CU-1890/GRC.

l. Record the R-1467/GRC-144 operating frequency.

m. Connect the equipment as shown in figure 3-33.

n. On R-1467/GRC-144, set the preselector bandpass filter 2FL4, post selector bandpass filter 2FL5, local oscillator bandpass filter 2FL6, and electrical frequency synthesizer 2A14 controls to 4700 MHz.

o. Remove the dust cover from the ATTEN ADJ control on Coupler, Directional CU-1890/GRC and, using a screwdriver, turn the ATTEN ADJ control clockwise until mechanical stop is reached.

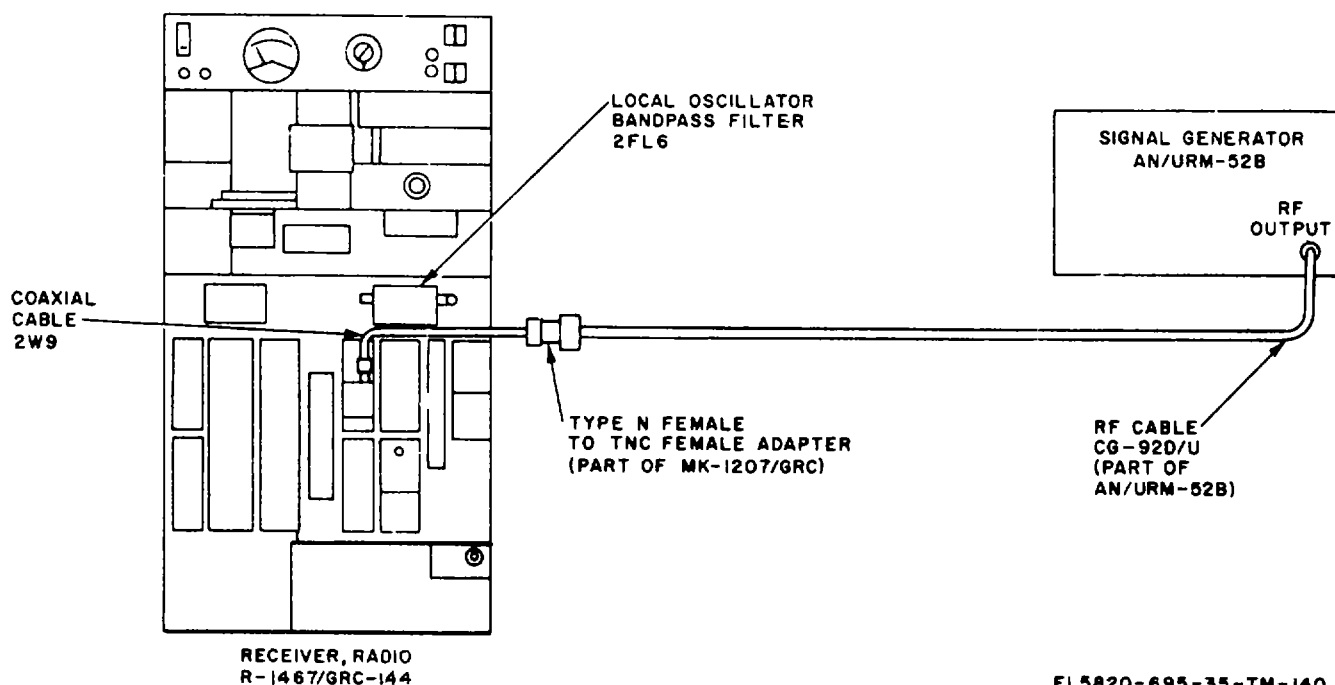
p. Turn the AGC SEL switch on 70 MHz intermediate frequency amplifier 2A5 to TEST.

q. Turn meter selector switch 2A15A2S1' on meter panel assembly 2A15A2 to CARRIER (IF).

**NOTE**

If meter 2A15A2 indication is off scale, when performing step r, reduce the POWER SET control on AN/URM-52B for an on scale meter reading. After performing step r, increase POWER SET control for a dial scale indication of -71 dbm on the AN/URM-42B.

r. Fine tune the SIGNAL FREQUENCY control on AN/URM-52B for a peak indication on meter 2A15A2M1.



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Figure 3-27. Calibration of R-1467/GRC-144 local oscillator metering circuits, equipment connections.

s. Meter indication on meter panel assembly 2A15A2 should be 150. If it is not, remove the green cap from the IF GAIN control on 70 MHz intermediate frequency amplifier 2A5 and, using the tuning tool, adjust the IF GAIN control for a meter indication of 150.

t. Turn meter selector switch 2A15A2S1 to OFF (TRANSIT).

u. Set the OUTPUT ATTEN control on AN/URM-52B for a dial scale indication of 7 dbm.

v. Set AGC SEL switch on 70 MHz intermediate frequency amplifier 2A5 to DIV OFF.

w. Remove the green cap from the ALM SET control on 70 MHz intermediate frequency amplifier 2A5 and, using the tuning tool, slowly adjust the control until the CARR (IF) alarm indicator on meter panel assembly 2A15A2 lights red. After the CARR (IF) alarm indicator lights red, adjust the AIM SET control in the opposite direction until the CARR (IF) alarm indicator lights green.

x. Replace the green caps removed in steps 8 and w.

y. Set meter selector switch 2A15A2SW1 to CARRIER (IF) and set the AGC SEL switch on 70 MHz intermediate frequency amplifier 2A5 to TEST.

z. Calibrate the radio test set by performing steps s through ai of paragraph 3-1.

### 3-67. Calibration of ID-1 708/GRC Meter 3M1

a. Turn on Test Set, Electrical Meter TS656/U and allow a 5-minute warmup period.

b. On the TS-656/U, set the FUNCTION switch

to DIR OUR, the CURRENT switch to 100 MICRO-AMP, and turn the DECREASE/INCREASE control counterclockwise, until mechanical stop is reached.

c. Set ON/OFF (TRANSIT) switch 8S1 on ID-1708/GRC to OFF (TRANSIT) (fig. 3-25).

d. Using a screwdriver, adjust the screw on the front of meter 3M1 for a zero meter indication.

e. Set ON/OFF (TRANSIT) switch 3S1 on ID-1708/GRC to ON.

f. Connect a test lead between the DIR CUR TERMINAL ON TS-56/U and pin A of ID-1708/GRC input connector 3W2P1.

g. Connect a test lead between the COMMON terminal on TS-656/U and pin B of ID-1708/GRC input connector.

h. On TS-656/U, hold the TEST switch in TEST (up) position and turn the DECREASE/INCREASE control in INCREASE direction (clockwise) until meter 3M1 on ID-1708/GRC indicates 100.

i. With the TEST switch on TS-656/U in the up position, the TS-656/U meter indication shall be  $50 \pm 10$  microamperes. If it is not, replace meter 3M1 (para 3-58) and repeat the calibration procedure.

j. Turn the TS-656/U off and disconnect the test leads.

k. Set ON/OFF (TRANSIT) switch 8S1 on ID-1708/GRC to OFF (TRANSIT).

## Section V. DIRECT SUPPORT TESTING PROCEDURES

### 3-68. General

a. The testing procedures contained in this section are used to determine whether repaired equipment is performing satisfactorily for return to users.

b. The testing procedures contained in this section assume that the equipment being tested is turned on and operating at the start of the procedure. When performing the tests, comply with the instructions preceding each chart before proceeding to the chart. Perform each test in sequence. *Do not vary the sequewe.* For each step, perform all the actions

required in the *Control settings* column; then perform each specific test procedure and verify it against its performance standard. Upon completion of the test procedure, turn off and disconnect the test equipment, and return the equipment to its original operating condition.

### 3-69. Test Equipment, Tools and Materials

All test equipment and tools required to perform the testing procedures provided in this section are listed in the following charts.



**a. Test Equipment.**

<b>Nomenclature</b>	<b>National stock No.</b>	<b>Technical Manual</b>
Counter Electronic, Digital Readout AN/USM-207	6625-00-911-6368	TM 11-6625-700-10
Test Set, Radio Frequency Power AN/USM-181	6625-00-892-5541	TM 11-6625-498-12
Signal Generator AN/USM-52B Meter Calibration Facilities Kit MK-1207/GRC	6625-00-965-1501  6625-00-133-7863	TM 11-6625-214-10  -----

- Signal Generator, (Ku Band) HP 626A
- Adapter, SMA(M) to  
N(F), Narda 57
- Adapter W/G/SMA.  
Narda 4609
- Attenuator, Narda 4779-3
- Test Cable N(H) to N(M) Pamona 1658-T-60
- Termination, Short, Narda  
4230-416
- Thermister Mount, (C Band) HP 478A
- Thermister Mount, (Ku Band) HP 486A
- Power Meter Hewlett Packard 432A
- Directional Coupler, Hewlett-Packard  
P752D
- Waveguide, Flexible  
Airtron AT-3-3-062-60
- Waveguide, Flexible, Hewlett-Packard  
11503A
- Attenuator, Waveline 707-20

**b. Tools.**

<b>Nomenclature</b>	<b>National stock No.</b>	<b>Technical Manual</b>
Tool Kit, Electronic Equipment, TK-105/G	5180-00-610-8177	SC 5180-91-CL-R07
Tool Kit, Electronic Equipment, TK-100/G	5180-00-605-0079	SC 5180-91-CL-R07

**c. Special Tool List and Fabrication.**

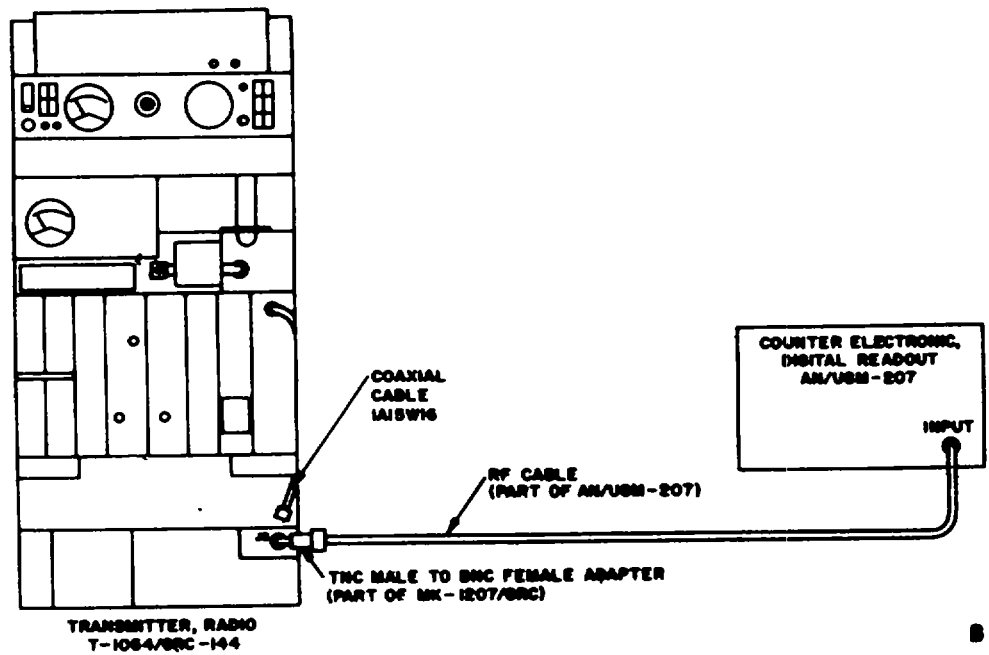
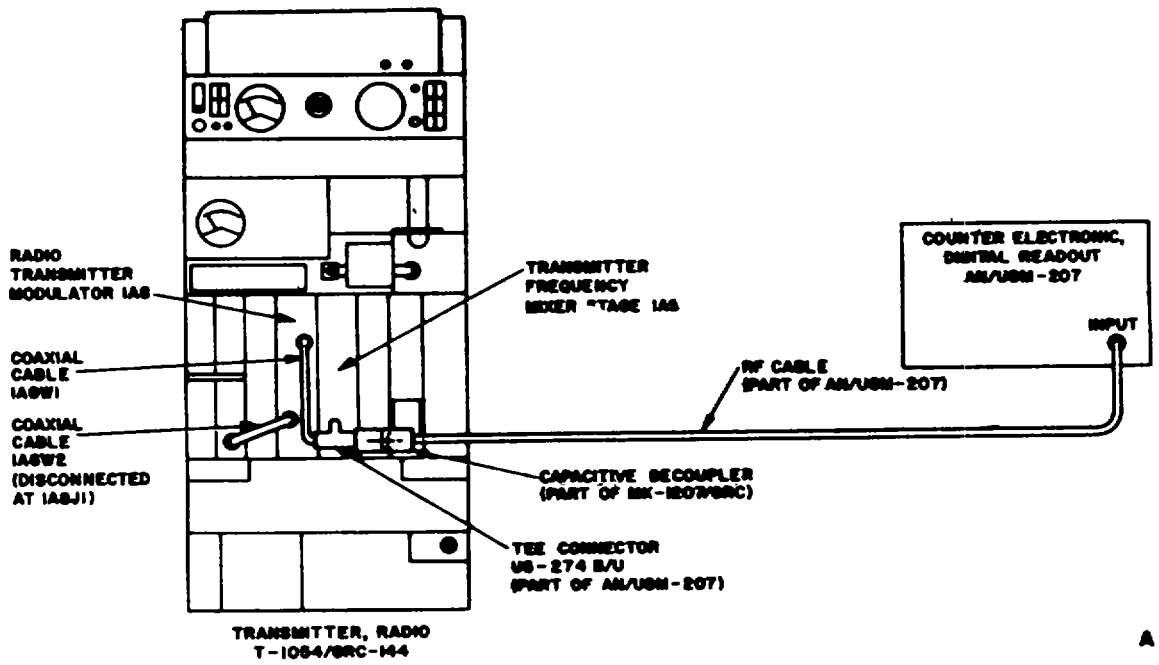
- (1) Tool. R-1467(P)A/GRC-144(V)  
Alignment Tool (NSN 5120-00-724-3767).
- (2) Fabrication. Taper the tuning blade to  
a maximum width of 0.058 inch and 45°.

**3-70. Physical Tests and Inspection**

- a. *Test Equipment and Materials.* None.
- b. *Test Connections and Conditions.*
  - (1) Set POWER ON/OFF switch on  
meter panel assembly 1A15A8 to OFF.
  - (2) Set POWER ON/OFF switch on  
meter panel assembly 2A15A2 to OFF.

c. Procedure.

Step No.	Test equipment	Control setting		
		Equipment under test	Test procedure	Performance standard
1	None	Controls may be in any position.	<p>a. Inspect all controls and mechanical assemblies for loose or missing screws, bolts, or nuts.</p> <p>b. Inspect subassemblies and their cases for physical damage and condition of finish.</p> <p><b>Note. Touchup painting is recommended whenever practicable. Screwheads, receptacles, connectors, and other plated parts will not be painted or polished with abrasive</b></p> <p>c. Inspect all connectors, plugs, receptacles, and meter and dial faceplates for looseness and damage.</p> <p>d. Remove fuseholder caps; inspect fuseholder for damage and fuses for correct type and rating.</p> <p>e. Inspect air filters for cleanliness and serviceability.</p>	<p>a. No loose or missing parts; screws, nuts, and bolts are tight</p> <p>b. No physical damage (bends, cracks, splits, <i>etch</i>) evident. Painted surfaces do not show bare metal. Panel lettering legible.</p> <p>c. All plugs and connectors are tight All receptacles are tight and free from damage. Meter and dial faceplates are secure and are not split or cracked.</p> <p>d. Fuseholders are in serviceable condition Each fuseholder contains a good fuse of proper type and rating, as indicated on the panel.</p> <p>e. Air filters are in a clean and serviceable condition.</p>



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Figure 3-28. T-1054/GRC-144 frequency accuracy test setup.

**3-71. T-1054(P)/GRC-144(V) and T-1054 (P)/GRC-144(V) Frequency Accuracy Test**

a. *Test Equipment and Materials.*

- (1) Counter Electronic, Digital Readout AN/USM-207.
- (2) Capacitive Decoupler (part of Meter Calibration Facilities Kit MK-1207/GRC).
- (3) Tee Connector, UG-274/B (part of AN/USM-207).

(4) TNC male to BNC female adapter (part of Meter Calibration Facilities Kit MK-1207/GRC).

b. *Test Connections and Conditions.*

- (1) Record the T-1054(P)/GRC-144(V) operating frequency.
- (2) Set Switch, Waveguide SA-1679/GRC to the TO LOAD (TEST) position.

c. *Initial Test Equipment Calibration.* Turn on the AN/USM-207 (TM 11-6625-700-10) and allow a 16-minute warmup period.

d. Procedure.

		<b>Control setting</b>		
<b>Step No.</b>	<b>Test equipment</b>	<b>Equipment under test</b>	<b>Test procedure</b>	<b>Performance standard</b>
1	AN/USM-2107 SENSITIVITY: PLUG-IN FUNCTION: FREQ Time base switch: GATE TIME (SEC -1) -10' DISPLAY: Desired display time Converter attenuator switches: 10V MAX DIRECT-HETERODYNE: HETERODYNE Mixing frequency selector switch: 100	N/A	<ul style="list-style-type: none"> <li>a. Disconnect coaxial cable 1A6W2 from the J1 connector on radio transmitter modulator 1A8.</li> <li>b. Disconnect coaxial cable 1A8W1 from the A1J1 connector on transmitter frequency mixer stage 1A9.</li> <li>c. Connect the equipment as shown in A, figure 3-28 Note that the Tee Connector is also connected to A1J1 on 1A9.</li> <li>d. Observe the LEVEL METER on AN/USM-207. If it reads in the green zone, proceed to f below. Otherwise, proceed to a below.</li> <li>e. Alternately set the upper and lower converter attenuator switches on AN/USM-207 to the left, one position at a time, until LEVEL METER indication is in the green zone.</li> <li>f. Observe digital display on AN/USM-27.</li> <li>g. Disconnect the AN/USM-207 and connect cables 1A8W1 to 1A9A1J1 and 1A6W2 to 1A8J1.</li> </ul>	<ul style="list-style-type: none"> <li>a. None.</li> <li>b. None.</li> <li>c. None.</li> <li>d. None.</li> <li>e. None.</li> <li>f. Digital display on ANUSM-(shell be 50 MHz ±20 kHz.</li> <li>g. None.</li> </ul>
2	Same as step 1, except: Set mixing frequency selector switch to 250.	N/A	<ul style="list-style-type: none"> <li>a. Set the controls on electrical frequency synthesizer 1A14 to 4490.0 MHz.</li> <li>b. Disconnect coaxial cable 1A15W16 from the J8 connector on electrical frequency synthesizer 1A14.</li> <li>c. Connect the equipment as shown in B, figure -8.</li> <li>d. Observe the LEVEL METER on AN/USM-207. If it reads in the green zone, proceed to f below. Otherwise, proceed to e below.</li> <li>e. Alternately set the upper and lower converter attenuator</li> </ul>	<ul style="list-style-type: none"> <li>a. None.</li> <li>b. None.</li> <li>c. None.</li> <li>d. None.</li> <li>e. None.</li> </ul>

*Control setting*

<b>Step No.</b>	<b>Test Equipment</b>	<b>Equipment under test</b>	<b>Test Procedure</b>	<b>Performance Standard</b>
			switches on AN/USM-D(207 to the left, one position at a time, until LEVEL METER indication is in the green zone	
			f. Observe digital display on AN/USM-207	f. Digital display on AN/USM-207 shall be 40 MHz $\pm$ 3 kHz



3-72. T-1054(P)/GRC-144(V) and  
T-1054 (P)A/GRC-144(V) Output  
Power Test

- a. *Test Equipment and Materials.* Test Set, Radio Frequency Power AN/USM-161.
- b. *Test Connections and Conditions.*

(1) Record the T-1054(P)/GRC-144(V) operating frequency.

(2) Insure that Switch, Waveguide SA-1679/GRC-144 is set to the TO ANTENNA (NORMAL) position.

c. *Initial Test Equipment Calibration.* Turn on the AN/USM-161 and allow a 80SO-minute warm- up period. Use the procedures given in TM11-6625-98-12 to calibrate the AN/USM-161 after the warmup period is over.

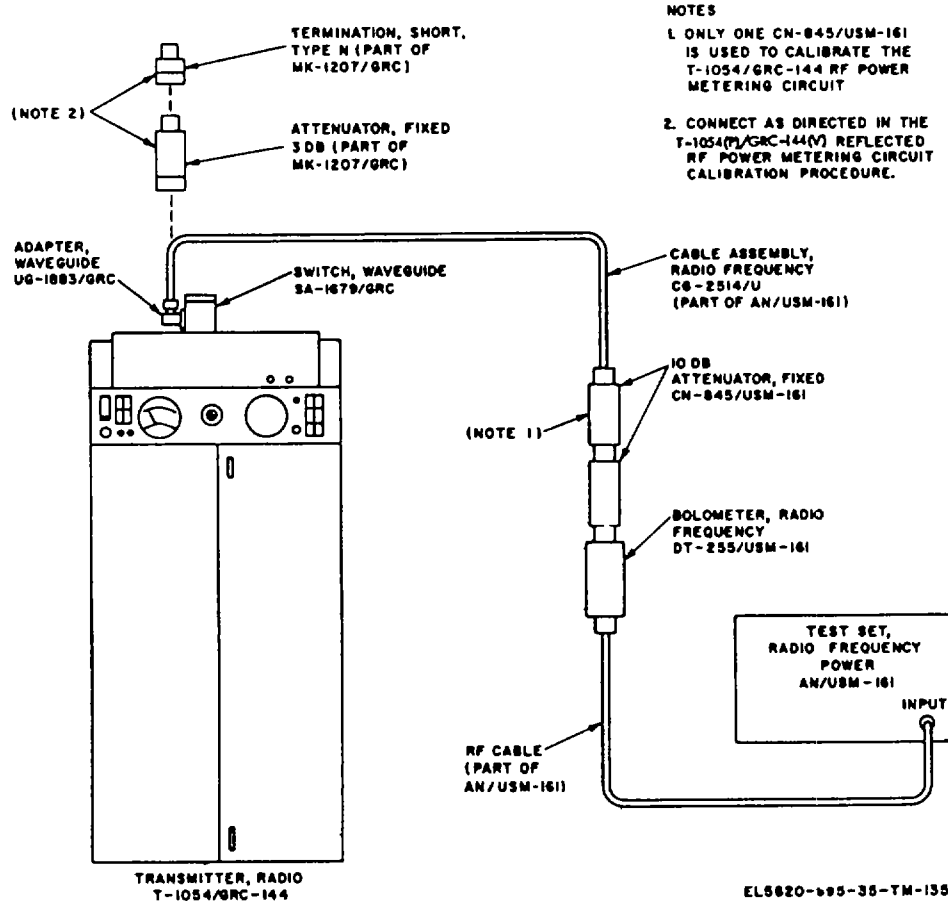


Figure 3-9. T-1054(P)/GRC-144(V) output power test setup.

d. Procedure.

Control setting

Step No.	Test Equipment	Equipment under Test	Test procedure	Performance Standard
1.	AN/USM-161 POWER RANGE 10 MW + 10 DBM POWER: 1.0 BIAS-READ: READ COMP ATTENUATOR: 0	N/A	<p>a. Remove Dummy load Electrical DA-541/GRC from Adapter, Waveguide UG-1883/GRC.</p> <p>b. Connect the equipment as shown in figure 3-29.</p> <p>c. Set Switch, Waveguide SA-1679/GRC to the TO LOAD (TEST) position.</p> <p>d. Set the controls on radio frequency bandpass filter 1FL3 and electrical frequency synthesizer 1A14 to 4400.0 MHz.</p> <p>e. Calculate the calibration plate correction factors for both CG-2514/U. And the CG-251/U Algebraically add the correction factors .If the sum of the correction factors is between -2.2 db and +2.2 db; set the COMP ATTENUATOR dial on the AN/USM-161 for the computed correction factor and read the outermost scale on the POWER control indicator, after it is adjusted for a null indication on the NULL INDICATOR meter .Multiply this indication by 1000 to obtain the T-1054(p)/GRC-144(V)-output power in milliwatts. If the computed correction factor is not between <math>\pm 2.2</math> db, refer to TM 11-6625-498-12 to determine the AN/USM-161 power indication.</p>	<p>a. None.</p> <p>b. None.</p> <p>c. None.</p> <p>d. None.</p> <p>e. T-1054(P)/GRC-I44(V) output as indicated on AN/JSM-161 shall be 150 milliwatts minimum.</p>
2.	Same as step 1.	N/A	<p>a. .Set the controls on radio frequency bandpass filter 1FL3 and electrical frequency synthesizer 1A14 to 4700.0 MHz.</p>	<p>a. None.</p>
3.	Same as step 1.	N/A	<p>b. Same as step 1e.</p> <p>a. Set the controls on radio frequency bandpass filter 1FL3 and electrical-frequency synthesizer 1A14 to 5000.0 MHz.</p> <p>b. Same as step 1e.</p>	<p>b. Same as step 1e.</p> <p>a. None.</p> <p>b. Same as step 1e.</p>
3-73.	R-1467(P)/GRC-144(V) and R-1467(P)A/GRC-144(V) Frequency Accuracy Test		<p>(3) TNC male to BNC female adapter (part of Meter Calibration Facilities Kit MK-1207/GRC).</p> <p>b. <i>Test Connections and Conditions.</i> Record the R-1467(P)/GRC -1440) operating frequency.</p> <p>c. <i>Initial Test Equipment Calibration</i> Turn on the KNIUSM-207 (TM 11762500-10) and allow a 15minute warmup period.</p>	
	<p>a. <i>Test Equipment and Materials.</i></p> <p>(1) Counter Electronic, Digital Readout AN/USM-207.</p> <p>(2) Selector Adapter, type 50-177-6801 (part of Meter Calibration Facilities Kit MK-1207/GRC).</p>			



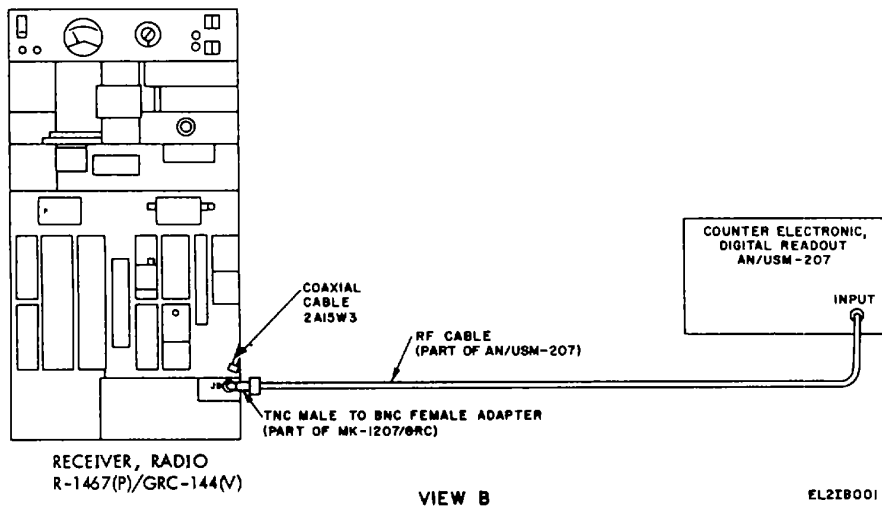
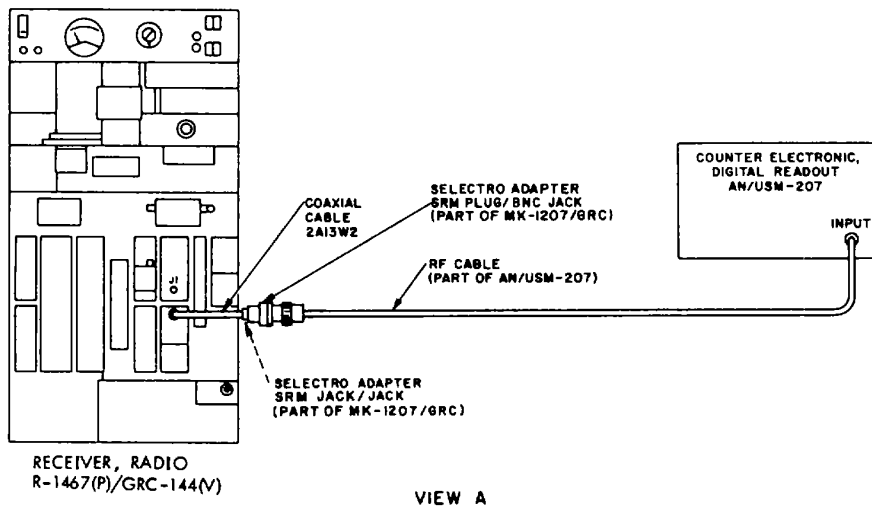


Figure 3-30. R-1467(P)/GRC-144(V) frequency accuracy test setup.

d. Procedure.

Control setting

Step No	Test Equipment	Equipment under Test	Test procedure	Performance Standard
1.	<p>AN/USM-207                      SENSITIVITY : PLUG-IN                      FUNCTION: FREQ                      Time has switch: GATE                      TIME (SEC -) -10                      DISPLAY: Desired display time                      Cone attenuator switches:                      10V MAX                      Mixing frequency selector switch: 200</p>	N/A	<p>a. Disconnect coaxial 2A13W2 from the J1 connector on receiver frequency mixer stage 2A 8.                      b. Connect the equipment as shown in A, figure 3-30.                      c. Observe the LEVEL METER on AN/USM-207. If it reads in the green zone, proceed to e below. Otherwise, proceed to d below                      d. Alternately set the upper and lower converter attenuator switches on AN/USM-207 to the left, one position at a time, until LE'VEL METER indication- is in green zone</p>	<p>a. None.                      b. None.                      c. None.                      d. None.</p>
2.	<p>Same as step 1, except: Set mixing frequency selector switch to 250</p>	N/A	<p>a. Disconnect the selector adapter from the AN/UiM-207 IF cable and connect cable 2A13W2 to 2A8J1.                      b. Set the controls on electrical frequency synthesizer 2A14 to 4490.0 MHz                      c. Disconnect coaxial cable 2A15W3 from the J8 connector on electrical-frequency synthesizer 2A14.                      d. Connect the equipment as shown in B, figure 330.                      e. Observe the LEVEL METER on AN/USM-207. if it reads in the green zone, proceed to g below. Otherwise, proceed to f below.                      f. Alternately set the upper and lower converter attenuator switches on AIN/USM-07 to the left, one position at a time, until LEVEL METER indication is in the green zone.                      g. Observe digital display on AN/USM-207.</p>	<p>e. Digital display on AN/USM-207 shall be 220 MHz ±20 kHz.                      a. None.                      b. None.                      c. None.                      d. None.                      e. None.                      f. None.                      g. Digital display on AN/USM-207 shall be 40 MHz ± KHz.</p>

3-74. R-1467(P)/GRC-144V) and R-1467(P)A/ GRC-144(V) Local Oscillator Power Test

b. *Test Connections and Conditions.* Record the R-1467(P)/GRC-144(V) operating frequency.

a. *Test Equipment and Materials.*

- (1) Test Set, Radio Frequency Power AN/ USM-161.
- (2) Test N female to TNC female adapter (part of Meter Calibration Facilities Kit MK- 1207/GRC).

c. *Initial Test Equipment Calibration.* Turn on the AN/USM-161 and allow a 30-minute warmup period. Use the procedures given in TM 11 6625-498-12 to calibrate AN/USM-161 after the warmup period is over.

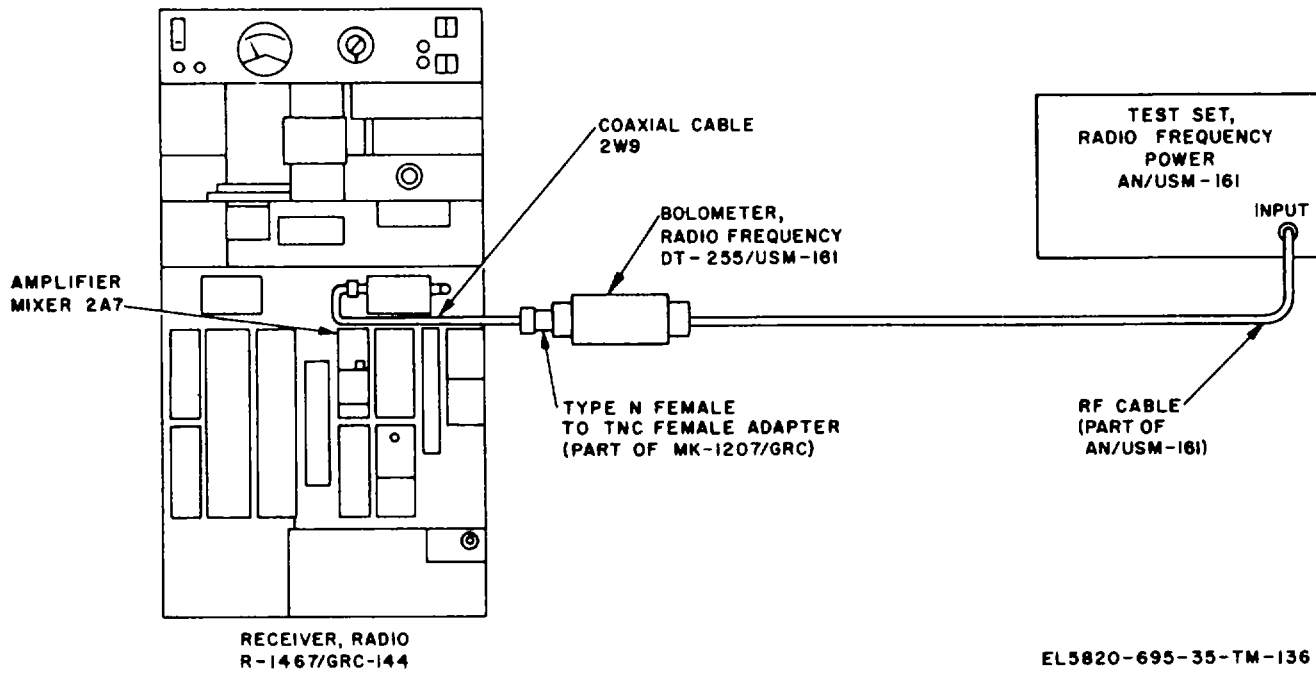


Figure 3-31. R-1467(P)/GRC-144(V) local oscillator power test setup.

*d. Procedure.*

**Control setting**

<b>Step No.</b>	<b>Test Equipment</b>	<b>Equipment under Test</b>	<b>Test procedure</b>	<b>Performance Standard</b>
1	AN/USM-161 POWER RANGE: 10 MW +10 DBW POWER: 1.0 BIAS-READ: READ COMP ATTENUATOR:0	N/A	<ul style="list-style-type: none"> <li>a. Disconnect coaxial 2W9 from the LO IN J2 connector on amplifier mixer 2A7.</li> <li>b. Set the controls on electrical frequency synthesizer 2A14 and local oscillator bandpass filter 2FL6 to 4400.0 MHz.</li> <li>c. Connect the equipment as shown in figure 3-31.</li> <li>d. Rotate the POWER control on AN/USM-it until a null Indication is obtained on the NULL INDICATOR meter.</li> <li>e. On the AN/USM -161, read the outermost on the POWER control indicator. Multiply this indication by 10 to obtain the R-147/GC-144 local oscillator-output power in milliwatts.</li> </ul>	<ul style="list-style-type: none"> <li>a. None.</li> <li>b. None</li> <li>c. None</li> <li>d. None.</li> <li>e. R-1467/GC-144 local oscillator output power shall be 0.4 milliwatt minimum</li> </ul>
2.	Same as step 1.	N/A	Repeat steps 1d and 1e leave for frequency of the 2A14 and 2FL6 at 4500, 4600, 4700, 4800, 4900, and 5000 MHz.	Same as 1e above for all frequencies.

3-75. R-1467(P)/GRC-144(V) and R-1467(P)/GRC-144(V) IF Gain and Carrier Alarm Test

a. *Test Equipment and Materials.*

- (1) Signal Generator AN/URM-52B.
- (2) Test Set, Radio Frequency Power AN/ USM-161.
- (3) Adapter UG-29B/U (part of Meter Calibration Facilities Kit, MK-1207/GRC).

b. *Test Connections and Conditions.* Performing this test will affect the calibration of the T54(P)/GRC-144(V) radio test set. Therefore, perform the radio test set calibration procedure given in paragraph 3-61 upon completion of the test procedure given in d below.

- (1) Set Switch, Waveguide SA-1679/GRC to the TO LOAD (TEST) position.
- (2) Disconnect the antenna waveguide from the rf entry panel on the external shelter wall.
- (3) Disconnect the coaxial cable connected to Coupler, Directional CU-1890/GRC.
- (4) Record the R-1467(P)/GRC-144(V) operating frequency.
- (5) The R-1467(P)/GRC-144(V)' must have a minimum of two hours warmup period before performing test procedure (d below).

c. *Initial Test Equipment Calibration..*

- (1) Turn on the AN/USM-161 and AN/URM-52B and allow a 30-minute warmup period.
- (2) Calibrate the AN/USM-161 using the procedures given in TM 11-6625-498-12.
- (3) Calibrate the AN/URM-52B at 4700 Mhz using the procedures given in TM 11-6625-498-12.
- (4) Connect the test equipment as shown in figure 3-32.
- (5) On the AN/UM-161, set the BIAS READ switch to READ, turn the POWER RANGE switch to 3.0 MW +5 DMB, and turn the POWER indicator dial for a dial scale indication of 1.0 on the center scale.
- (6) Adjust the OUTPUT ATTEN control on the AN/URM-52B for a null indication on the AN/USM-161 NULL INDICATOR meter.
- (7) Adjust the POWER SET control on the AN/URM-52B for an index indication of 0 dbm on the OUTPUT ATTEN dial.
- (8) Turn off the AN/USM-161 and disconnect RF Cable CG-92D/U from Adapter UG-29B/U (fig. 3-32).
- (9) Set the OUTPUT ATTEN control on AN/URM-2B for a dial scale indication of -71 dbm.

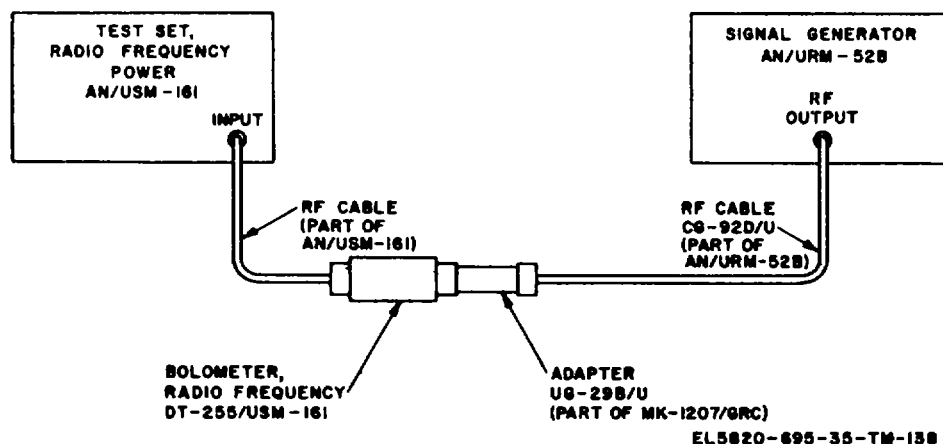
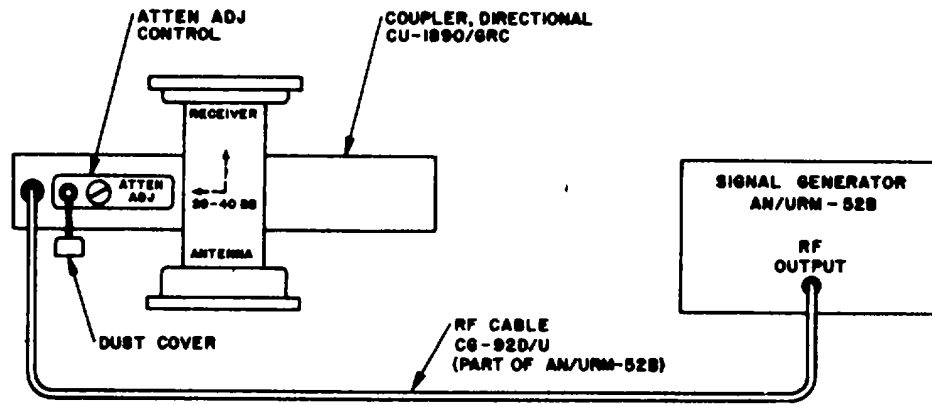
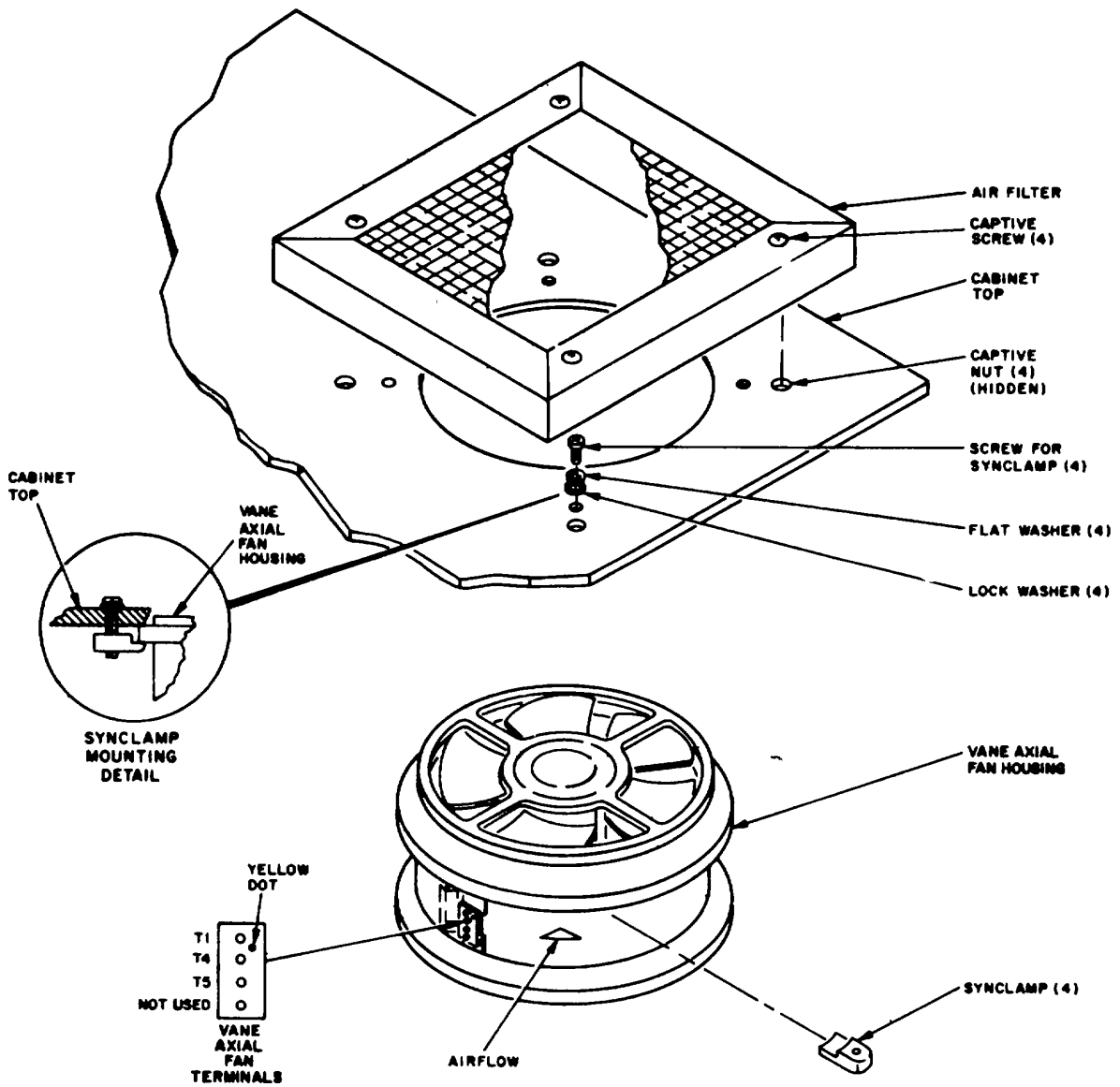


Figure 3-32. Calibration of Signal Generator AN/URM-52B equipment connections.



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Figure 3-33. If gain and carrier alarm test setup.



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Figure 3-34. Mounting detail, vans axial fans, 1A15B1 and 2A15B1.

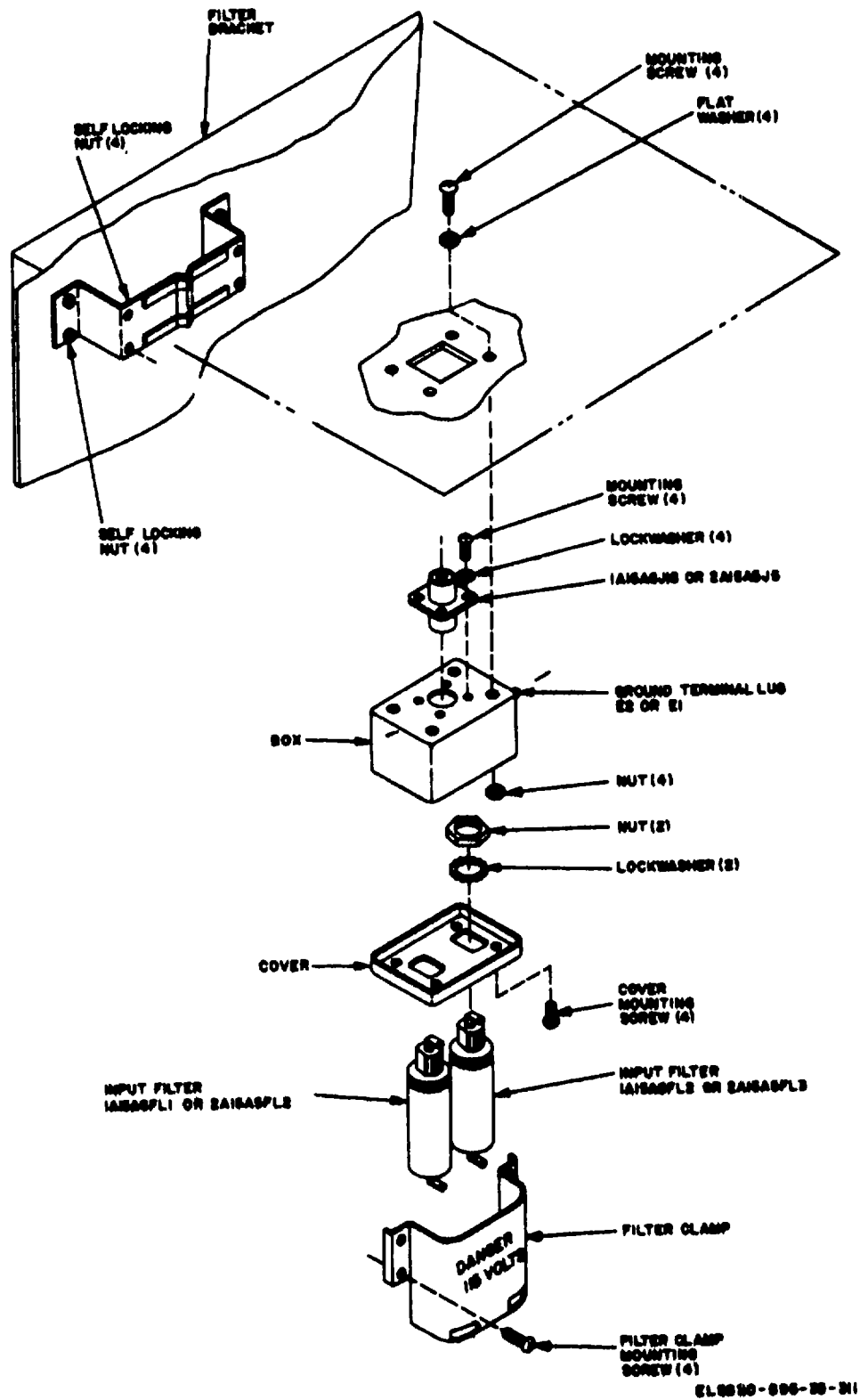


Figure 3-35. Exploded view input filter assembly 1A15A6 and 2A15A5.

d. Procedure.

Control setting

Step No.	Test Equipment	Equipment under Test	Test procedure	Performance Standard
1.	N/A	N/A	<p>a. On R-1467/GRC-144, set the preselector bandpass filter 2FLA post selector bandpass filter 2FLA, local oscillator bandpass filter 2FL6, and electrical frequency synthesizer 2A14 controls to 4700 MHz.</p> <p>b. Unscrew the dust cover from the ATTEN ADJ controls on Coupler, Directional CU-1890-GRC and, using a screwdriver turn the ATTEN ADJ control clockwise until mechanical stop is reached.</p> <p>c. Turn the AGC SEL switch on 70 MHz intermediate frequency amplifier 2A5 to TEST.</p> <p>d. Turn the meter selector switch on meter panel assembly 2A15A2 to CARRIER.</p>	<p>a. None</p> <p>b. None</p> <p>c. None</p> <p>d. None</p>
	(IF)		<p>e. Connect the equipment as shown in figure 3-63.</p> <p>f. Fine tune the SIGNAL FREQUENCY control on AN/URM 52B for a peak meter indication on meter panel assembly 2A15A2</p>	<p>e. None</p> <p>f. Meter indication on meter panel assembly 2A15A0 shall be <math>150 \pm 10</math>.</p>
2	N/A.	N/A	<p>Set the OUTPUT ATTEN control On AN/URM -52B for a dial scale indication of -67 dbm.</p> <p>b. Turn AGC SEL switch on 70 MHz intermitted frequency amplifier 2A5 to DIV OFF.</p> <p>c. Slowly adjust the OUTPUT ATTEN control on AN/URM-52B for a dial scale indication of -69 dbm.</p> <p><i>Note. Perform the radio test set calibration procedure given in paragraph 3-41 before turning off and disconnecting the test equipment.</i></p>	<p>a. None.</p> <p>b. CARR (IF) indicator on meter panel assembly 2A15A2 shall light green.</p> <p>c. CARR (IF) indicator on meter panel assembly 2A15A2 shall light red.</p>



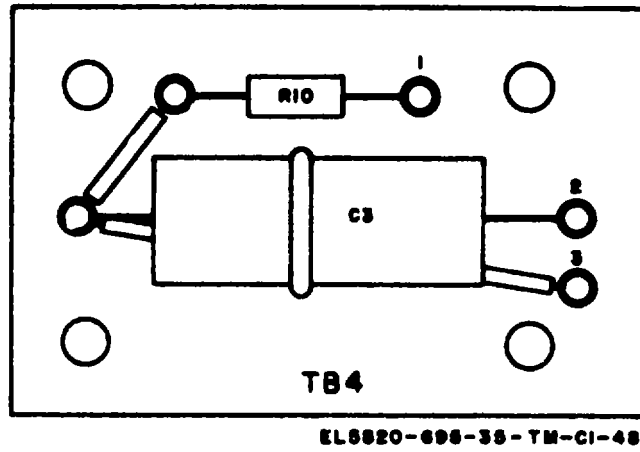
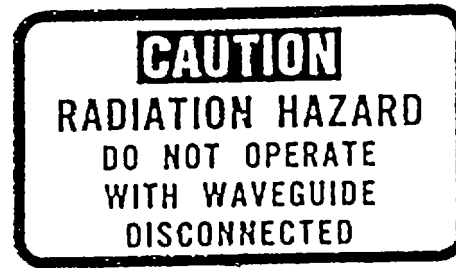


Figure 3-36. Transmitter cabinet, terminal board 1A15TB4, parts location

Change 1 3-100

3-76. AN/GRC-144(V)4 Output Power Test at 14.4 to 15.0 GHz and Power Alarm Calibration



Radio Set AN/GRC-144(V)4 output power test 14.4 to 15.0 GHz assumes that the T-1054(P)A/GRC-144 output power test has been performed and all performance standards are in accordance with paragraph 3-72.

a. Test Equipment and Materials.

- (1) Thermister Mount, Hewlett-Packard P486A
- (2) Power Meter, Hewlett-Packard 432A
- (3) Attenuator, Waveline 707-20

b. Test Connections and Conditions.

**NOTE**

To perform the AN/ GRC-144(V)4 output power test, the waveguide connection at Converter Multiplier CV-3633/ GRC-144(V) 3A7J4 ANT waveguide flange must be opened.

- (1) Record the T-1054(P)A/GRC144(V) and CV-3633/GRC-144(V) filters 3A3 and 3A4 operating frequency and dial settings respectively.

**NOTE**

Disregard status panel waveguide switch **FREQUENCY BAND IN USE** and transmitter **WAVEGUIDE SW** indicator alarms.

- (2) Insure that transmit waveguide switch is set to the 15 GHz TEST (TO LOAD) position. For the AN/GRC-144(V)4 optional configuration, insure that Switch, Waveguide SA-1679/GRC is set to the TO LOAD (TEST) position.

- (3) Open waveguide connection at Converter-Multiplier CV-3633/GRC-144(V) ANT J4 output and first shelter waveguide connection by removing screws that secure waveguide and the CV-3633/ GRC-144(V) together.

- (4) Move the waveguide to a safe location.

**CAUTION**

Do not support test equipment by waveguides. Test equipment must be properly supported.

**NOTE**

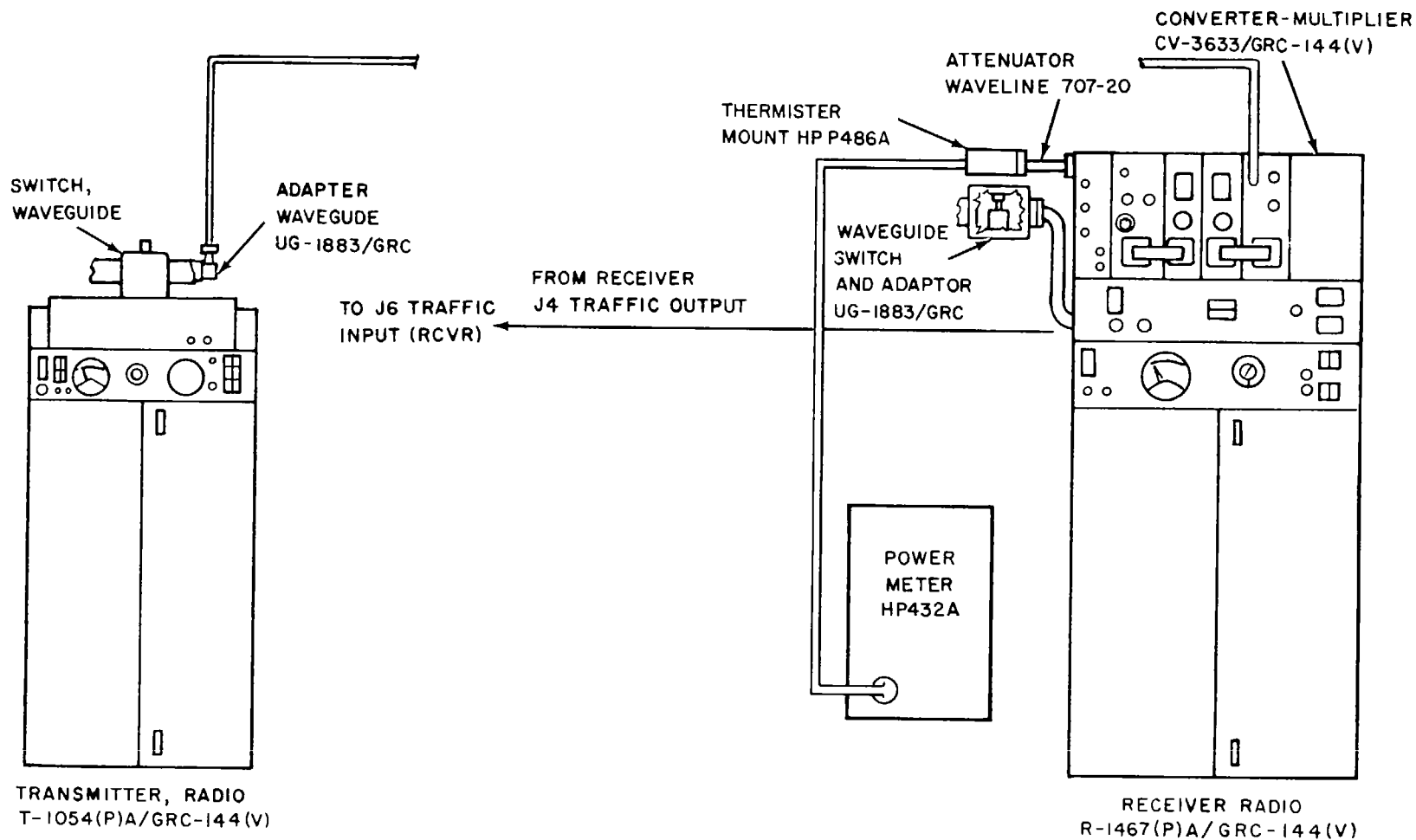
Locate the test equipment close to the CV-3633/ GRC-144(V) to permit proper interconnection.

- (5) Interconnect the test equipment in accordance with the test setup shown in figure 3-37.

c. Initial Test Equipment Calibration.

Turn on the test equipment and allow a 30 minute warmup period. Use the following technical manual procedures to zero the test equipment.

<u>Item</u>	<u>Technical Manual</u>
Power Meter, Hewlett Packard HP 432A	
Attenuator, Waveline 707-20 (prepare a calibration chart for the attenuator at 14.4 to 15.0 GHz at 0.1 GHz steps),	



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Figure 3-37. AN/GRC-144(V)4 output power test at 14.4 to 15.0 GHz.

d. Procedure

Step No	Test Equipment	Control Setting Equipment Under Test	Test Procedure	Performance Standard
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NOTE

1	POWER METER HP432A MOUNT RESISTANCE: 100 ohms RANGE: 10 mW (10 dBm) CALIBRATION FACTOR: As required to match Thermistor-mount calibration curve.	TRANSMITTER T-1054 (P)A/GRC-144 BANDPASS FILTER 1FL3 SET TO 4800 MHz modulator 1A8 BAND SET switches S101: 15 GHz S102: 14.4 to 14.6997 GHz - frequency synthesizer 1A14 thumb-wheel switches 4800.0 MHz CONVERTER-MULTIPLIER CV-3633/GRC -144(V) BANDPASS FILTERS 3A3: 14.8 GHz 3A4: 14.4 GHz	For the AN/GRC-144 (V)4 optional configuration figuration set Switch Waveguide SA-1679/GRC to the TO ANTENNA (NORMAL) position.  a. Set transmit switch waveguide to the 15 GHz OPERATE position.  b. Adjust AMPL-RF knob 1A3MP9 for a meter indication of 90 with meter panel assembly METER SELECTOR SWITCH (fig. 3-1) set to the TRAFFIC position.  c. Calibrate power meter and measure and record the CV-3633/GRC -144(V) output.	a. None  b. None  c. The CV-3633/GRC-144(V) output power as indicated on the power meter shall be 250 milliwatts (+24 dBm) minimum Ex: Power meter indication plus attenture calibration value for frequency equals power out.
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2 Same as step 1. N/A

NOTE

Repeat paragraph 3-76 steps (1) and b(2).

a. Set controls on transmitter T-1054(P)A/GRC-144 (V) frequency synthesizer 1A14 to 5000.0 MHz and modulator 1A8 BAND SET switch to 14.7-15 GHz, and Filter 1FL3 to 5000 MHz.	a. None.
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d. Procedure

Step No	Test Equipment	Control Setting Equipment Under Test	Test Procedure	Performance Standard
			<p>b. Set Converter-Multiplier CV-3633/GRC-144(V) bandpass filter 3A4 to 15.0 GHz.</p> <p>c. Calibrate power meter and measure and record the CV-3633/GRC-144(V) output.</p>	<p>b. None.</p> <p>c. The CV-3633/GRC-144(V) output power as indicated on the power meter shall be 250 milliwatts (+24 dBm) minimum. Ex.: Same as step c above.</p>
3	Same as step 1.	N/A	<p>Detune Transmitter-Radio T-1054 (P)A/GRC-144(V) bandpass filter 1FL3 until power meter indicates 6 dB less than indication recorded in step 2c.</p>	<p>The status panel ALARMS SUMMARY and Transmitter T-1054 (P)A/GRC-144(V) CNTRL ALARM indicators shall illuminate and audible alarm sound. If the alarm indications do not occur proceed to step 4 and perform the forward power threshold alarm calibration-procedures and repeat steps 1 b and 2c and 3a.</p>

d. Procedure

Step No	Test Equipment	Control Setting Equipment Under Test	Test Procedure	Performance Standard
4	Same as step 1.	N/A	<p>a. Remove the test lead from the mount in the R-1467(P)/A/GRC-144(V) SPECIAL TOOLS AND SPARE FUSES compartment</p> <p>b. Set meter panel assembly 2A15A2 switch to the + TEST position.</p> <p>c. Connect probe on one end of test to TEST LEAD jack on meter panel as-assembly 2A15A2 and connect probe on other end of test lead to the CV-3633/GRC-144(V) 3A5 TP3 PWR OUT test point.</p> <p>d. To calibrate the forward power threshold alarm, perform the following steps:                      (1) Using a small tuning tool turn the CV-3633/GRC-144(V) FWD PWR 3A1R2 screwdriver adjustment control clockwise if necessary until the status panel ALARM SUMMARY indicator is lit red.                      (2) Return filter 1FL3 to 5000 MHz, the SUMMARY ALARM shall turn green.</p>	<p>a. None.</p> <p>b. None.</p> <p>c. The test point meter indication should be in the yellow band 30 to full scale).</p> <p>d. None.</p>

## NOTE

## 3-77. CV-3633/GRC-144(V) Reflected Power Threshold Test and Calibration

Converter-Multiplier CV-3633/GRC-144(V) reflected power threshold test and calibration test assumes that the AN/GRC144(V)4 output power test at 14.4 to 15.0 GHz and power alarm calibration procedures have been performed and all performance standards are in accordance with paragraph 3-76.

a. Test Equipment and Materials

- (1) Adapter WG/SMA(F), Narda 4609,
- (2) Attenuator, Narda 4779-3,
- (3) Termination Short, Narda 4230-416.

b. Test Connections and Conditions

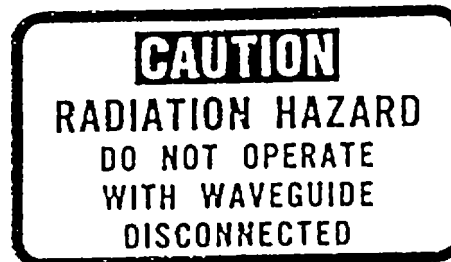
## NOTE

**To perform the AN/ GRC-144(V)4 output power test the waveguide connection at Converter Multiplier CV-3633/ GRC-144(V) 3A7J4 ANT waveguide flange must be opened.**

- (1) Record the T-1054(P)A/GRC144(V) and CV-3633/GRC-144(V) filter 3A3 and 3A4 operating frequency and dial settings respectively.

**Disregard status panel waveguide switch FREQUENCY BAND IN USE and transmitter WAVEGUIDE SW indicator alarms.**

- (2) Insure that transmit switch waveguide is set to the 15 GHz TEST (TC LOAO) position. For the AN/GRC-144(V)4 optional configuration, insure that Switch, Waveguide SA-1679/GRC is set to the TO LOAD (TEST) position.

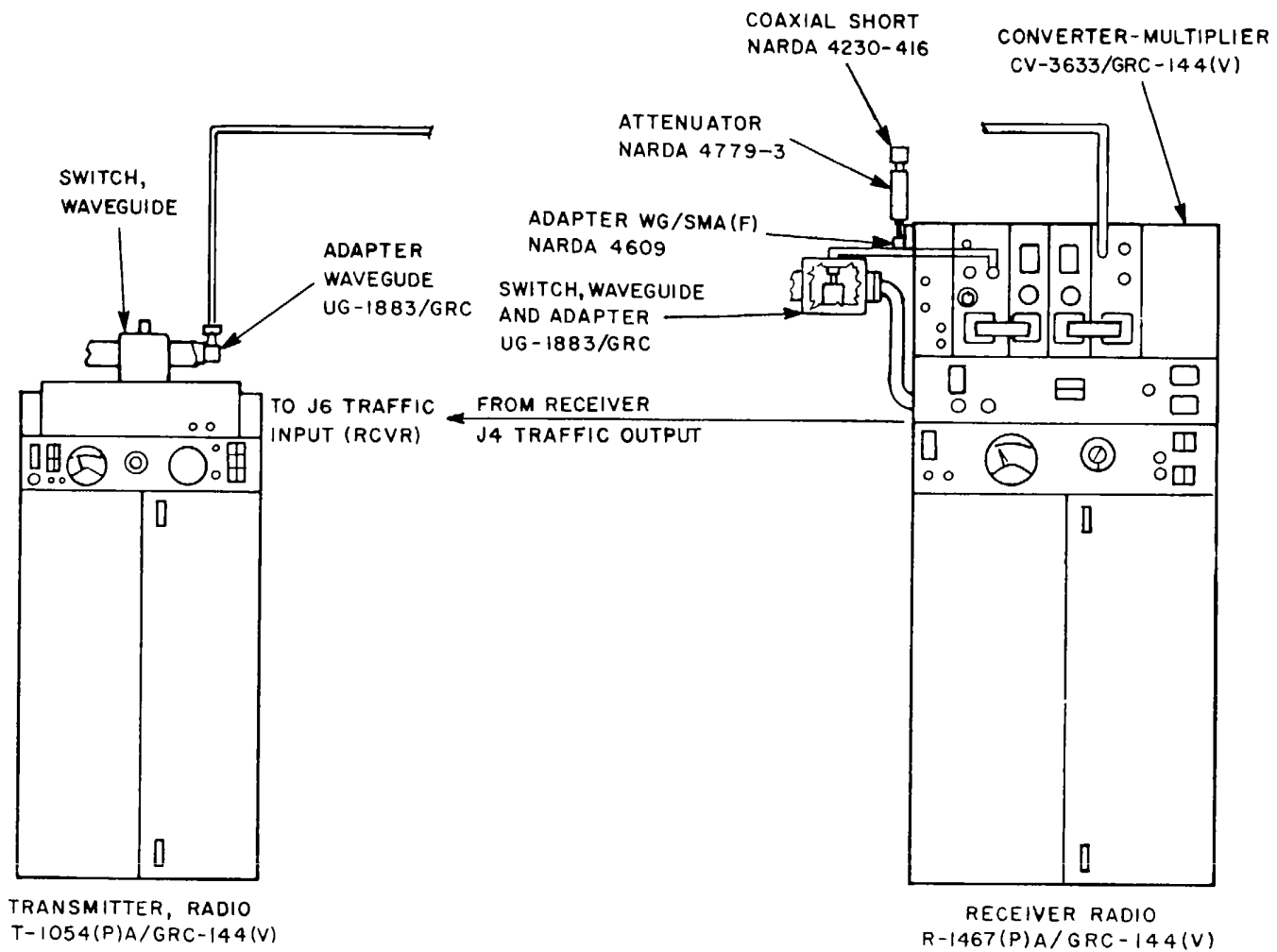


- (3) Open waveguide connection at Converter-Multiplier CV-3633/GRC -144(V) ANT 34 output and first shelter waveguide connection by removing Screws that secure waveguide and the CV-3633/GRC-144(V) together.

- (4) Move the waveguide to a safe location.

- (5) Interconnect the test equipment in accordance with the test setup shown in figure 3-38.

c. Initial Test Equipment Calibration. None.



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Figure 3-38. CV -3633/GRC-144(V) reflection power alarm threshold test and calibration.



Step		Control Setting		
No	Test Equipment	Equipment Under Test	Test Procedure	Performance Standard
1	None.	Transmitter T-1054 1054(P)A/GRC-144(V) Bandpass filter 1FL3 set to 4900 MHz Modulator 1A8 S1O1: 15 GHz S1O2: 14.7-15 GHz Frequency Synthesizer- 1A14 Thumb- wheel Switches 4900.0 MHz Converter- Multiplier CV- 3633/GRC-144(V) Bandpass Filter 3A3:14.8 GHz 3A4:14.7 GHz		
		N/A	NOTE  For the AN/GRC-144 (V)4 optional con- figuration set Switch Waveguide SA-1679/GRC to the TO ANTENNA (NORMAL) position. Set transmit waveguide switch to the 15 GHz OPERATE - position.	The status panel SUMMARY ALARM and Transmitter T-1054(P)A/GRC- 144(V) CNTRL ALARM indicators shall illuminate red and audible alarm shall sound. If the alarm indications do not occur proceed to step 2 and perform the reflected alarm adjustment range procedures and re- peat step 1.
	2. Same as step 1.	None	a. Remove test lead from the mount in the R-1467(P)A/GRC -144(V) SPECIAL TOOLS AND SPARE FUSES compartment	a. None.

Step	Control Setting	Equipment Under Test	Test Procedure	Performance Standard
No	Test Equipment			
			<p>b. Set the meter panel assembly 2A15A2 switch to the + TEST position.</p> <p>c. Connect probe on one end of test lead to TEST LEAD jack on meter panel assembly 2A15A2 and connect probe on other end of test lead to the CV-3633/GRC-144(V), 3A1A1, REFLD PWR test point.</p> <p>d. To verify the reflected power alarm adjustment range, perform the following steps:</p> <p>(1) Using a small tuning tool turn the 3A1 R27 REFLD PWR screwdriver adjustment control clockwise, until the status panel ALARMS SUMMARY indicator just changes from red to green.</p> <p>(2) Reconnect the shelter waveguide to the 3A734 (ANT) flange and perform the adjustment of paragraph 5-32, step t of TM 11-5820-695-12.</p>	<p>b. None.</p> <p>c. The test point meter indication-should read 80 minimum</p> <p>d. None.</p>

3-78. CV-3633/GRC-144(V) Local Oscillator Frequency Accuracy Test and Alarm Calibration

a. Test Equipment and Materials

- (1) Frequency Counter, Hewlett Packard 5340A.
- (2) Test Cable, N(M) to N(M), Pomona 1680-T-60.
- (3) Signal Generator, Hewlett Packard 626A.
- (4) Adapter WG/N(F), Narda 609.
- (5) Directional Coupler, Hewlett Packard P752D.
- (6) Waveguide, Flexible, HP11503A.

b. Test Connections and Conditions

Record the CV-3633/GRC-144(V) operating frequency.

**NOTE**

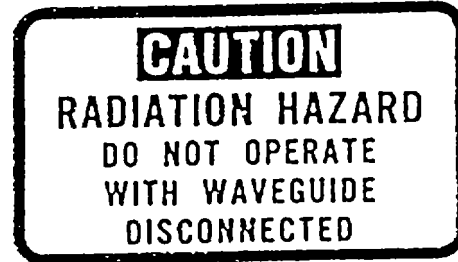
**To perform the AN/GRC-144(V)4 local oscillator frequency accuracy test and alarm calibration test, the waveguide connection at Converter-Multiplier CV-3633/GRC-144(V) 3A7J4 ANT waveguide flange must be opened.**

- (1) Record the T-1054(P)A/GRC144(V) and CV-3633/GRC-144(V) filter 3A3 and 3A4 operating frequency and dial settings respectively.

**NOTE**

**Disregard status panel waveguide switch FREQUENCY BAND IN USE and transmitter WAVEGUIDE SW indicator alarms.**

- (2) Insure that transmit switch waveguide is set to the 15 GHz TEST (TO LOAD) position. For the AN/GRC-144 (V)4 optional configuration, insure that Switch, Waveguide SA-1679/GRC is set to the TO LOAD (TEST) position.



- (3) Break waveguide connection at Converter-Multiplier CV-3633/GRC-144 (V) ANT J4 output and first shelter waveguide connection by removing screws that secure waveguide and the CV-3633/GRC-144(V) together.

- (4) Move the waveguide to a safe location.

- (5) Interconnect the test equipment in accordance with the test setup shown in figure 3-39.

c. Initial Test Equipment Calibration.

Turn on the frequency counter and signal generator and allow a 15 minute warmup period.

Step No	Test Equipment	Control Setting Equipment Under Test	Test Procedure	Performance Standard
1	FREQUENCY COUNTER HP 5340A RANGE: 250 MHz- 18 MHz RESOLUTION: 10kHz SIGNAL GENERATOR HP 626A MOD SELECTOR: CW FREQUENCY DIAL: 14700 MHz OUTPUT ATTEN DBM: ODBM POWER SET: As required for-10 DBM output.	Transmitter T-1054 (P)A/GRC-144(V) POWER ON/OFF switch to OFF.  Converter-Multi plier CV-3633/ GRC-144(V) BAND SET switch to position 1. BP Filter 3A3 set to 14700 MHz.	a. Disconnect coaxial cable from 3A2AT 2J2 connector on electronics frequency converter 3A2.  b. Connect the equip- ment as shown in figure 3-39, (solid line con- nections).  c. Observe the digital display on the frequency counter. NOTE Do not adjust signal generator fre- quency or output level during per- formance of this test.	a. None.  b. None.  c. Record for reference in later steps.
2	Same as step 1.	Receiver, Radio R-1467(P)A/GRC- 144(V), FL4 and FL5 set to 4700 MHz.	Connect the equip- ment as shown in figure 3-39 (dash- ed line connec- tions).	The digital dis- play on the frequency counter shall be the value recorded in step 1 minus 10 GHz ± 100 KHz.
3	Same as 1.	BAND SET switch to position 2.	Observe digital dis- play on the fre- quency counter.	The digital dis- play on the frequency counter shall be the value recorded in step 1 minus 10.02 GHz ± 100 KHz.

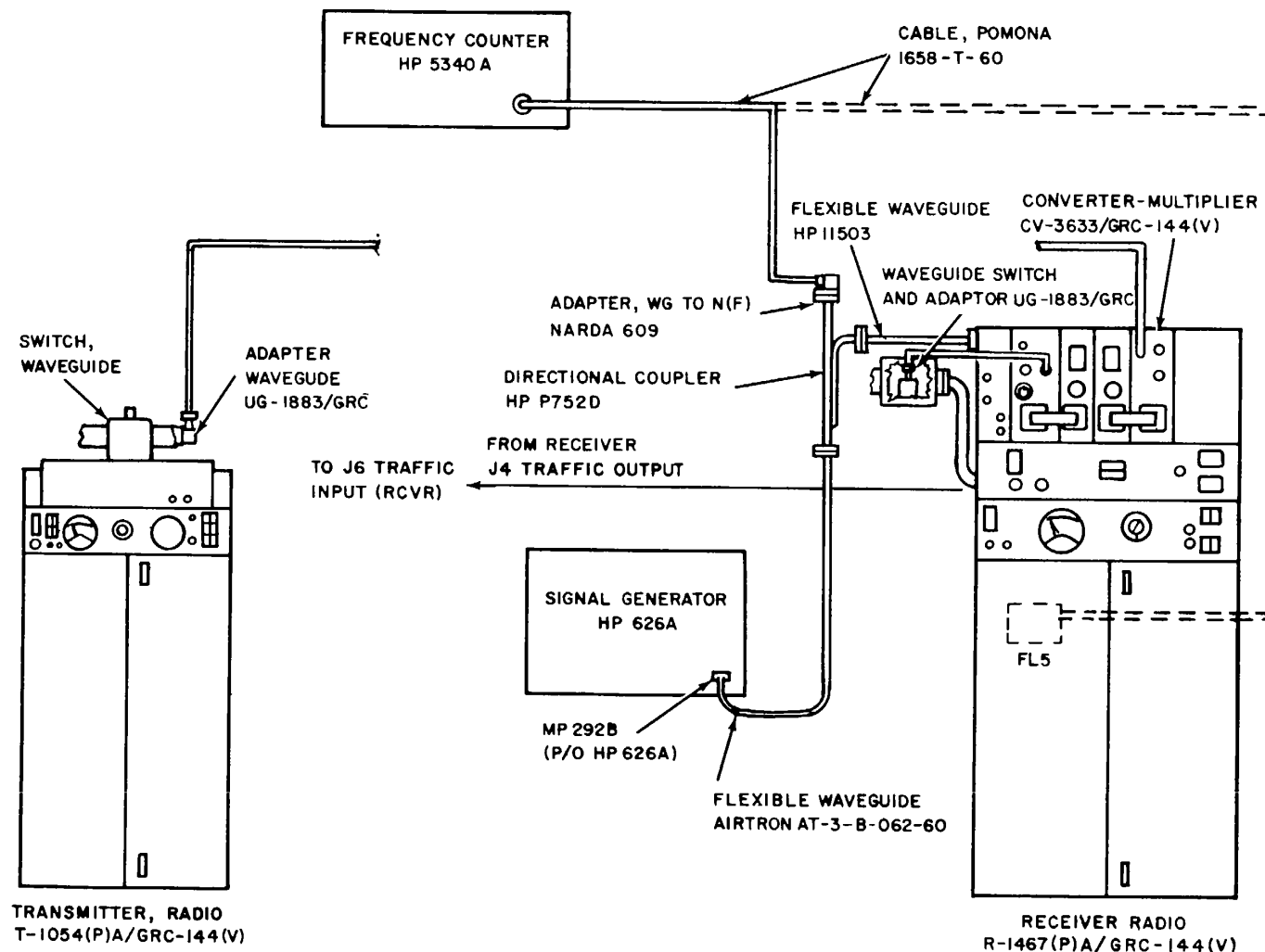


Figure 3-39. CV-3633/GRC-144(v) local oscillator frequency accuracy test setup.

Step		Control Setting		
No	Test Equipment	Equipment Under Test	Test Procedure	Performance Standard
4	Same as step 1.	N/A.	<p><u>a.</u> Remove the test lead (LO) from the mount in the R-1467(P)/GRC-144(V) SPECIAL TOOLS AND SPARE FUSES compartment.</p> <p><u>b.</u> Set the meter panel assembly 2A15A2 switch to the + TEST position.</p> <p><u>c.</u> Connect probe on one end of test meter lead to TEST LEAD jack on meter panel assembly 2A15A2 and connect probe on other end of test lead to the CV-3633/GRC-144(V) LO PWR test point.</p>	<p><u>a.</u> None.</p> <p><u>b.</u> None.</p> <p><u>c.</u> The test point indication should read 60 to 140</p>
5	N/A.	N/A.	<p>To calibrate the power threshold alarm, perform the following steps:</p> <p><u>a.</u> Using a small tuning-tool turn the CV-3633/GRC-144(V) LO PWR screwdriver adjustment control clockwise until the status panel ALARM SUMMARY indicator just lights red.</p> <p><u>b.</u> Turn the LO PWR screwdriver adjustment control counter-clockwise until the status panel ALARM SUMMARY indicator just changes from red to green; then continue adjustment one full turn counter-clockwise.</p>	None.

3-79. CV-3633/GRC-144(V) Receive Section Conversion Gain Test

a. Test Equipment and Materials.

- (1) Signal Generator, Hewlett Packard 626A.
- (2) Frequency Counter, Hewlett Packard 5340A.
- (3) Power Meter, Hewlett-Packard 432A.
- (4) Thermister Mount, Hewlett Packard P486A.
- (5) Thermister Mount, Hewlett Packard 478A.
- (6) Adapter SMA(M) to N(F) Narda 57.
- (7) Adapter Waveguide Coax N(F) Narda 609.
- (8) Directional Coupler, Hewlett-Packard P752D.
- (9) Test Cable, N(M) to N(M), Pamona 1658-T-60.
- (10) Waveguide, Flexible Waveguide HP 11503A

b. Test Connections and Conditions

**NOTE**

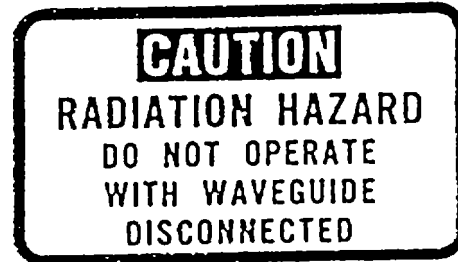
**To perform the CV-3633/GRC-144(V) receive section conversion gain test, the waveguide connection at 3AJ4 ANT waveguide flange must be open.**

- (1) Record the CV-3633/GRC-144(V) BP filters 3A3 and 3A4 dial settings.

**NOTE**

**Disregard status panel waveguide switch FREQUENCY BAND IN USE and transmitter WAVEGUIDE SW indicator alarms.**

- (2) Insure that transmit waveguide switch is set to the 15 GHz TEST (TO LOAD) position. For the AN/GRC-144(V)4 optional configuration, insure that Switch, Waveguide SA-1679/GRC is set to the TO LOAD (TEST) position.



- (3) Open waveguide connection at Converter-Multiplier CV-3633/GRC-144(V) ANT 34 output and first shelter waveguide connection by removing screws that secure Waveguide and the CV-3633/GRC-144(v) together.

- (4) Move the waveguide to a safe location.

**CAUTION**

Do not support test equipment by waveguides. Test equipment must be properly supported on a suitable equipment rack.

**NOTE:**

Locate the test equipment close to the CV-3633/GRC-144(V).

**NOTE**

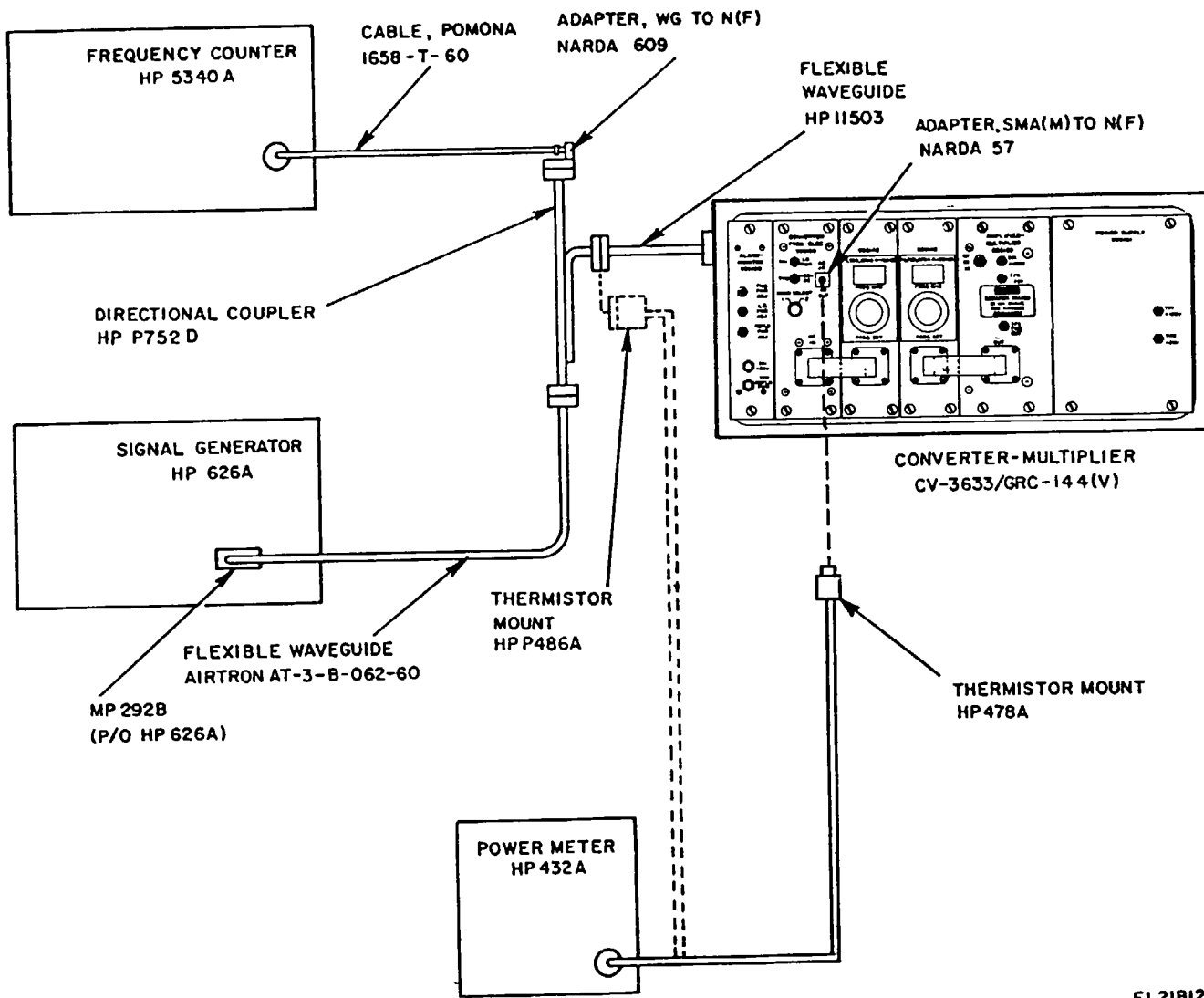
Connect power meter to directional coupler shown with dashed line.

- (5) Interconnect the test equipment in accordance with the test setup shown in figure 3-40.

c. Initial Test Equipment Calibration.

Turn on the test equipment and allow a 30 minute warmup period. Use the following technical manual procedure to calibrate the test equipment.

<u>Item</u>	<u>Technical Manual</u>
Signal Generator, HP 626A	TM 11-6625-2910-14
Frequency Counter, HP 5340	TM 11-6625-2808-14
Power Meter, HP 432A	TM 9-6625-2469-15



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Figure 3-40. CV-3633/GRC(v) receive section conversion gain test.



Step	Control Setting		
No	Test Equipment	Equipment Under Test	Test Procedure
1	SIGNAL GENERATOR HP 626A MODE SELECTOR: CW SYNC SELECTOR: INT FM OUTPUT ATTEN DBM: 0.0 FREQ DIAL: 14.4 GHz PWR: CCW FREQUENCY COUNTER HP 5340A RANGE: 250 MHz - 18 GHz RESOLUTION: 10 KHz POWER METER HP 432A MOUNT RESISTANCE: 100 ohms CALIBRATION FACTOR: Calibrate same as in paragraph 3-76d. step 1 RANGE 0 DBM	Converter-Multiplier CV-3633/GRC-144(V) BAND SET switch to position 1 Bandpass filter 3A3:14.4 GHz 3A4:14.8 GHz	
a.	Connect the HP 486A thermistor mount to the directional coupler coupled output. Adjust signal generator FREQ DIAL for 14.4 GHz on frequency counter and the PWR SET DIAL for -20.0 DBM on power meter.	a. N/A.	a. N/A.
			NOTE Do not adjust signal generator output level during performance of this test. NOTE Thermistor Mount Hewlett-Packard HP 478A is used to connect frequency converter 3A2 to
b.	Increase signal generator OUTPUT ATTEN DBM dial until it reads -10 DB. (-30 DBM input to converter). shown in figure 3-40.	b. N/A.	b. Disconnect power meter from directional coupler and connect power meter to 3A2AT2J2 RF OUT connector on electronic frequency converter 3A2 as
			b. None.

Step	Control Setting	Equipment Under Test	Test Procedure	Performance Standard
No	Test Equipment	Equipment Under Test	Test Procedure	Performance Standard
c.	Set power meter-MOUNT RE-SISTANCE switch to 200. CALIBRATION FACTOR: Calibrate same as in paragraph 3-76d step 1.	c. N/A.	c. Connect directional coupler to CV-3633/GRC-144(V) ANT 3AJ4 connector.	c. The CV-3633/GRC-144 receive section conversion shall be 5.5 minimum indicated by a -24.5 dBm minimum reading on the power meter. Same as step 1c.
2	Same as step 1, except: Set FREQ DIAL to 14.7 GHz.	N/A.	N/A.	Same as step 1c.
3	Same as step 1, except: Set FREQ DIAL to 15.0 GHz.	N/A.	N/A..	Same as step 1c.

## CHAPTER 4

## DEPOT MAINTENANCE

## Section I. REPAIRS

## 4-1. General

a. Depot maintenance repair procedures, which supplement repair data in chapter 3, are provided in this section. Depot repair consists primarily of removal and replacement procedures for defective subassemblies or piece parts. Most subassemblies and piece parts are readily accessible and are easily replaced. Repair instructions, therefore, are supplied only for those assemblies requiring special techniques or a sequence of steps which are not readily obvious.

b. Special instructions for particular assemblies of Transmitter, Radio T-1054(P)/GRC-144() and T-1054(P)A/GRC-144 are covered in paragraphs 4-4 through 4-9; particular assemblies of Receiver, Radio R-1467(P)/GRC-144() and R-1467(P)A/GRC-144 are covered in paragraphs 4-10 and 4-11. Special instructions for particular assemblies of Converter-Multiplier CV-3633/GRC-144(V) are covered in paragraphs 4-11.1 through 4-11.4.

c. Throughout equipment repair, reference should be made to wiring diagram and parts location illustrations. Illustrations supplied in this chapter supplement those located in chapters 3 and 5, and those contained in TM 115820-695-12. Wiring diagrams and parts location diagrams for Transmitter, Radio T-1054(P)/GRC-144() and T-1054(P)A/GRC-144 are provided in figures 4-6 through 4-35 and 5-59 through 5-89; illustrations for Receiver, Radio R-1467(P)/GRC-144(V) and R-1467(P)A/GRC-144 are provided in figures 4-36 through 4-46 and 5-90 through 5-97. The wiring diagram for Indicator, Antenna Alignment ID-1708 GRC is provided in figure 4-47. Parts location diagrams for Converter-Multiplier CV3633/GRC-144(V) are provided in figures 5-108 through 5-118.

## 4-2. General Parts Replacement Techniques

a. General instructions on parts replacement for direct support maintenance must also be observed during depot maintenance activity. Refer to paragraph 3-19 for general parts replacement techniques.

b. If conformal coating on printed wiring boards is removed during maintenance, recoat the printed wiring boards following the instructions provided in paragraph 4-13.

## 4-3. Equipment Required

Tools and materials required to perform the depot repairs given in this section are listed below:

- a. Tool pit, Radio Repair TK-100/G, FSN 6180-0-79.
- b. Tool Kit, Electronic Equipment TK-105/G, FSN 5180-610-8177.
- c. Crimping tool MS 3191-4 with head assembly W25, FSN 5120-230-771.
- d. Extraction tool MS 18278, Size 20, FSN 5120-230-3770.
- e. Extraction tool CET-C6B, FSN 5120-963-7661.

## 4-4. Repair of Transmitter Frequency Mixer Stage 1A9 (fig. 6-71)

Transmitter frequency mixer stage 1A9 contains coaxial circulator 1A9HYI, replaceable at direct support level (para 3-26) and is nonrepairable, and crystal mixer 1A9A1, replaceable at organizational maintenance level (TM 11-5820-695-12).

For depot repair of crystal mixer 1A9A1, specific instructions are provided for the replacement of crystal diode 1A9A1CR1. Instructions for the removal and replacement of crystal diode 1A9A1CR1 are provided in a and b below.

**CAUTION**

**Before handling crystal diode 1A9A1CR1, ground yourself to equipment case ground in order to dissipate any static charge.**

a, Removal of Crystal Diode 1A9A1CR1 (fig. 5-71).

(1) Remove 1A9A1 from case of 1A9 and remove the four screws securing connector 1A9A1J2 to crystal

mixer 1A9A1. Pull connector 1A9A1J2 out of crystal mixer 1A9A1.

(2) Using long nose pliers, extract crystal diode 1A9A1CRL from connector 1A9A1J2.

b. *Replacement of Crystal Diode 1A9A1CR1.*

**NOTE**

Check choke solder connections on connector 1A9AIJ2 for signs of cracks or looseness. If there is any sign of cracks or looseness, Resolder connections

(1) Observe diode orientation when replacing the crystal diode 1A9A1CR1. The correct diode orientation is shown in figure 5-71 and stamped on the cover of the 1A9A1 assembly. Coat the cathode of diode 1A9A1CR1 with Dow Corning No. 340 heat sink compound and insert the anode end into diode holder on connector 1A9A1J2.

(2) Insert 1A9A1J2, with 1A9A1CR1, into cavity 1A9A1Z1, being certain that the cathode of 1A9A1CR1 is seated properly within 1A9A1Z1 and that the choke is installed in the upward position.

(3) Secure connector 1A9A1J2 in place with the four screws removed in a(l) above and replace 1A9A1 in 1A9 case.

**4-5. Repair of Transmitter Frequency Multiplier Group IA10 (fig. 41 and 5-72)**

Transmitter 2nd stage frequency multiplier 1A10A1 and transmitter 3rd stage frequency multiplier 1A10A2 are replaced at the organizational maintenance level (TM 11-5820-695-12). Coaxial circulator 1A10HY1 is replaced at the direct support maintenance level (para 3-27). Depot repair of these assemblies consists of replacing defective piece parts. Precautionary measures should be observed in replacement of varactor diodes 1A10A1CR1 and 1A10A2CR1. Removal and replacement procedures for 1A10A1CR1 and 1A10A2CR1 are provided below.

a. *Removal and Replacement of Varactor Diode 1A10A1CR1.* To replace varactor diode 1A10A1CR1 proceed as follows:

(1) Loosen the 10 screws and washers securing cover on transmitter 2nd stage frequency multiplier 1A10A1 and remove cover (fig. 5-72).

(2) Rotate tuning plunger and adjustment screw for cavity 1A10A1Z1C counterclockwise to pull tuning plunger (C, fig. 4-1) into contact plunger. Continue until tuning plunger is inside contact plunger.

(3) It should be noted that as step (2) was performed, a spring within the sleeve pushed out on the coupling and kept the cup in contact with TM 11-5820-695-35 the tuning plunger. The end of the spring is now out well beyond the end of the sleeve and is flexible Lift the coupling and cup (as a unit) off end of spring. Do not

separate the coupling and cup; there are three small nylon spacers between them which must not be lost.

(4) Remove the spring from the sleeve. Rotate the sleeve one turn clockwise, as viewed from cavity 1A10A1Z1C.

(5) Remove the hex-nut securing the contact plunger in cavity 1A10A1Z1C. Unscrew the contact plunger and remove it from cavity 1A10A1Z1C.

(6) Remove the setscrew from access hole in outside wall of cavity 1A10A1Z1C.

(7) Insert a small screwdriver through the access hole (step (6)) and unscrew the nut securing coupling disc and washer (B, fig. 4-1) to capacitor 1A10A1C3 assembly. Remove the nut, coupling disc, washer, diode holder strap, and varactor diode 1A10A1CR1.

(8) Apply a small amount of heat sink compound Dow Corning No. 340 to the cathode of replacement varactor diode 1A10A1CR1 (see fig.4-1 to determine varactor diode orientation) and insert the cathode end of varactor diode 1A10A1CR1 into seat in wall of cavity 1A10A1Z1C.

(9) Replace diode holder strap, washer, coupling disc and tighten nut on shaft of capacitor 1A10A1C3 assembly.

(10) Replace contact plunger in cavity 1A10A1Z1C. Be sure it is screwed all the way in, then secure it in place with the hex nut removed in (5) above. Tighten hex-nut firmly.

(11) Rotate sleeve (step (4) above) one turn counterclockwise.

(12) Insert spring into sleeve, then insert cup and coupling over spring and replace coupling over the spring.

(13) Replace setscrew, removed in step (6), in the access hole. Check that setscrew is flush with inside surface of cavity wall and does not extend into cavity 1A10A1Z1C.

(14) Replace cover and secure with the 10 screws and washers removed in step (1) above.

b. *Removal and Replacement of Varactor Diode 1A10A2CR1.*

(1) Hold transmitter 3rd stage frequency multiplier 1A10A2 in the vertical position with connector 1A10A2J1 facing up and unscrew diode holder (center screw, fig. 4-2) approximately three complete turns.

(2) Unscrew plunger and pull plunger, diode holder, and varactor diode 1A10A2CR1 out of the cavity. (If necessary, use tweezers to extract 1A10A2CR1 from seat in crossbar.)

(3) Coat cathode of new varactor diode with heat sink compound Dow Corning No. 340 and install cathode end of varactor diode 1A10A2CR1 into diode holder (fig. 4-2).

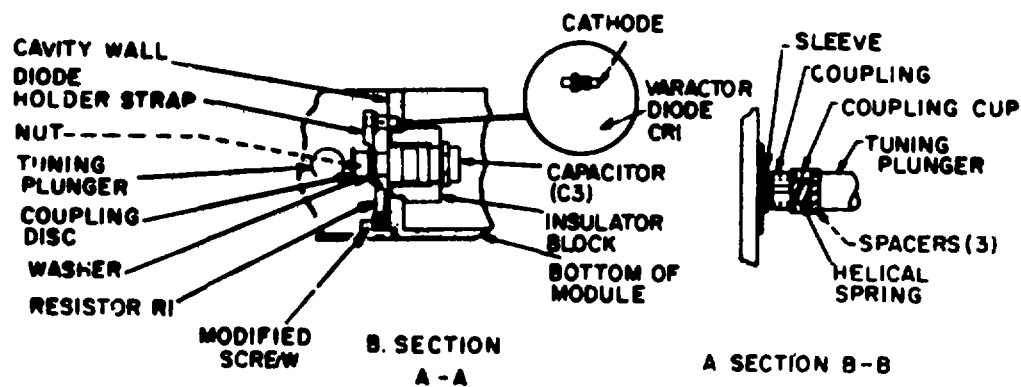
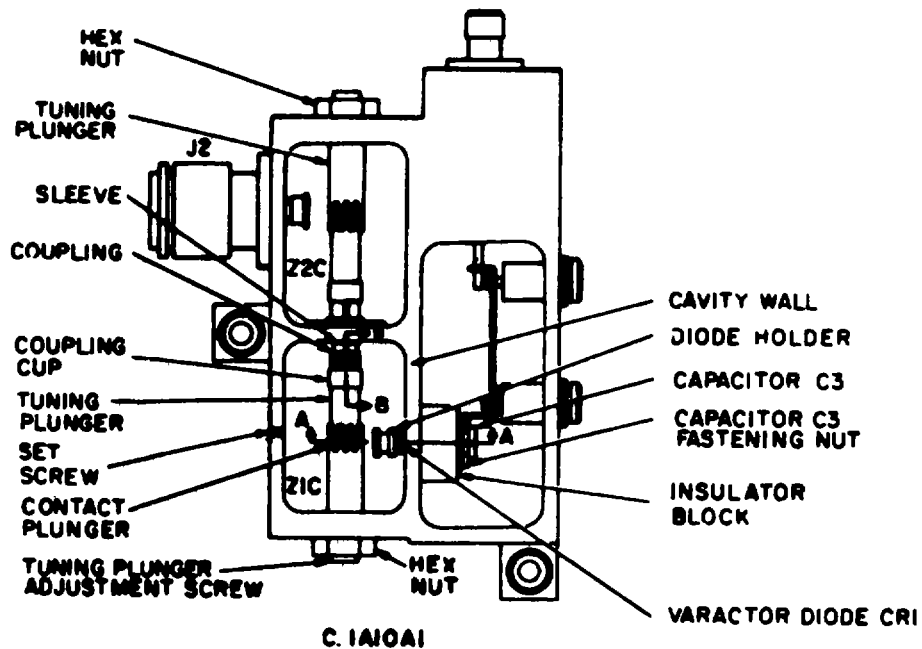
(4) Hold transmitter 3rd stage frequency multiplier 1A10A2 in the vertical position and screw the assembly (comprised of varactor diode 1A10A2CR1, diode holder, and plunger) into the cavity until plunger bottoms; then, screw in the diode holder until 1A10A2CR1 gently, but firmly, bottoms into position.

**4-6 Repair of Transmitter Amplifier-Frequency Multiplier 1A11 (fig. 4-3 and 5-74)**

Depot repair of transmitter amplifier, frequency multiplier 1A11 consists of defective piece part replacement. Particular instructions for varactor diode 1A11CR3 replacement are provided below.

*a. Removal of Varactor Diode 1A11CR3.*

(1) Remove the 26 screws and washers securing top cover on transmitter amplifier-frequency multiplier 1A11 and remove the cover (fig. 5-74).



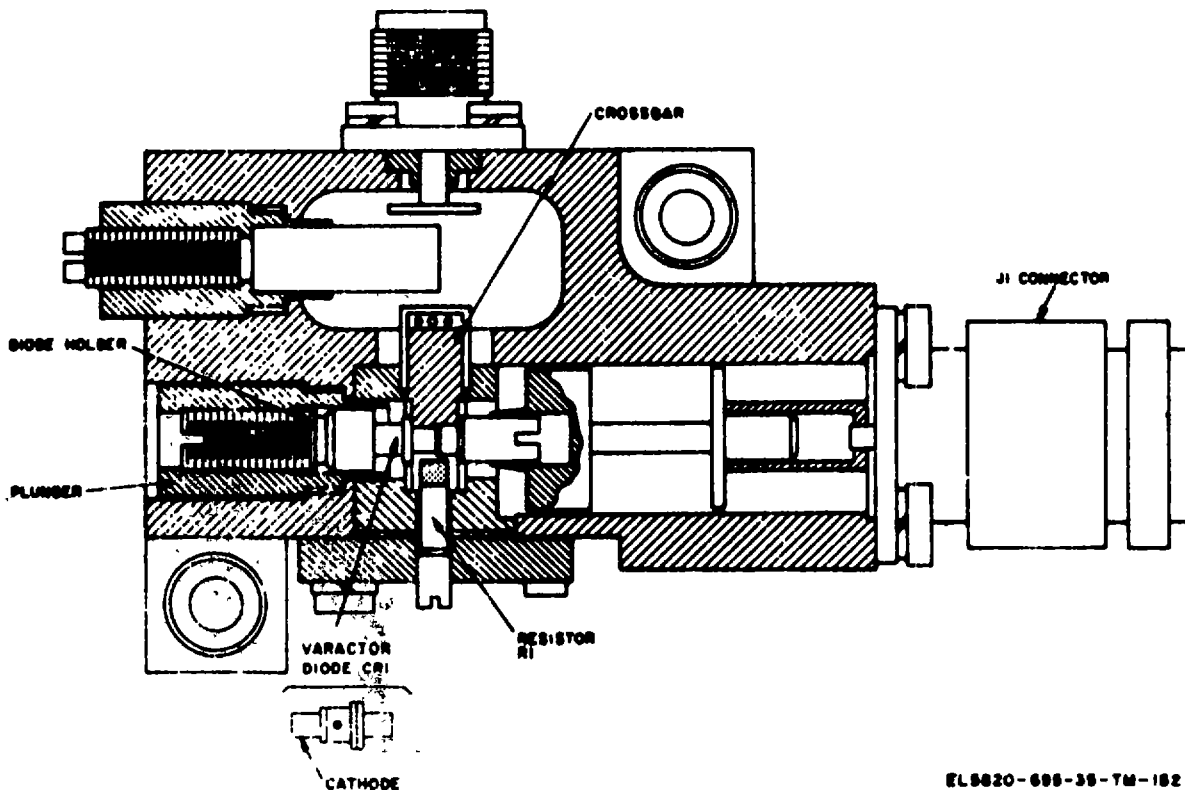


Figure 4-2. Transmitter 3rd stage frequency multiplier 1A10A2, varactor diode replacement.

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(2) Remove the 18 screws and washers securing heat sink on transmitter amplifier-frequency multiplier 1A11 and remove the heat sink.

(3) Remove mounting nuts and lockwashers from capacitors 1A11C35 and 1A11C37. Lift terminal lug for resistor 1A11R22 off 1A11C35. washer from capacitor 1A11C37 (fig. 5-74).

(4) Remove rigid cable 1A11W5 connected between connector 1A11J4 and 1A11J6 (B, fig. 5-74).

(5) Remove hex nut and spring lockwasher at opposite end of varactor diode 1A11CR3 (fig.4-3). Remove inductor 1A11L26 (meter bar) along with 1A11CR3 soldered to it.

(6) Unsolder varactor diode 1A11CR3 from 1A11L26 and discard 1A11CR3. Remove excess solder from 1A11L26.

*b. Replacement of Varactor Diode 1A11CR3.*

(1) Install new varactor diode 1A11CR3 in place by fastening it securely to the chassis with hex-nut and spring lockwasher removed in step a(5).

(2) Replace rigid cable 1A11W5 removed in step a(4) above.

(3) Replace inductor 1A11L26 and terminal lug for resistor 1A11R22. Replace nuts, flat washers, and lockwashers (removed in step a(3) above) on capacitors 1A11C35 and 1A11C37. Do not tighten the nuts.

(4) Spacing between 1A11L26 and 1A11L27 must be adjusted to  $0.060 \pm 0.003$  inch; spacing between 1A11L26 and 1A11L25 must be adjusted to  $0.090 + 0.003$  inch. In each case edges of inductors must be parallel within 0.002 inch. Secure 1A11L26 in place by tightening nuts on 1A11C35 and 1A11C37.

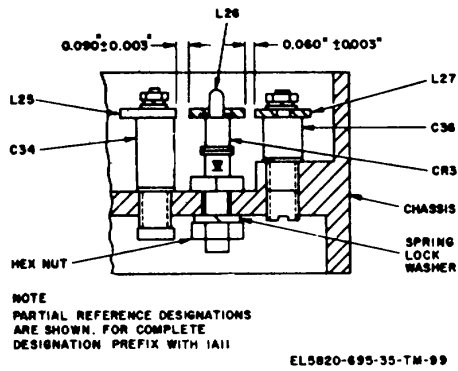
(5) Solder diode 1A11CR3 to inductor 1A11L26.

(6) Replace and secure top cover on transmitter amplifier-frequency multiplier 1A11 using the 26 screws and washers removed in a(1) above. Start with screws in center and work outward, Tighten screws to torque of 40-50 inch ounces.

(7) Replace and secure heat sink to 1A11 using the 18 screws and washers removed in a(2) above.

**4-7. Repair of Digital Data Modem 1A12**

a. General. Digital data modem 1A12 contains 11 plug-in components replaceable at the organizational maintenance level (TM 11-5820-695-12) and digital



**Figure 4-3. Transmitter amplifier-frequency multiplier 1A11, varactor diode replacement.**

data modem chassis 1A12A12 replaceable at the direct support level (para 3-29). Digital data modem 1A12 depot repair entails parts replacement on plug-in components 1A12A2 through 1A12A10 and on digital data modem chassis 1A12A12. Location of parts on the plug in components is shown in figures 5-75 through 5-83. No special instructions are required for parts replacement. Digital data modem chassis 1A12A12 parts location is provided in figures 4-15 through 4-19. Disassembly of digital data modem chassis 1A12A12 is described in b below.

**b. Disassembly of Digital Data Modem Chassis 1A12A12.**

(1) Remove the four screws securing the rear cover to digital data modem chassis 1A12A12 and remove the rear cover.

(2) Remove the two screws located between jack pair, 1A12A12A1J1 and 1A12A12A1J2, and 1A12A12A2J3 and 1A12A12A2J4.

(3) Turn digital data modem chassis 1A12A12 upside down and remove the two screws on outside of chassis case.

(4) On the plug-in component connector rack, remove the four screws securing digital data modem chassis 1A12A12 to the chassis case.

(5) Slide digital data modem chassis 1A12A12 out the back end of the chassis case, thereby allowing access to all parts.

**c. Reassembly of Digital Data Modem Chassis 1A12A12.**

(1) Slide digital data modem chassis 1A12A12 into the chassis case.

(2) Replace and tighten the four screws removed in b(4) which secure digital data modem chassis 1A12A12 to the chassis case.

(3) Replace and tighten the two screws removed in step b(2) above.

(5) If a connector (1A12A12XA2 through 1A12A12XA13) has been replaced, use the plug-in component that mates with the connector as a gauge in aligning the replacement connector as follows:

(a) Loosen the two screws securing the replacement connector to the connector rack.

(b) Insert the mating plug-in component into the guide rails for the replacement connector and slowly slide it back until firmly seated in the replacement connector. Tighten the two screws securing the connector to the connector rack. Remove the plug-in component used for connector alignment.

(c) Repeat steps (5)(a) and (b) for each of the replacement connectors (1A12A12XA2 through 1A12A12XA10).

(6) Insert the rear cover back on digital data modem chassis 1A12A12 and secure with the four screws removed in step b(1) above.

**4-8. Repair of Orderwire Assembly 1A13**

Orderwire assembly 1A13 contains five plug-in daughter board assemblies 1A13A1 through 1A13A5 replaceable at organizational level and an orderwire chassis (1A113A7) replaceable at the direct support level (para 3-30). Depot repair of these assemblies is piece part replacement. Parts location for daughter board assemblies 1A13A1 through 1A13A5 is provided in figures 584 through 5-89. Parts location for orderwire chassis 1A13A7 is shown in figures 4-20 and 4-21. No special instructions are required for depot level disassembly and piece part replacement.

**4-9. Repair of Electrical Frequency**

Synthesizer 1A14 and 2A14 With the exception of reference designators, electrical frequency synthesizer 1A14 in T-1054/RC-144 is identical to electrical frequency synthesizer 2A14 in R-1467/GRC-144. Electrical frequency synthesizer 1A14 contains six repairable plug-in components (1A14A1 through 1A14A6) and two nonrepairable plug-in components (1A14A7 and 1A14A8) all replaceable at the organizational level. The electrical equipment chassis 1A14A10 with printed wiring board assembly 1A14A9 is replaceable at the direct support level (para 3-31). With the exception of the two nonrepairable plug-in components, depot repair of these



pair of these assemblies is piece part replacement. Parts location and wiring diagrams for plug-in components 1A14A1 through 1A14A6 are shown in figures 4-24 through 4-35. Electrical parts location on electrical equipment chassis 1A14A10 and printed wiring board 1A14A9 is shown in figures 4-22 and 4-23. No special instructions are required for depot level disassembly and piece part replacement.

**4-10. Repair of Amplifier-Mixer 2A7**

Depot repairs to amplifier-mixer 2A7 (fig. 4-41) consists of replacement of defective parts. Special consideration must be given to the replacement of matched pair crystal diodes 2A7ZICR1 and 2A7Z1CR2 as indicated below.

**CAUTION**

**Before handling crystal diodes, ground yourself to equipment case ground to dissipate any existing static charge.**

*a. Removal of Crystal Diode 2A7ZICR1 or 2A7Z1CR2.*

(1) Using a screwdriver, unscrew and remove the diode cover screw covering the defective crystal diode.

(2) Using long nose pliers, grasp the diode's base and extract it from amplifier-mixer 2A7.

(3) Pull diode from diode base.

*b. Replacement of Crystal Diode 2A7Z1CR1 or 2A7Z1CR2.*

(1) Note cathode orientation when replacing the crystal diode. Orient the replacement crystal diode in accordance with the polarity shown in figure 4-41 and stamped on the assembly and insert crystal diode into the diode base, insuring positive seating.

(2) Insert diode (with base) into amplifier mixer 2A7.

(3) Replace and firmly secure diode cover screw.

**4-11. Repair of Amplifier-Frequency Multiplier 2A10**

Amplifier-frequency multiplier 2A10 (fig. 6-95) depot repair is the replacement of defective part. Special instructions for removal and replacement of varactor diode 2A10CR3 are provided below.

*a. Removal of Varactor Diode 2A10CR3.*

(1) Remove the 18 screws securing the top cover on amplifier-frequency multiplier 2A10 and remove the cover (fig. 5-95).

(2) Remove the 11 screws securing the bottom cover on amplifier-frequency multiplier 2A10 and remove the cover.

(3) Remove the screw, lockwasher, and locking lever (fig. 4-4) for diode 2A10CR3, on the bottom side of chassis.

(4) Unscrew diode 2A10CR3; remove and discard it. Retain the spring tension washer.

*b. Replacement of Varactor Diode 2A10CR3.*

(1) Screw in the replacement varactor diode noting when the spring tension washer comes into contact with surface of inductor 2A101A14. Continue rotation of the diode only one-half turn beyond this point.

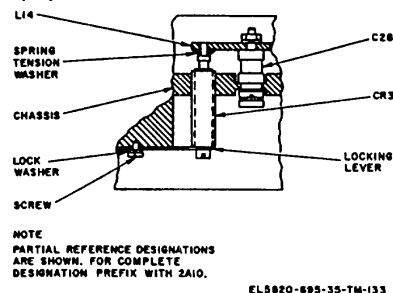
(2) Replace the locking lever, lockwashers and nut removed in step a(3).

(3) Replace bottom cover on amplifier-frequency multiplier 2A10 and secure with the 11 screws moved in a(2).

(4) Replace top cover on 2A10 and secure in place using the 18 screws removed in a(1). Start with screws in center and work outward. Tighten screws to torque of 40-50 inch-ounces.

**4-11.1. Converter-Multiplier CV-3633/GRC-144(V), Unit 3**

Converter-Multiplier CV-3633/GRC-144(V) contains five plug-in assemblies 3A1, 3A2, 3A5, 3A6 and 3A8 that are replaceable at the organizational level and four assemblies 3A3, 3A4, 3ACR1 and 3A7HY1 that are replaceable at the direct support level (para 3-53.3 through 3-53.6). Depot repair of the CV-3633/GRC-144(V) consists of piece part and component replacement. Parts location illustrations of the CV-3633/GRC-144(V) are shown in figures 5-108 through 5-118. There are no special instructions required for depot level disassembly and piece part replacement for the alarm-monitor 3A1, power supply 3A6, electrical equipment chassis 3A7 and



**Figure 4-4. Amplifier frequency multiplier 2A10 varactor diode replacement.**

status panel 3A8. Bandpass filters 3A3 and 3A4 are nonrepairable assemblies that are replaced at the direct support maintenance level (para 3-53.5).

#### 4-11.2. Alarm-Monitor 3A1

To gain access to alarm-monitor 3A1 printed wiring board assembly (fig. 5108) components remove four panhead screws at rear of frame and slide covers toward rear exposing wiring board assembly.

#### 4-11.3. Electronic Frequency Converter 3A2

Depot repair of electronic frequency converter consists of replacement of defective parts. Exercise care when removing or replacing rigid coaxial cables. Detail procedures are provided in TM 11-5820-695-12 for removal and replacement of rigid coaxial cables.

a. Removal. To replace components in the electronic frequency converter 3A2 proceed as follows:

(1) Remove two panhead screws at rear of chassis and slide cover toward rear exposing electronics frequency converter components.

(2) If required remove rigid coaxial cables from component to be replaced.

(3) If required remove connector plug and attaching hardware from component to be replaced.

#### NOTE

**The coaxial mixer 3A2A2 must be removed prior to or along with isolator 3A2AT2. To remove the isolator 3A2AT2 perform step (4). To remove tunnel diode amplifier 3A2A1 perform step (5).**

(4) Remove rigid coaxial cables from coaxial mixer 3A2A2 and remove two panhead machine screws

at front panel located adjacent to RF OUT J2 connector. Remove two nuts screws and nuts that secure the coaxial mixer to the chassis and remove the coaxial mixer and isolator together.

(5) Remove rigid coaxial cable and connector plug from tunnel diode amplifier 3A2A1. Remove two panhead machine screws at front panel located adjacent to top portion of RF IN Waveguide flange and four panhead machine screws and flat washers located at bottom of electronic frequency converter chassis and remove tunnel diode amplifier.

b. Replacement. Replacement consist of-following the reverse order of removal instructions.

#### 4-11.4. Amplifier-Multiplier 3A5

Depot repairs to amplifier-multiplier 3A5 consist of replacement of defective parts. Exercise care when removing or replacing rigid coaxial cables. Detail procedures are provided in TM 11-5820695-12 for removal and replacement of rigid coaxial cables.

a. Removal. To replace components in the amplifier-multiplier 3A5 (fig. 5110) proceed as follows:

(1) Remove two panhead screws at rear of chassis and slide cover toward rear exposing amplifier-multiplier components.

(2) Remove screws and hardware that secure current regulator 3A5A8 to post and chassis frame.

(3) If replacement of current regulator 3ASA8 is required carefully tag then unsolder leads connected to current regulator. If access to a component under current regulator is required carefully move current regulator aside so that wires are not damaged when removing component.

(4) Remove suspect defective component from chassis frame using care not to damage rigid coaxial cables.

b. Replacement. Replacement consists of following the reverse order of removal instructions.

#### **4-12. Repair and Replacement of Connectors**

*a. General.* Connector repair consists of the replacement of the defective connector (solder type nonremovable contacts) or the replacement of the

defective connector contacts (crimp or solder type removable contacts). Connectors on assemblies to be repaired at depot level are identified in b (Transmitter, Radio T-1054(P)/GRC-144(V), and T-1054(P)A/GRC-144) c (Receiver, Radio R-1467(P)/GRC-144(V) and R-1467/GRC-144) and d (Converter-Multiplier CV-3633/GRC144(V) below. Also listed are applicable tools and a reference to the paragraphs which detail the required repair procedures.

**Change 6 4-6.2**

b. Transmitter, Radio T-1054(P)/GRC-144(V) and T-1054(P)A/GRC-144(V) Component Connectors.

Connector	Extraction/ insertion tool	Crimping tool	Procedure paragraph	Figure reference
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**NOTE**

The connectors listed below identified with an asterisk are not part of Transmitter, Radio T-1054(P)A/GRC-144.

1A2P3	MSI8278,size20/none	MS3191-4withhead	3-37c assyW25	5-63
1A3PI	Same	Same	3-37c	5-64, 5-64.1 and 5-64.2
1A4P1	Same	Same	3-37c	4-11
1A5P1	Same	Same	3-37c	5-66
1A7P1	Same	Same	3-37c	5-68
1A8P3	Same	Same	3-37c	5-70 and 5-70.
IAIIP1	Same	Same	3-37c	5-74
*1A12A12AIP1	Same	Same	3-37c	4-16
*1A12A12A2P2	Same	Same	3-37c	4-17
1A13A7P2	Same	Same	3-37c	4-20
1A14A9XA4J1	Same	Same	3-37c	4-22
1A14A9XA5J1	Same	Same	3-37c	4-22
1A14A9XA6J1	Same	Same	3-37c	4-22
1A5P2	CET-C6B/none	None	3-37d	5-66
1A13A7P1	Same	None	3-37d	4-20
1AI4PI	Same	None	3-37d	4-23
1A14A9XAIJ1	Same	None	3-37d	4-22
1A14A9XA2J1	Same	None	3-37d	4-22
1A14A9XA3J1	Same	None	3-37d	4-22
*1A12A12AXA1	None	None	3-37f	4-16
*1A12A12A2XAll	None	None	3-37f	4-17
*1A12AI2XA3	None	None	3-37f	4-15
1A12A12XA10	through			
1AI3A7XA1	None	None	3-37f	4-20
1A13A7XA5	through			
1A14XA7	None	None	3-37f	4-22

**NOTE**

The connectors listed below pertain to the T-1054 (P)A/GRC-144 only.

1A12A1	MS18278, size 20/none	MS3191-4 with head assy W25	3-37c	5-83.1
1A12P2	Same	Same	3-37c	5-83.1
1A12J1	Same	Same	3-37c	5-83.1
1A12J2	Same	Same	3-37c	5-83.1
1A12XA1	None	None	3-37f	5-83.1
through 1A12XA8				

c. Receiver, Radio R-1467(P)/GRC-144(V) and R-1467(P)A/GRC-144(V)) Component Connectors.

Connector	Extraction/ insertion tool	Crimping tool	Procedure paragraph	Figure reference
2A4P1	MS18278,size20/none	MS3191-4 with head assyW25	3-37c	5-90 (1) and 5-90.1
2A5P3	Same	Same	3-37c	5-92 (1)
2A7P1	Same	Same	3-37c	4-41 (1)
2A8P5	Same	Same	3-37c	4-44
2A10P1	Same	Same	3-37c	5-95
2A11P1	Same	Same	3-37c	4-11 (1)
2A12P1	Same	Same	3-37c	5-66 (1)
2A13P1	Same	Same	3-37c	5-97
2A14A9XA4J1	MS18278,size20/none	MS3191-4with'head assyW25	3-37c	4-22
2A14A9XA5J1	Same	Same	3-37c	4-22
2A14A9XA5J1	Same	Same	3-37c	4-22
2A12P2	CET-C6B/none	None	3-37d	5-66 (1)
2A14P1	Same	None	3-37d	4-23
2A14A9XAIJ1	Same	None	3-37d	4-22
2A14A9XA2J1	Same	None	3-37d	4-22
2A14A9XA3J1	Same	None	3-37d	4-22
2A2J3	None	None	3-37f	
2A14XA7	None	None	3-37f	4-22

d. CV-3633/GRC-144(V) Connector Chart.

Connector	Extraction/ insertion tool	Crimping tool	Procedure paragraph	Figure reference
3A7P1	MS24256 R20/A20	MS3191-4 with head assy W1	3-37e	5-107
3A7P3	Same	Same	3-37e	5-107
3A7J1	Same	Same	3-37e	5-107
3A7J2	Same	Same	3-37e	5-107
3A7J3	Same	Same	3-37e	5-107
3A7P2	MS18278 Size 20/ None	MS3191-4 with head assy W25	3-37c	5-107
3A7P4	Same	Same	3-37c	5-107
3A7XA1	Same	Same	3-37c	5-107
3A7XA2	Same	Same	3-37c	5-107
3A7XA5	Same	Same	3-37c	5-107
3A7XA6A	Same	Same	3-37c	5-107
3A7XA6B	Same	Same	3-37c	5-107

**4-13. Repair of Conformal Coating**

The following procedure describes the process and material requirements to apply a flexible polyurethane (PUR) coating to printed wiring boards.

a. *Printed Wiring Board Preparation.*

(1) Using medium grade sandpaper, remove all sharp edges and ridges from the repaired area on the board.

(2) Assemble parts on the printed wiring board making certain that all leads are bent and cut short. Solder parts installed on board.

**WARNING**

**All cleaning operations must be done under a hood which is ventilated to the outside. Protective clothing, rubber gloves and eye protection must be worn. Avoid breathing the vapors and avoid skin contact with resin or catalyst.**

(3) Using a medium stiff nylon brush clean the repaired area on the printed wiring board using Freon TMC solution. Remove all extraneous materials such as solder flux, dust, dirt, or fingerprints.

(4) Using a forced drying method, remove all traces of solvent or moisture.

(5) Place repaired board under an ultraviolet light and verify that all dirt or other foreign matter has been removed.

(6) Vacuum bake the printed wiring board at a temperature of 180° F. for four hours.

(7) After baking mask all areas of the printed wiring board which do not require conformal coating.

(8) Vacuum clean the printed wiring board immediately prior to conformal coating application (c below).

*b. Conformal Coating Preparation.* To insure that the characteristics of a minimum weight of 100 grams of polyurethane is maintained during preparation of the coating mixture, preparations should be maintained in accordance with the following chart.

Polyurethane type	Mfr.	Components	Pot life	Parts by weight
PUR	Hysol Corp. PC-26M	Part A	1 1/2 Hrs.	100
		Part B	-----	36
	PC-29M	Part A	6 Hrs. -----	100
		Part B	-----	60
	Conap Inc.	Part A	6 Hrs. -----	100
		Part B	-----	70
	Essex Chemical	Part A	8 Hrs. -----	100
		Part B	-----	39

**Notes**

1. Polyurethane (Part A) must be stored at the temperature specified by the manufacturer. The material should be free of any film, cloudiness, crystals, or lumps. If the material exhibits any evidence of deterioration, it should be discarded.

2. Catalyst (Part B) must be stored at the temperature specified by the manufacturer. If the material exhibits any evidence of deterioration, it should be discarded.

(1) Pot life is the usable time of the mixture during which viscosity still allow application to the printed wiring board.

(2) Weight the larger quantity, Part A first, and then add Part B, using a tongue depressor, thoroughly mix part B into part A.

(3) Place coating solution on a clean air bench and using a stir-master, stir for 16 minutes; then, allow 16 minutes for solvent gal to leave the solution.

c. Conformal Coating Application, Circuit Side.

(1) Coating may be applied by brushing or spraying. If the spraying method is used, a Zicon Corp. closed system or equivalent should be used.

**NOTE**

**The Zicon Corporation equipment permits spraying of solventless 100% solid materials. The coating is atomized by a superheated solvent under high about .003 to .050 inches to be applied by continuous spraying.**

**WARNING**

**All spraying operations must be performed in a well ventilated area.**

(2) Place board on a clean surface with circuit side up.

(3) Application of the coating requires that the applier have some degree of skill to assure that a thorough coverage and uniformity of the coating is maintained.

(4) Two or three successive layers of coating may be required to minimize the possibility of pinholes (which could provide a path for ingress of moisture).

**NOTE**

**To maintain a constant level of the thickness at all times, viscosity of the coating must be monitored and closely maintained by gradual addition of solvents.**

(5) Check the thickness of the coating using a wet gage. A total buildup of .006 to .0025 inches is adequate.

(6) Place board (coated side up) on a clean air bench for a period of 2 hours thereby insuring that all thinning solvents have been vaporized and carried off.

*d. Coating Cure, Circuit Side.*

(1) Place board into an air circulating oven with the coating side up.

(2) Follow the baking and curing time periods for the various materials as indicated in the chart below.

<i>Mfr.</i>	<i>Baking time</i>	<i>Curing time</i>
Hysol Corp.	4 hrs. at 148° F	Same, plus 2 days at room temp.
PC-26M PC-29M	3 hrs. At 150° F	Same, plus 2 days at room temp.
CONAP Inc.	3 hrs. At 138° F	Same, plus 2 days at room temp.
Essex Chemical	3 hrs. At 150° F	Same, plus 2 days at room temp.

*e. Conformal Coating Application, Component Side.*  
Follow steps described under c above, to coat

component side. Follow the curing time periods for materials used in accordance with the chart in *d* above.

**Section II. TESTING PROCEDURES**

**4-14. General**

Testing is limited to verifying the quality of rigid coaxial cables used in Transmitter, Radio T1054/GRC-144 and Receiver, Radio R-1467/ GRC-144.

**4-15. Equipment Required**

Equipment required for testing is listed below.

- a. Time Domain Reflectometer Plug-in HP1415A.
- b. Oscilloscope HP-140A.
- c. Calibrated Mismatch 1.10 VSWR Mecca Model 400-1.10.
- d. Adapter GR874-TO-Type N General Radio 874 GNP.
- e. 60 ohm Termination, HP908A.
- f. Elbow Adapter General Radio GR874 (two required).
- g. Adapter, GR874B-to-SMJ OMNI Spectra 21210.
- h. Adapter, UG-29B/U N female-o-N female.

**4-16. Coaxial Cable Test**

a. Coaxial cable assemblies are tested using Oscilloscope HP-140A with Time Domain Reflectometer Plug-in HP-441&A. The reflectometer incorporates a step generator which produces a positive-going incident wave which is fed into the coaxial cable undergoing test. The incident and reflected waveforms are then analyzed to determine if there is a mismatch or if there are any discontinuities along the cable.

b. The oscilloscope high impedance input bridges the cable at its junction with the reflectometer step

generator (via the elbow adapters). When a load impedance terminating a coaxial cable matches the cable characteristic impedance, no wave will be reflected and the oscilloscope will display only the incident voltage propagated down the cable. If a mismatch exists, part of the incident wave is reflected. The reflected voltage wave will appear on the oscilloscope display algebraically added to the incident wave. These waveforms are illustrated in views A and B, figure 4-5.

- c. The quality criteria for the rigid coaxial cable used in the T-1054/GRC-144 and R1467/GRC-144 is a VSWR of 1.1 maximum. This can be measured using the reflectometer as follows:

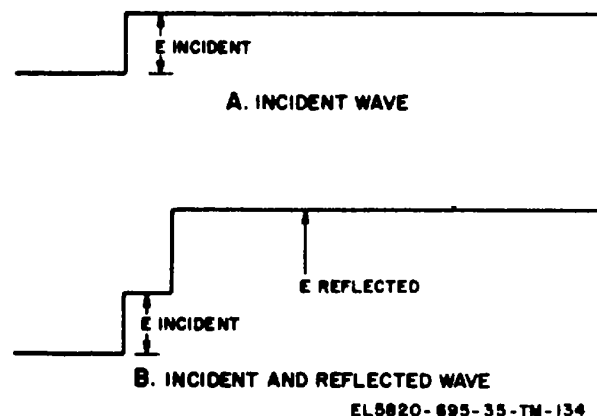


Figure 4-5. Reflectometer test waveforms.

(1) Connect the two elbow adapters to bridge the STEP OUTPUT jack to the SIGNAL IN jack on the front panel of the reflectometer, and connect the GR874-to-N adaptor and the UG-29B/U adaptor to the SIGNAL OUT jack on the front panel of the reflectometer.

(2) Place POWER switch to ON and set the controls on the reflectometer to the following positions:

Control	Position
OM LINE/OM DISLAY-----	20
MAGNIFIER -----	6
MAGNIFIER DELAY .-----	4
REFL COEFFICIENT-----	0.5
SWEEP -----	NORMAL

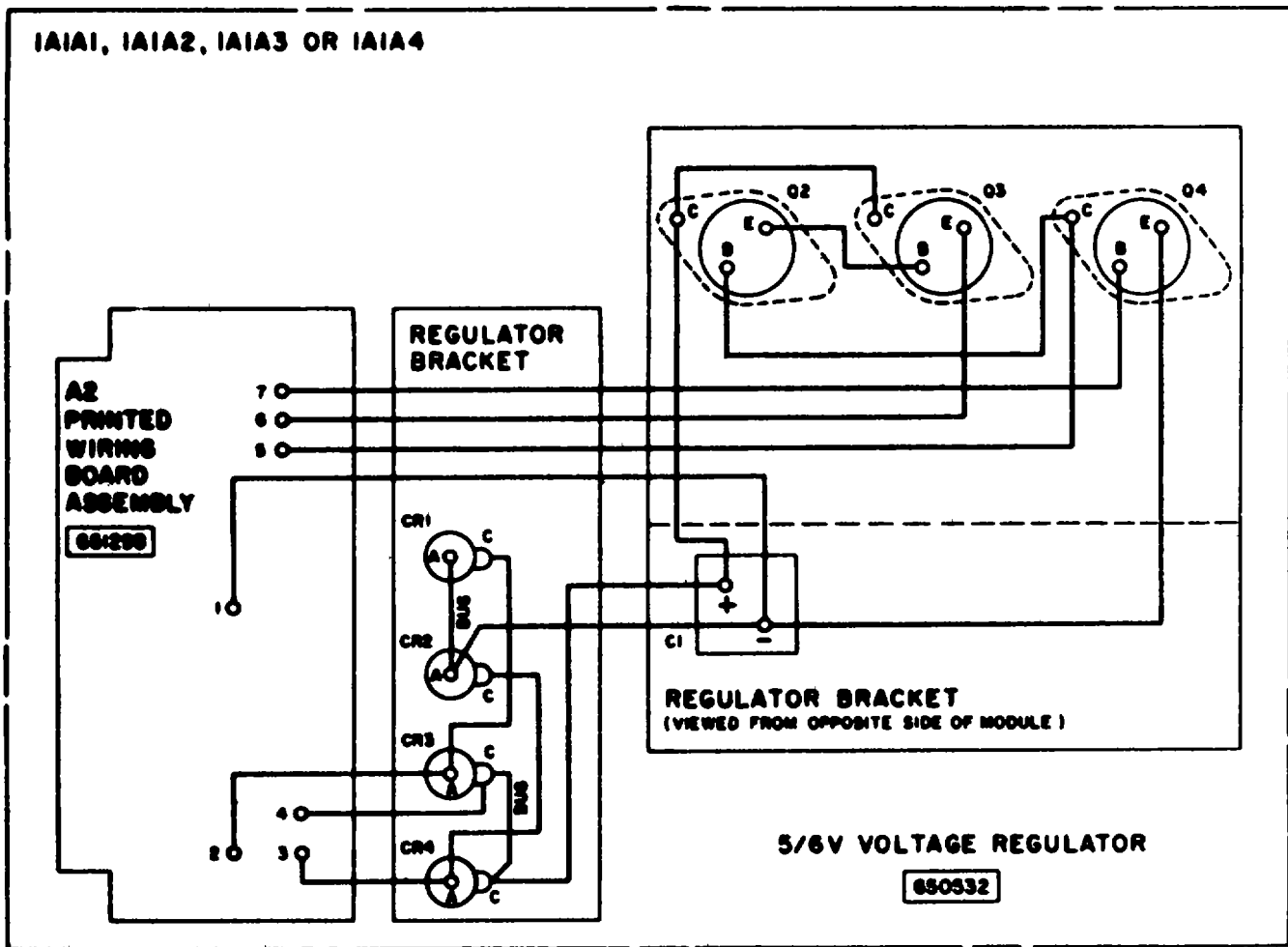
(3) Connect 50 ohm termination HP-908A to the SIGNAL OUT Jack using the adapters installed in step (1).

(4) Adjust the incident wave voltage step to coincide with the center screen graticule line of the oscilloscope using the VERT POSITION control.

(5) Remove the 50 ohm termination and insert the calibrated 1.1 VSWR mismatch (Mecca model 400-1.10). Note the upward deflection point on the oscilloscope, this represents an SWR of 1.1. Therefore, the increments between the 50 ohm terminated center scale and the 1.1 SWR calibrated line indicate values of SWR between the nominal SWR of the 50 ohm termination (typically 1.05 residual SWR) and the calibrated 1.1 SWR reference line. The 1.1 SWR reference point can be adjusted to some convenient graticule line using the VERNIER CAL adjust (inner control of the REFL COEFFICIENT controls).

(6) Remove the calibrated mismatch from the SIGNAL OUT jack and connect the coaxial cable to be tested to the SIGNAL OUT jack using the adaptor GR874B-toOSM J. Observe the oscilloscope to determine if the coaxial cable being tested meets the 1.1 VSWR criteria.



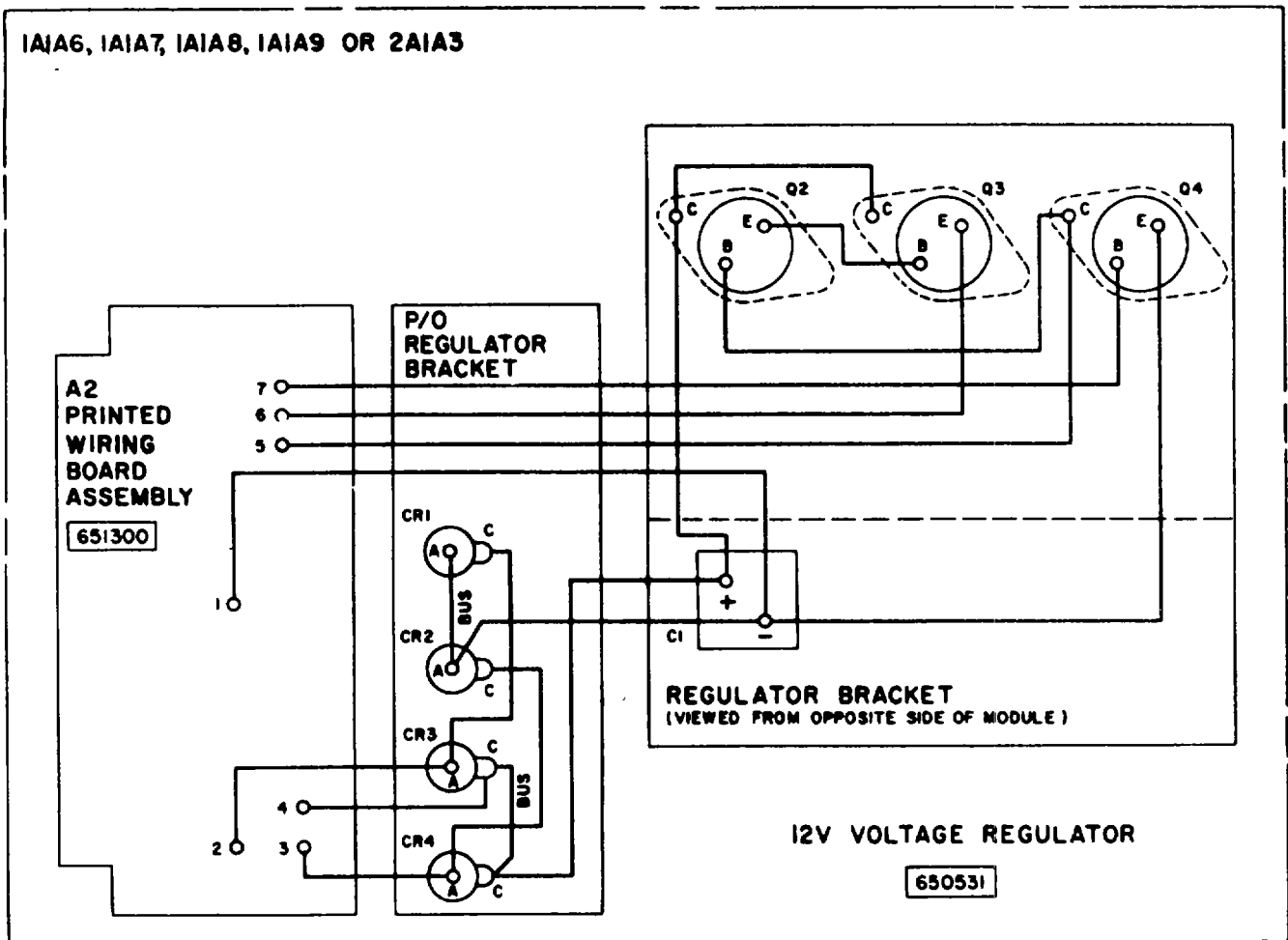


**NOTES:**

1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 22 AWG STRANDED, TEFLON INSULATED, EXCEPT BUS WIRE WHICH IS NO. 22 SOLID.

EL5820-695-35-TM-156

Figure 4-6.5/6v voltage regulator 1A1A1 through 1A1A4, bracket wiring diagram.

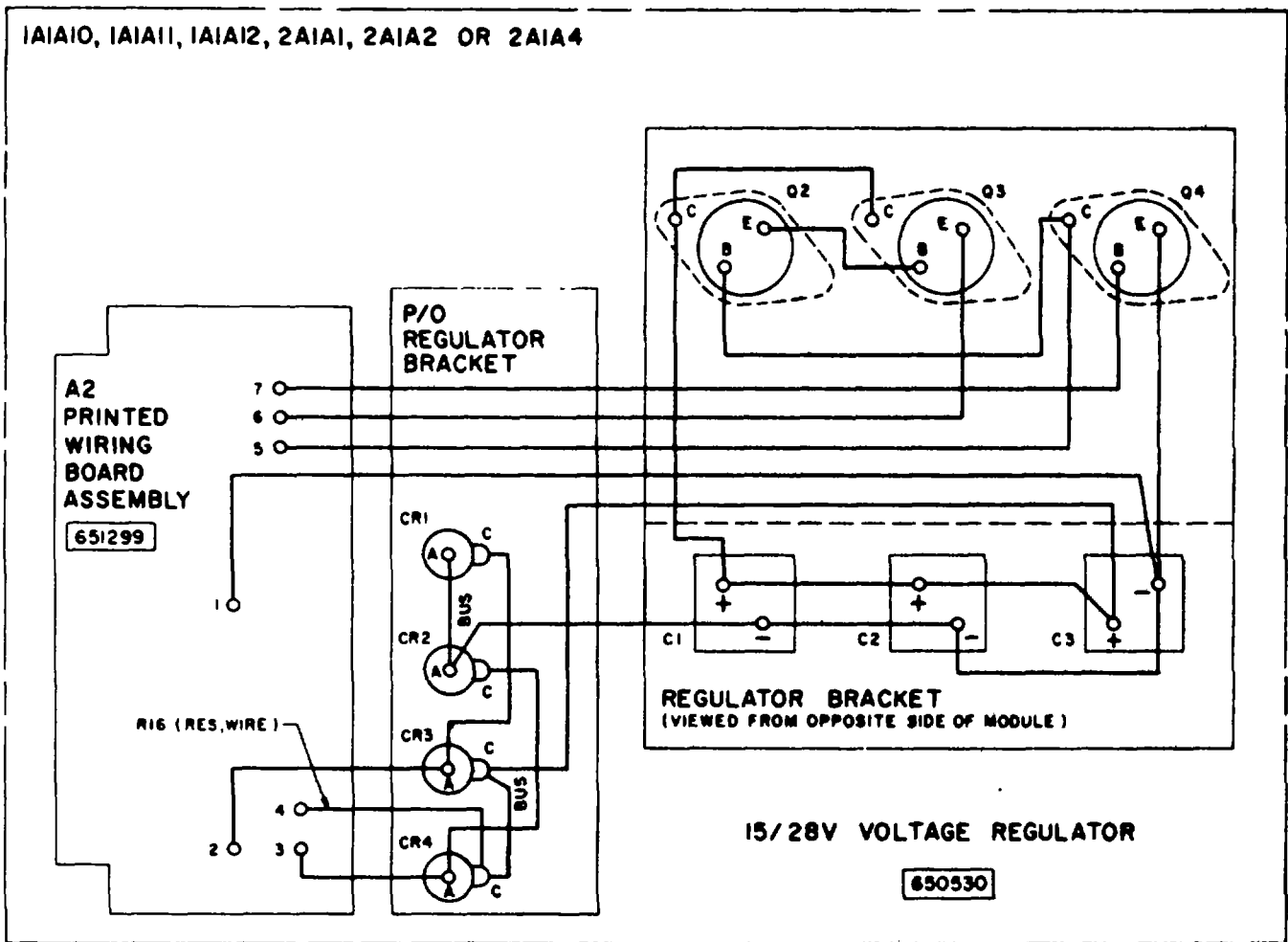


NOTES

- 1 THIS IS A MULTIPLE USE ASSEMBLY  
PARTIAL REFERENCE DESIGNATIONS ARE  
SHOWN FOR COMPLETE DESIGNATION,  
PREFIX WITH UNIT NUMBER AND SUB-  
ASSEMBLY DESIGNATION
- 2 ALL WIRE IS NO 22 AWG STRANDED,  
TEFLON INSULATED, EXCEPT BUS  
WIRE WHICH IS NO 22 SOLID.

EL5820-695-35-TM-158

Figure 4-7. 12v voltage regulator 1A1A6 through 1A1A9 and 2A1A3, bracket wiring diagram.

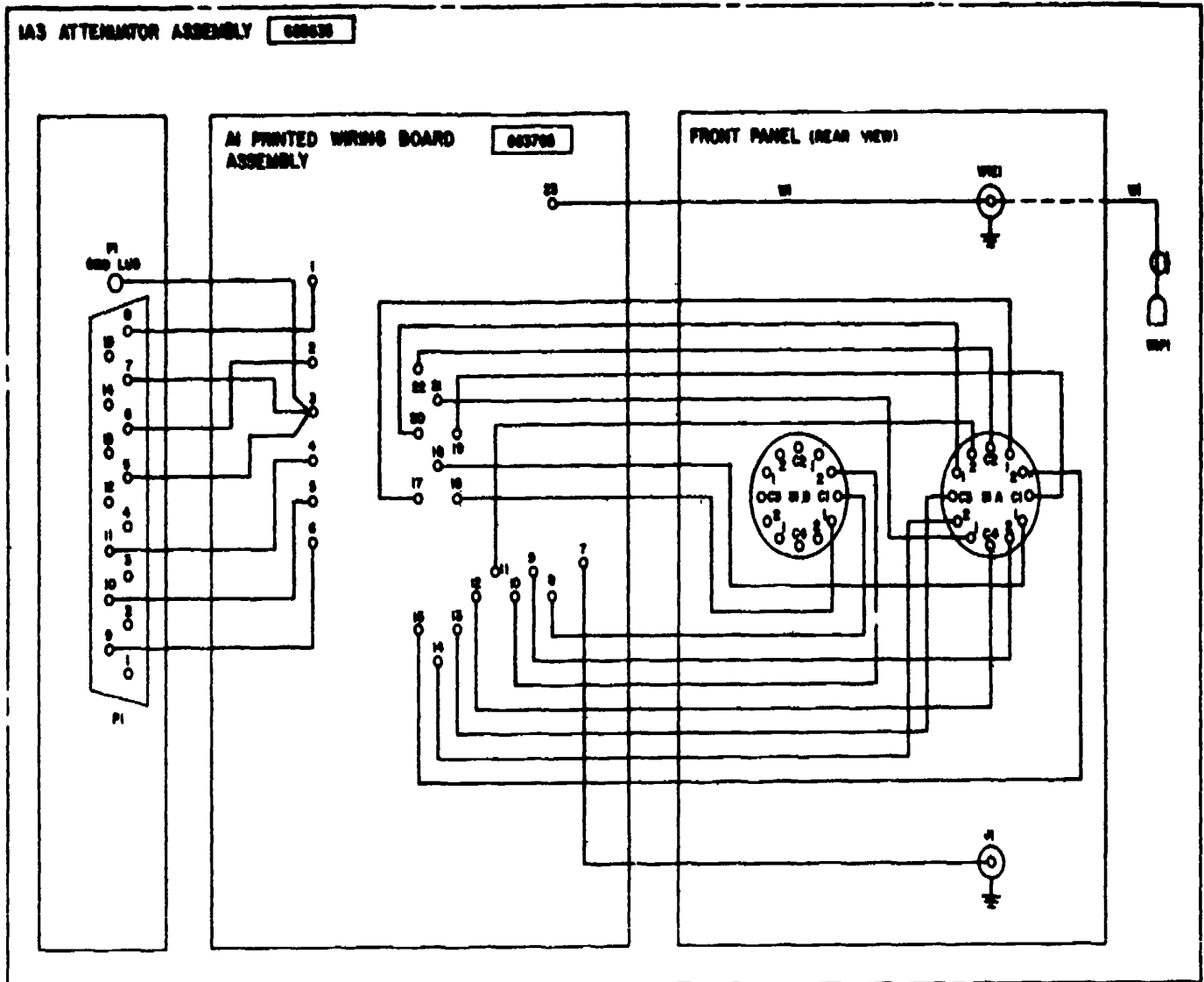


NOTES

- 1 THIS IS A MULTIPLE USE ASSEMBLY PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION
- 2 ALL WIRE IS NO 22 AWG STRANDED, TEFLON INSULATED, EXCEPT BUS WIRE WHICH IS NO 22 SOLID

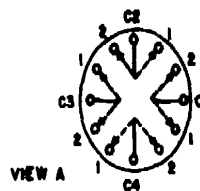
EL5820-695-35-TM-100

Figure 4-8. 15/28v voltage regulator 1A1A10 through 1A1A12, 2A1A1, 2A1A2, and 2A1A4, bracket wiring diagram.



NOTES:

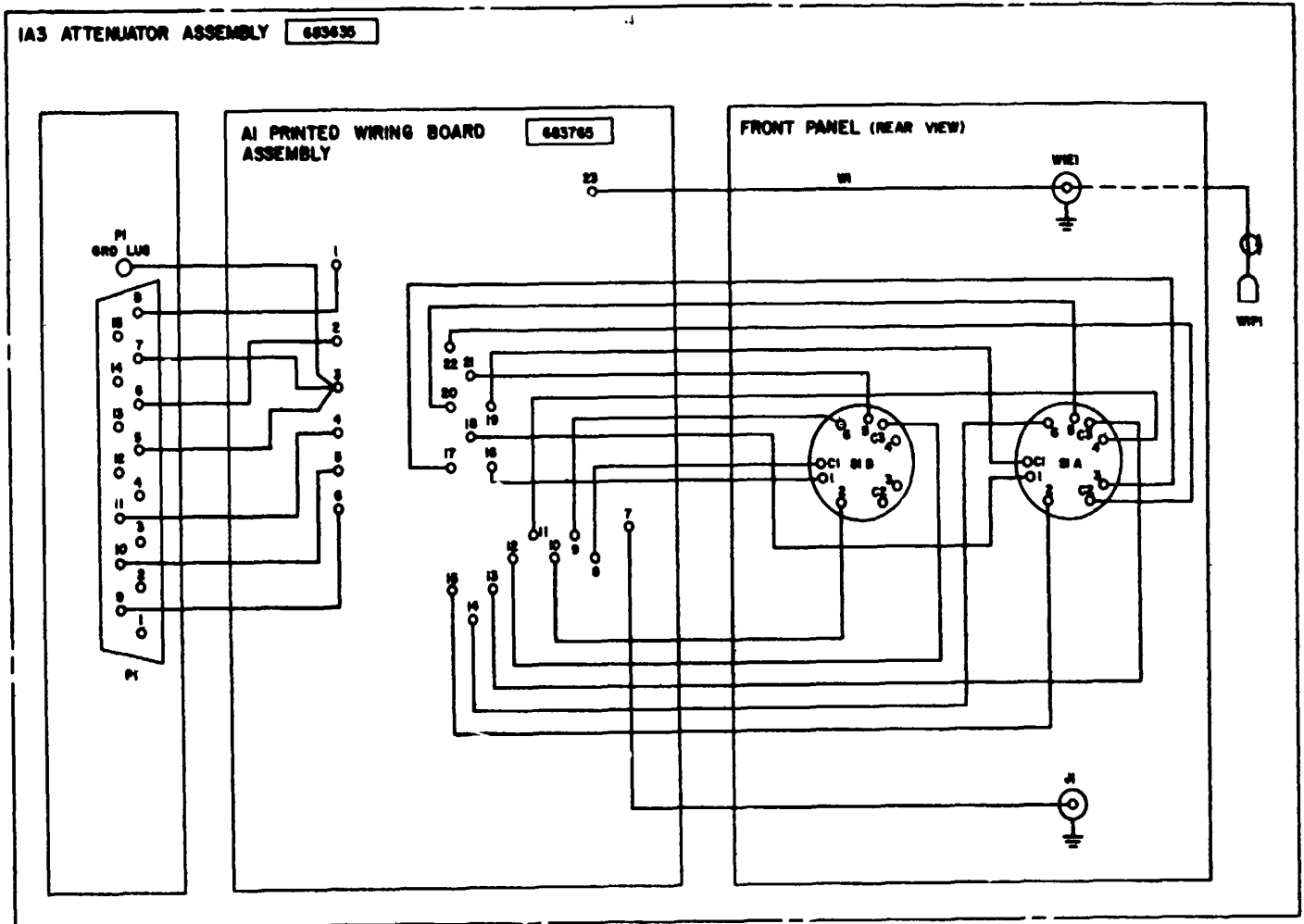
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 1AS AND SUBASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 22 AWG STRANDED, TEFLON INSULATED, EXCEPT CABLE W1.
3. SEE VIEW A FOR TERMINAL CONFIGURATION OF D1A AND D1B (WIRING END).
4. SWITCH PART NO. 84-B-684380 (PART 1 OF 2) OR PART NO. 84-B-684783 (PART 2 OF 2) IS USED FOR S1. REFER TO APPROPRIATE WIRING DIAGRAM.



EL000-695-35-TM-C-11 ①

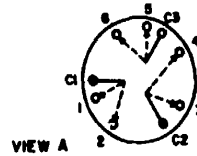
Figure 4-9(1). Attenuator Assembly 1AS wiring diagram (part 1 of 2).

Change 1 4-14



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH IAS AND SUBASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 22 AWG STRANDED, TEFLON INSULATED, EXCEPT CABLE W1.
3. SEE VIEW A FOR TERMINAL CONFIGURATION OF S1 A AND S1 B (WIRING END).
4. SWITCH PART NO. SM-S-684380 (PART 1 OF 2) OR PART NO. SM-S-684783 (PART 2 OF 2) IS USED FOR S1. REFER TO APPROPRIATE WIRING DIAGRAM.



EL 6820-695-35-TM-C-11 (2)

Figure 4-9(2). Attenuator Assembly 1AS, wiring diagram (part 2 of 2).

Change 1 4-14.1

**NOTES**

- 1 THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION.
- 2 ALL WIRE IS NO.22 AWG STRANDED, TEFLON INSULATED

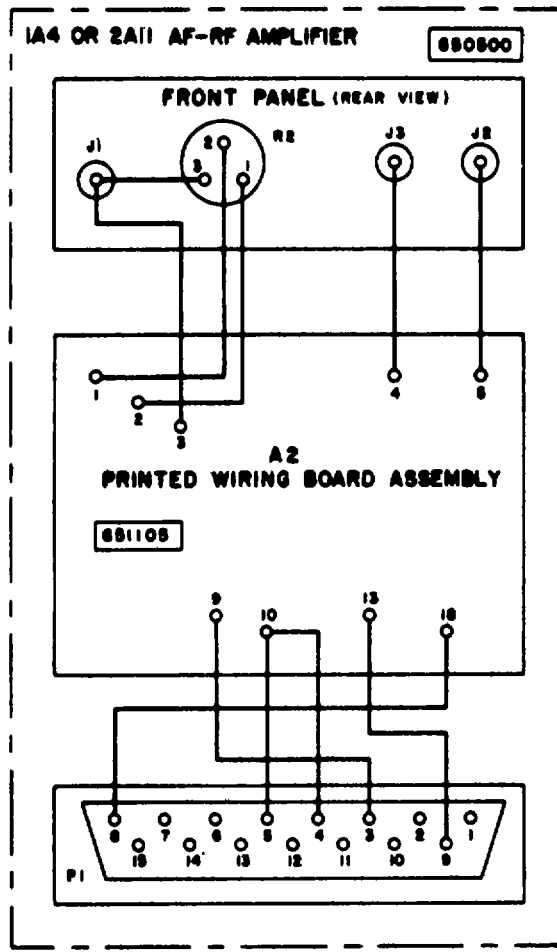
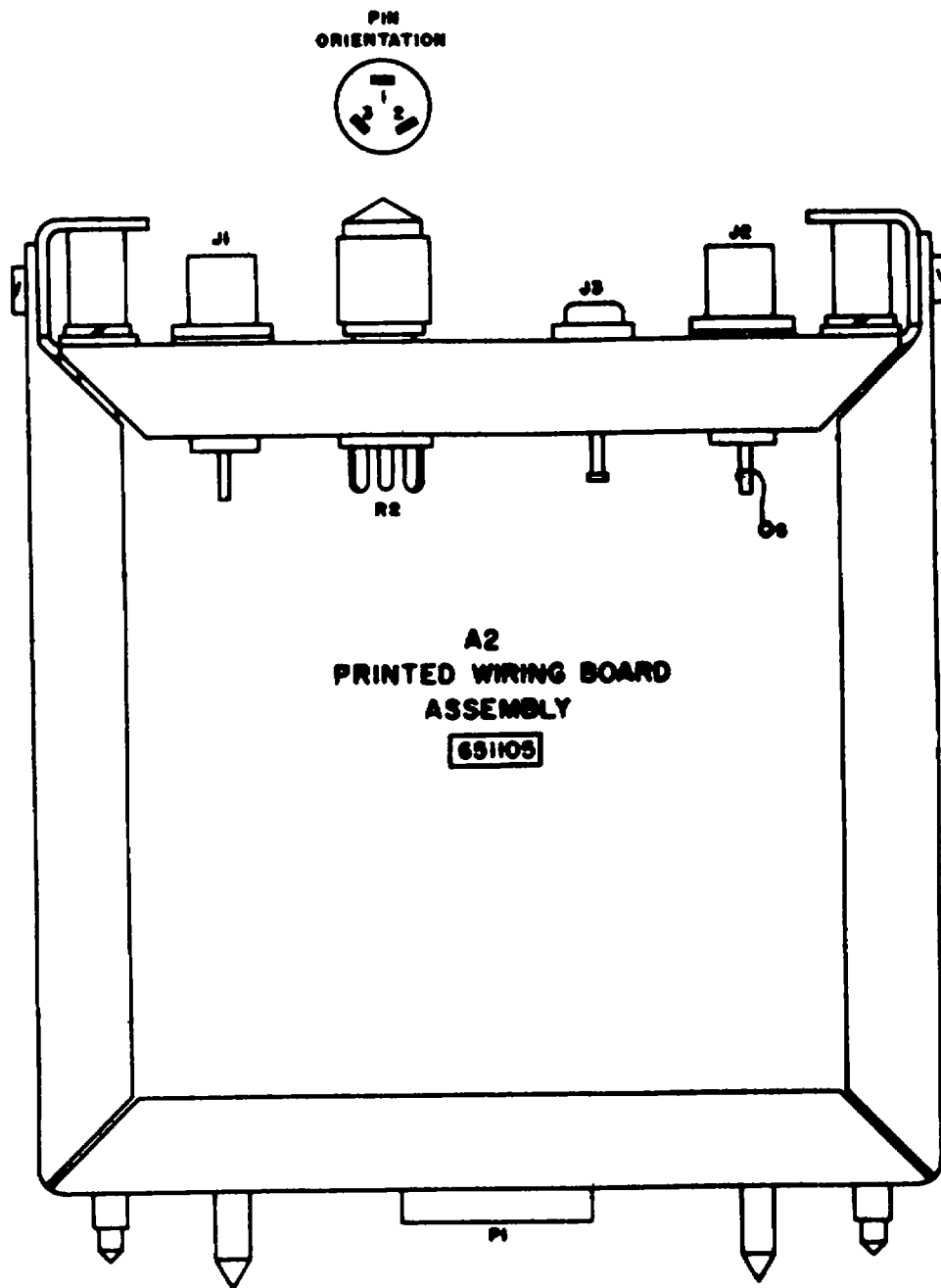


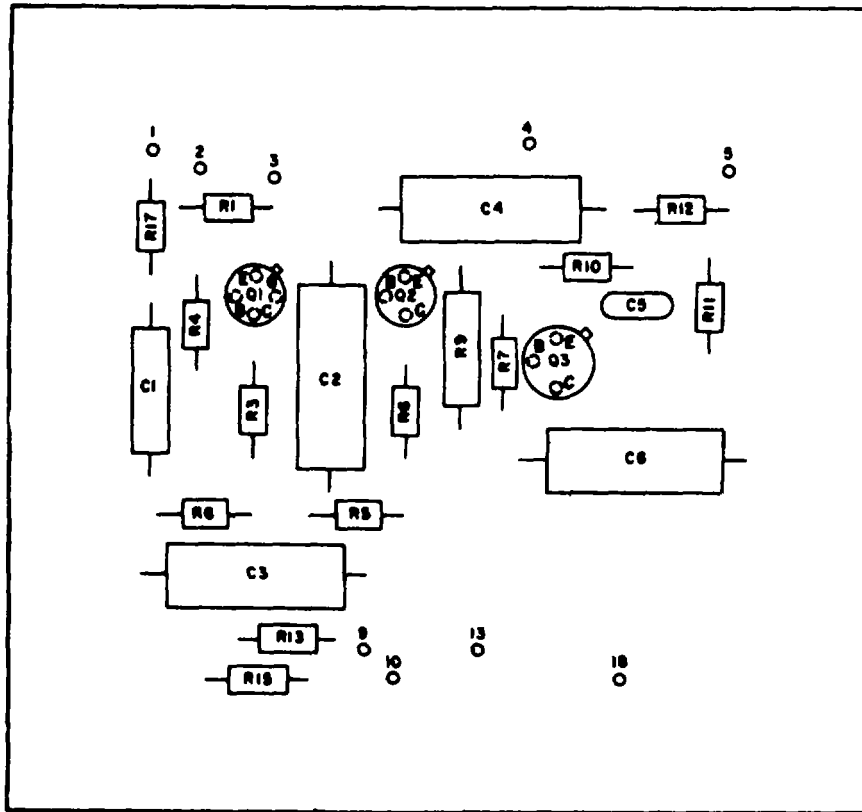
Figure 4-10. Af-rf amplifier 1A4/2A11, wiring diagram.



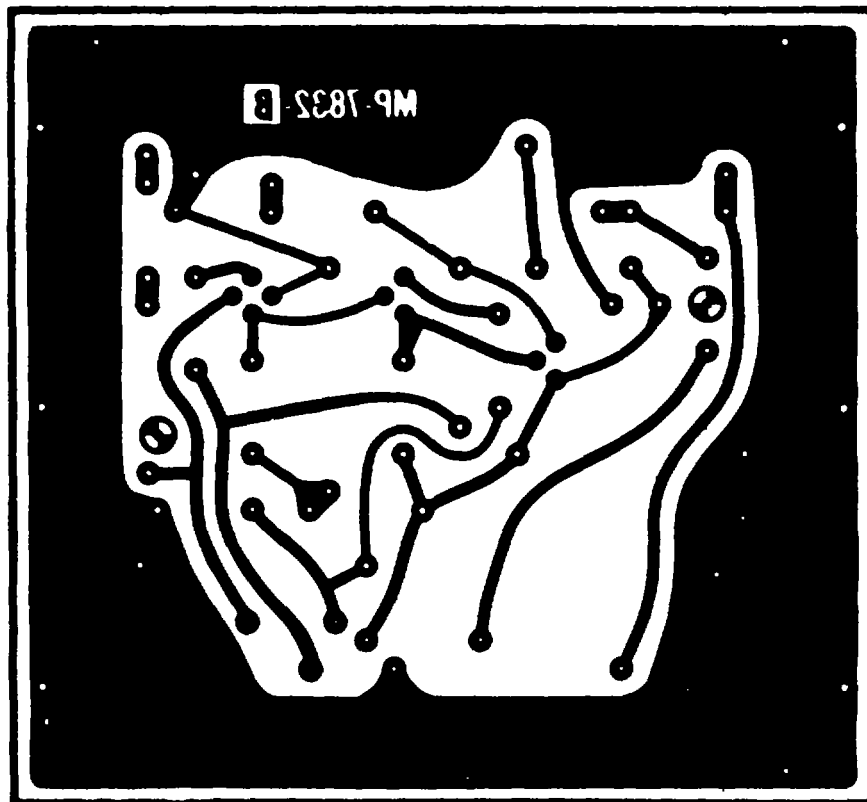
**NOTE:**  
 THIS IS A MULTIPLE USE ASSEMBLY.  
 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.  
 FOR COMPLETE DESIGNATION, PREFIX WITH 1A4  
 OR 2A11 AND SUBASSEMBLY DESIGNATION.

EL 6950-000-00-TB-107 ①

Figure 4-11(1). Af-rf amplifier 1A4/2A11, parts location and printed wiring diagram (part 1 of 2)



A. PARTS ON FRONT OF BOARD A2.

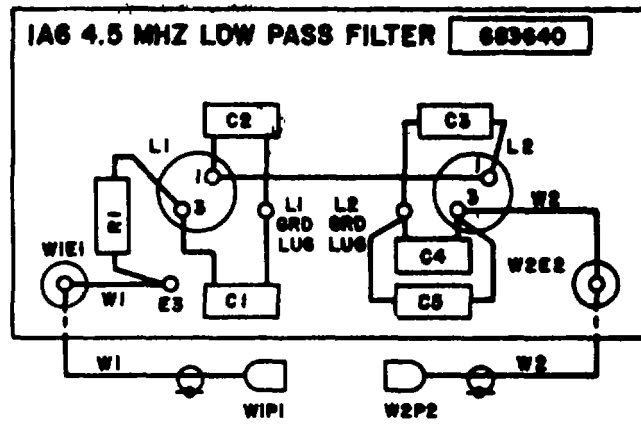


B. WIRING ON BACK OF BOARD A2 (VIEWED THROUGH FRONT).

EL6820-695-35-TM-167 ②

Figure 4-11(2). Af-rf amplifier 1A4/2A11, parts location and printed wiring diagram (part 2 of 2)





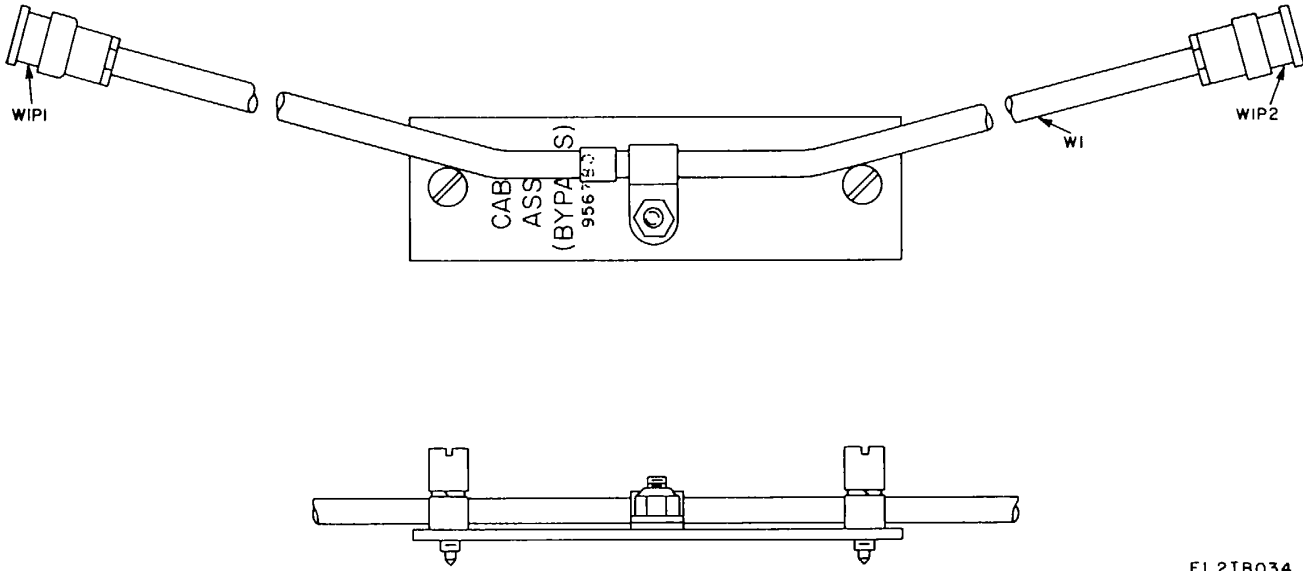
**NOTES:**

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH IA6.

2. WIRING IS NO. 22 AWG STRANDED WIRE, TEFLON INSULATED, EXCEPT CABLES W1 & W2.

EL6820-695-35-TM-170

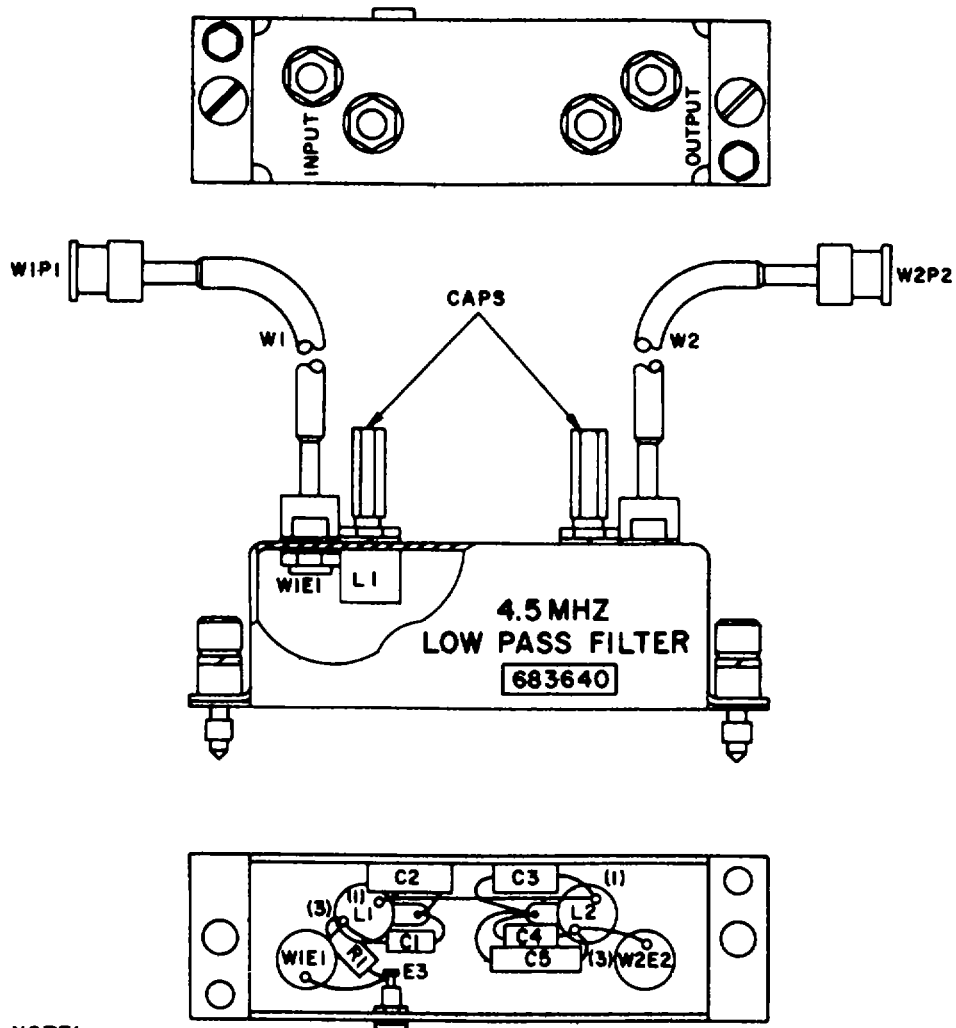
Figure 4-12. 4.5 MHz low pass filter 1A6, wiring diagram.



EL2IB034

Figure 4-12.1 Cable, Bypass Parts Location Diagram.

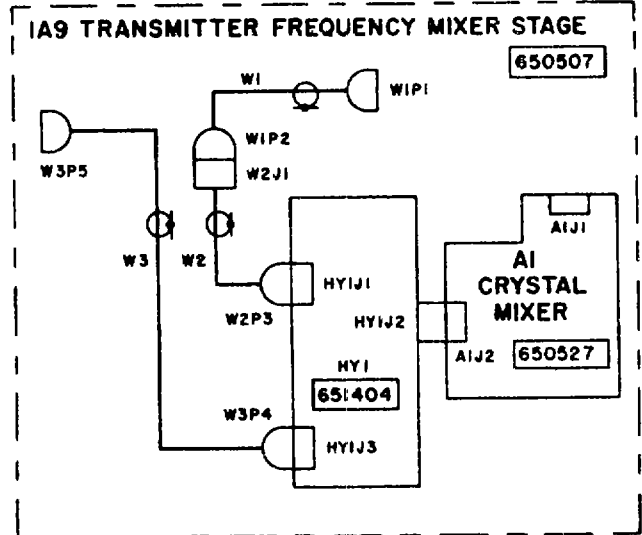
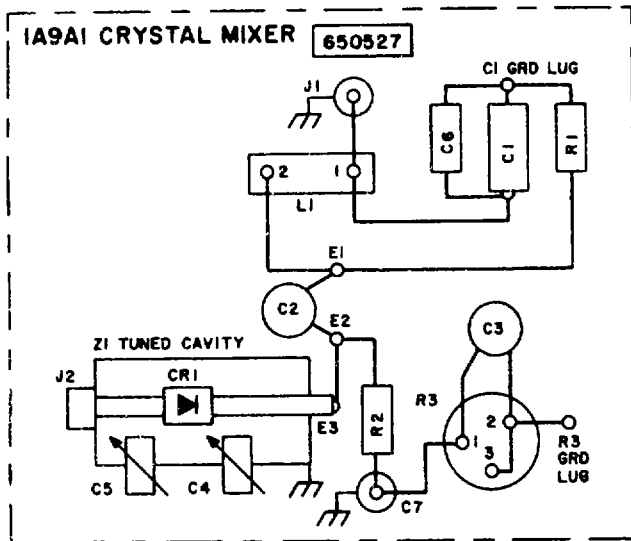
Change 6 4-18.1/(4-18.2 blank)



**NOTE:**  
 PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN. FOR COMPLETE  
 DESIGNATION, PREFIX WITH IA6.

EL5820-695-35-TM-171

Figure 4-13. 4.5 MHz low pass filter 1A6, parts location.



NOTES

1 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION

2 ALL WIRE IS NO 22 SOLID, TINNED COPPER

EL5820-695-35-TM-176

Figure 4-14. Transmitter frequency mixer stage 1A9, wiring diagram.

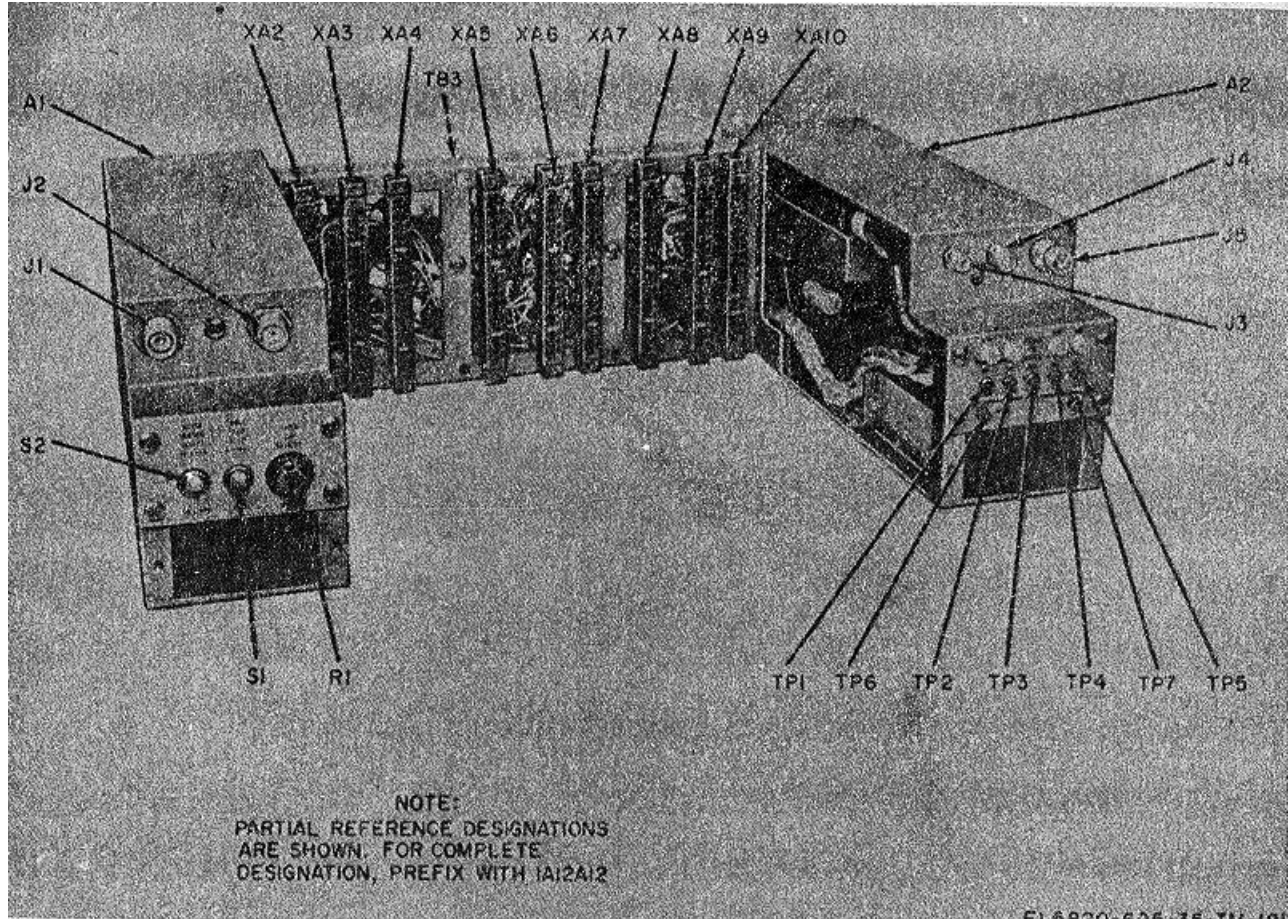


Figure 4-15. Digital data modern chassis 1A12A12, parts location.

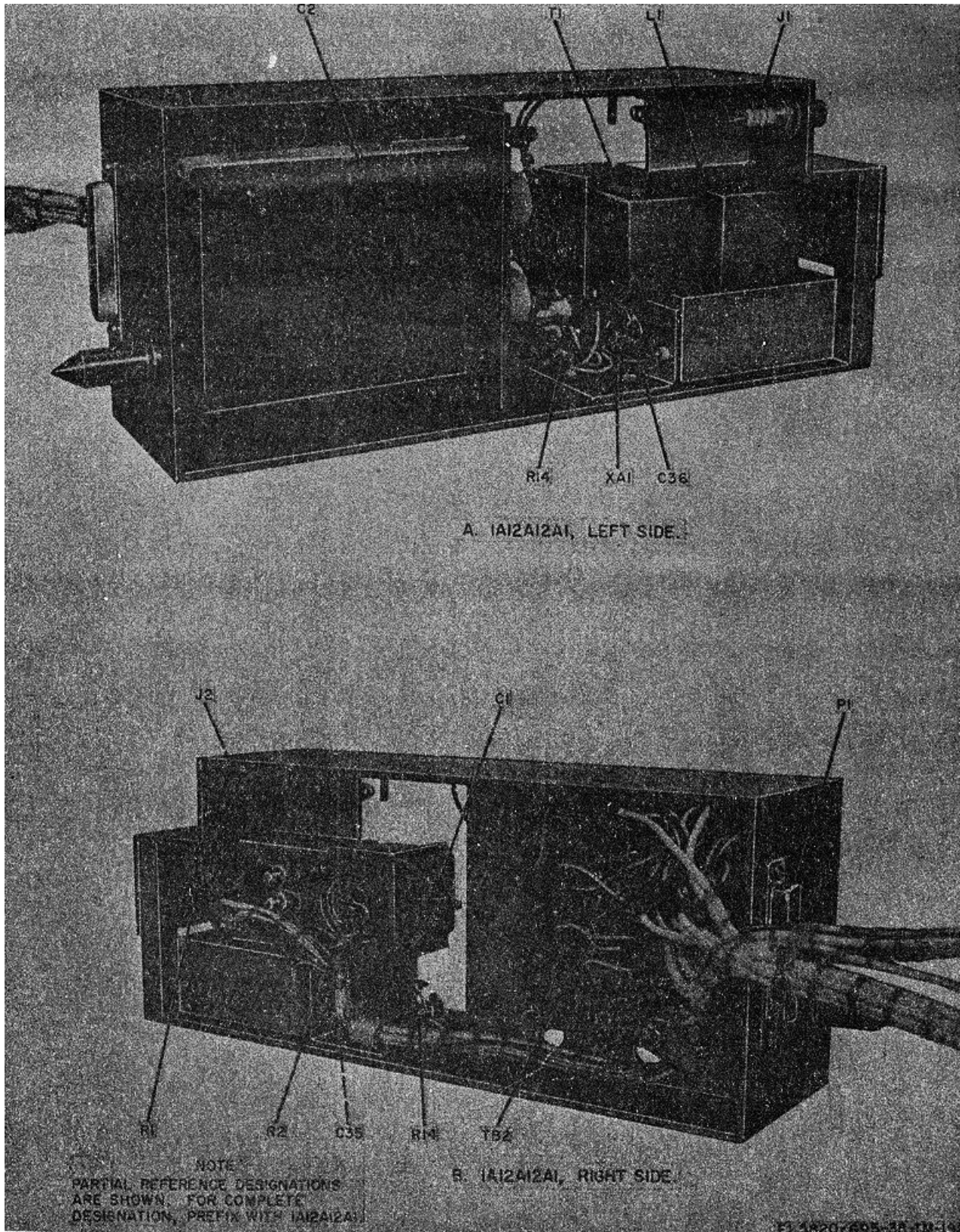


Figure 4-16. Digital data modern chassis assembly 1A12A12A1, parts location.



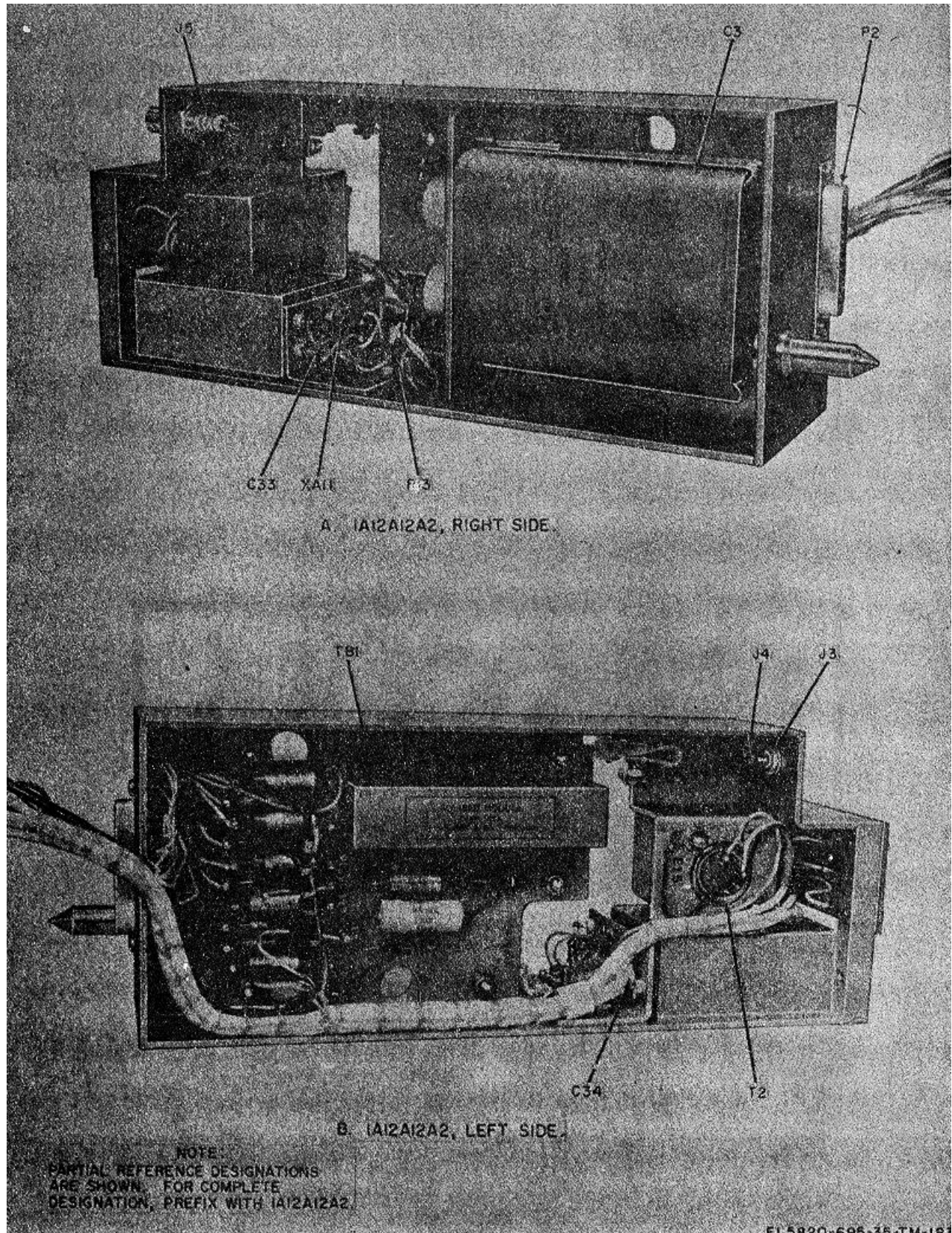
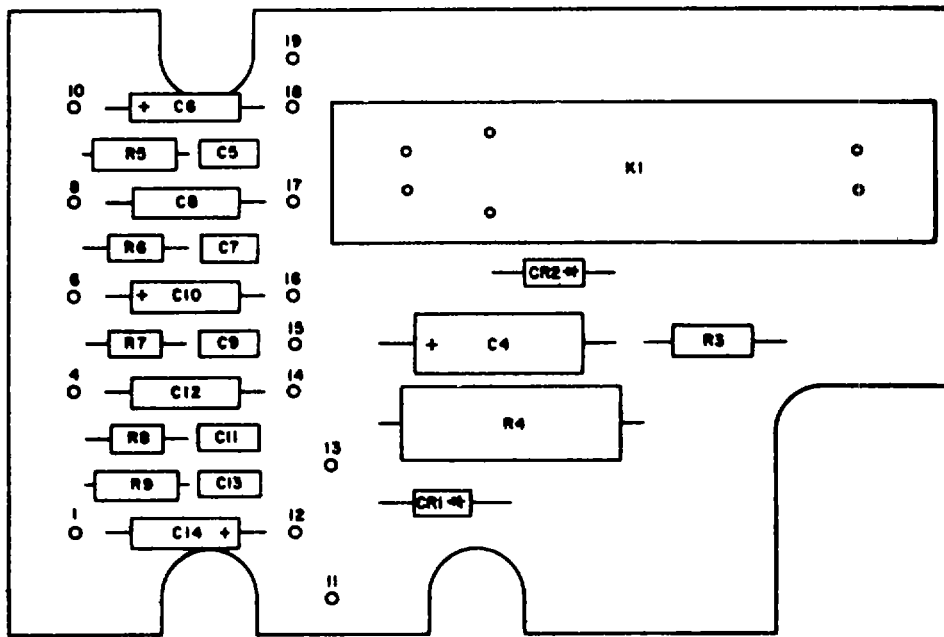
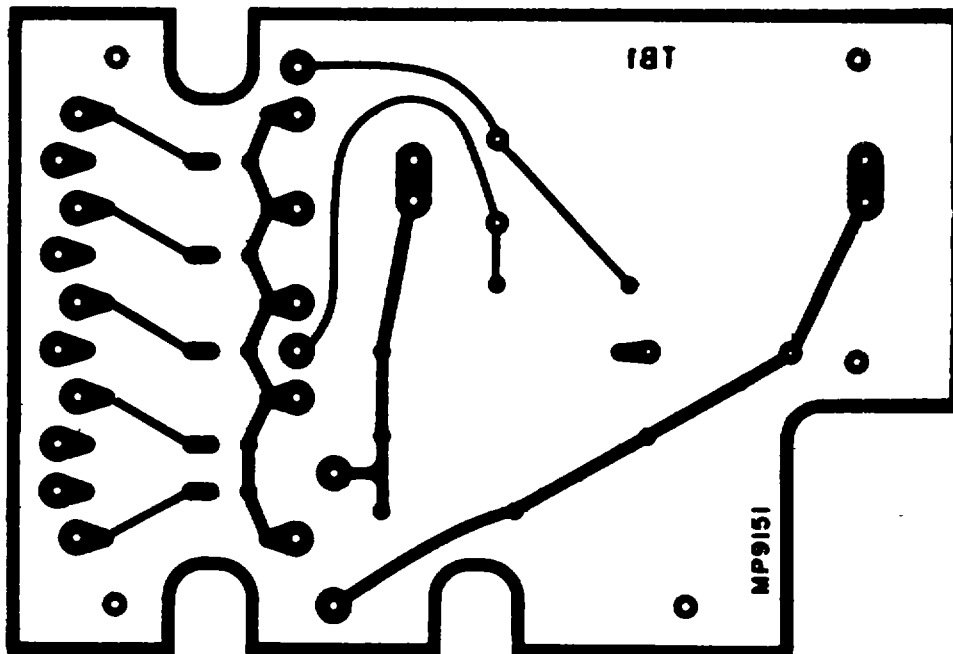


Figure 4-17. Digital data modem chassis assembly 1A12A12A2, PARTS LOCATION.



A. PARTS ON FRONT OF BOARD TBI (663025).



B. WIRING ON BACK OF BOARD TBI (VIEWED THROUGH FRONT).

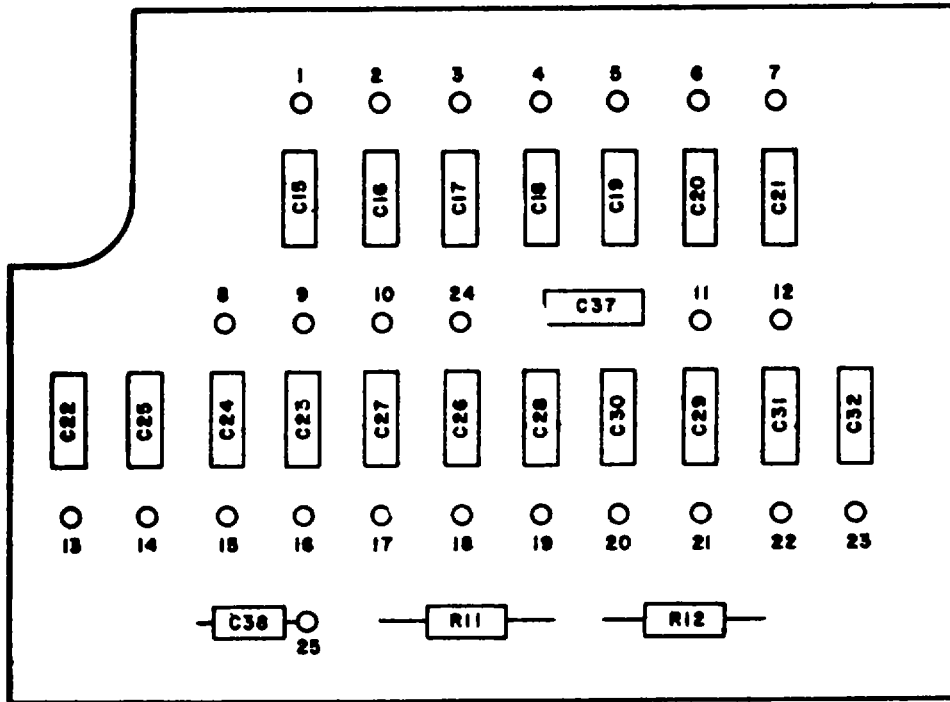
NOTE:

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.  
FOR COMPLETE DESIGNATION, PREFIX WITH 1A12A12A2TB1

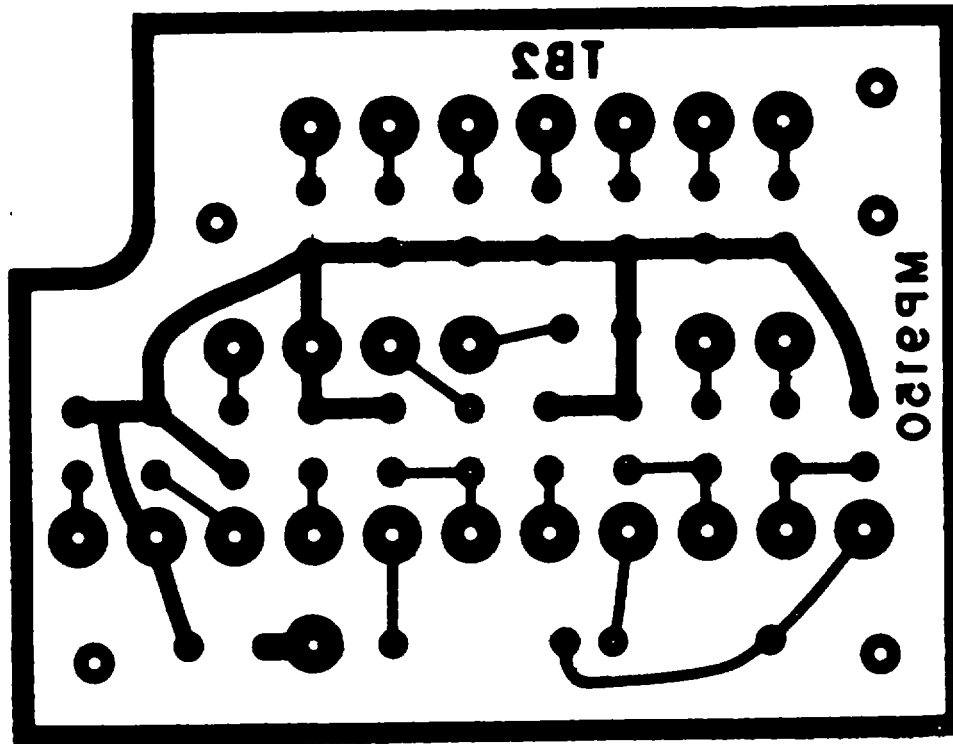
EL5820-695-35-TB-104

Figure 4-18. Printed wiring board assembly 1A12A12A2TB1, parts location and printed wiring diagram.





A. PARTS ON FRONT OF BOARD TB2 (683822)



B. WIRING ON BACK OF BOARD TB2 (VIEWED THROUGH FRONT).

**NOTE:**

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.  
FOR COMPLETE DESIGNATION, PREFIX WITH 1A12A12A1TB2

EL5820-695-35-TM-185

Figure 4-19. Printed wiring board assembly 1A12A12A2TB1, parts location and printed wiring diagram.

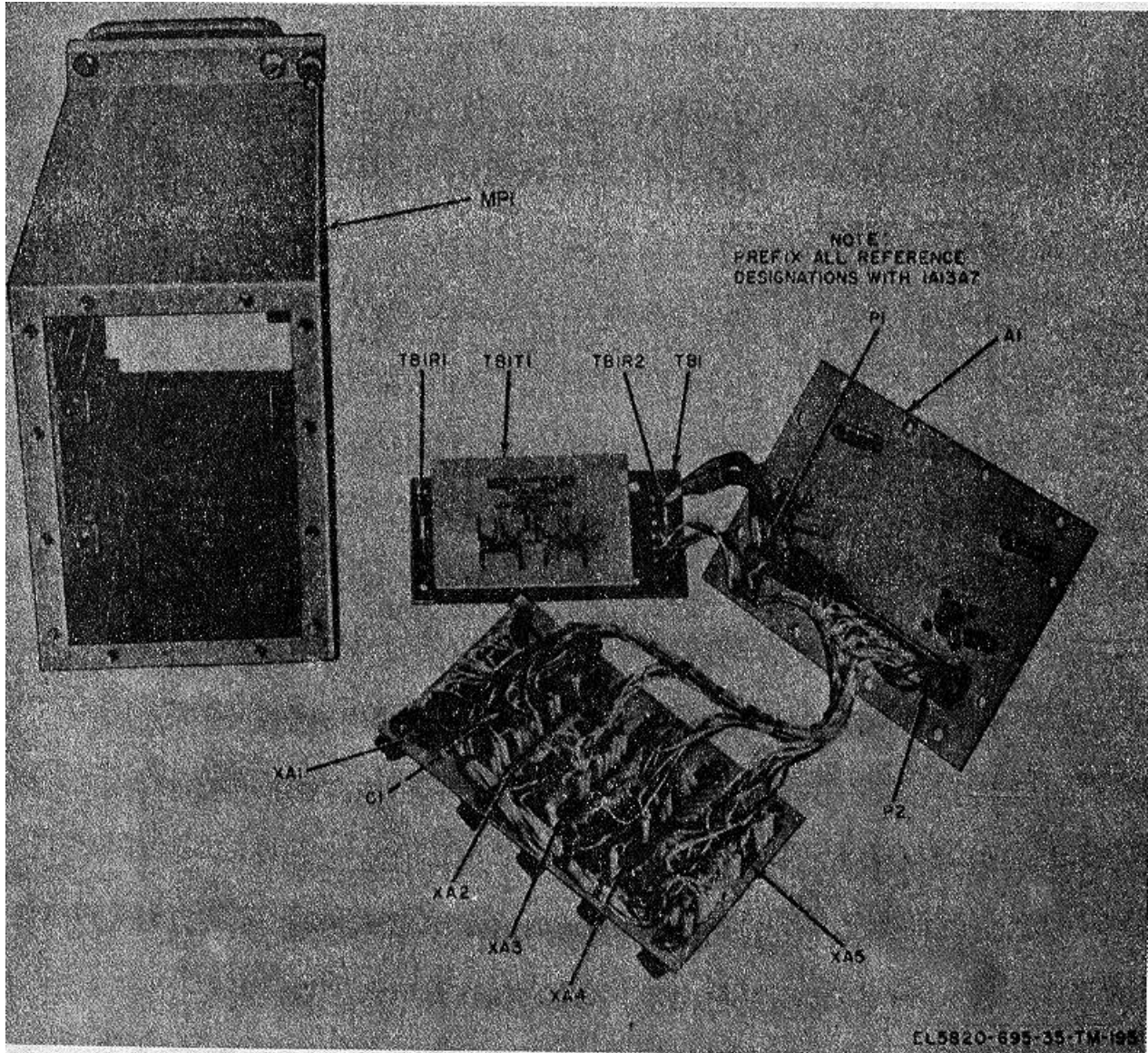
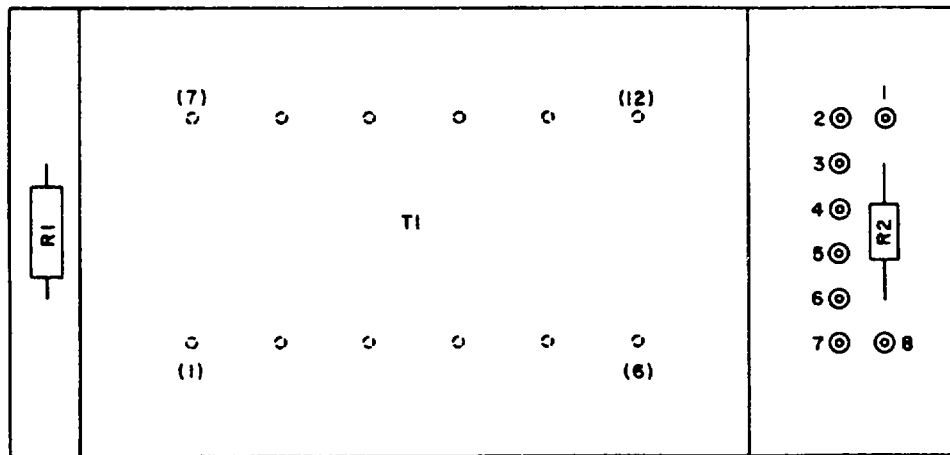
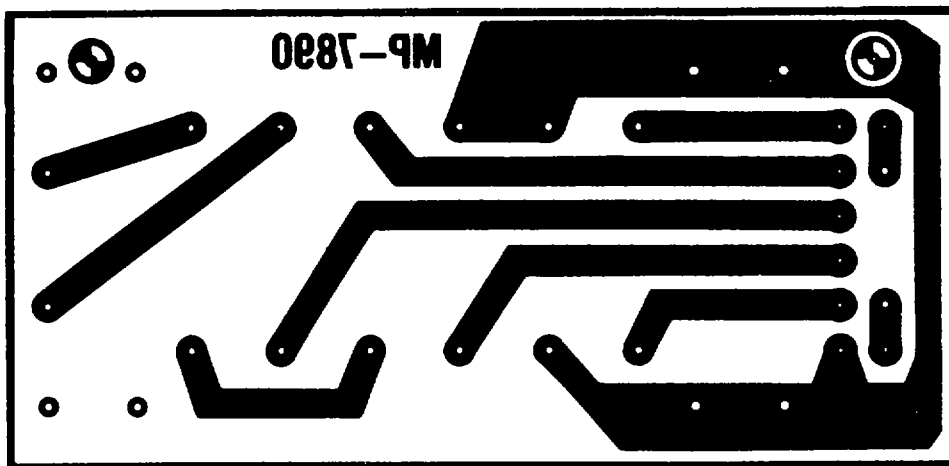


Figure 4-20. Orderwire chassis 1A13A7, partially disassembled, parts location.



A. PARTS ON FRONT OF BOARD TBI (652087).



B. WIRING ON BACK OF BOARD TBI (VIEWED THROUGH FRONT).

**NOTE:**

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN  
FOR COMPLETE DESIGNATION, PREFIX WITH 1A13A7TB1

EL5820-695-35-TM-196

Figure 4-21. Printed wiring board assembly 1A13A7TB1, parts location and printed wiring diagram.

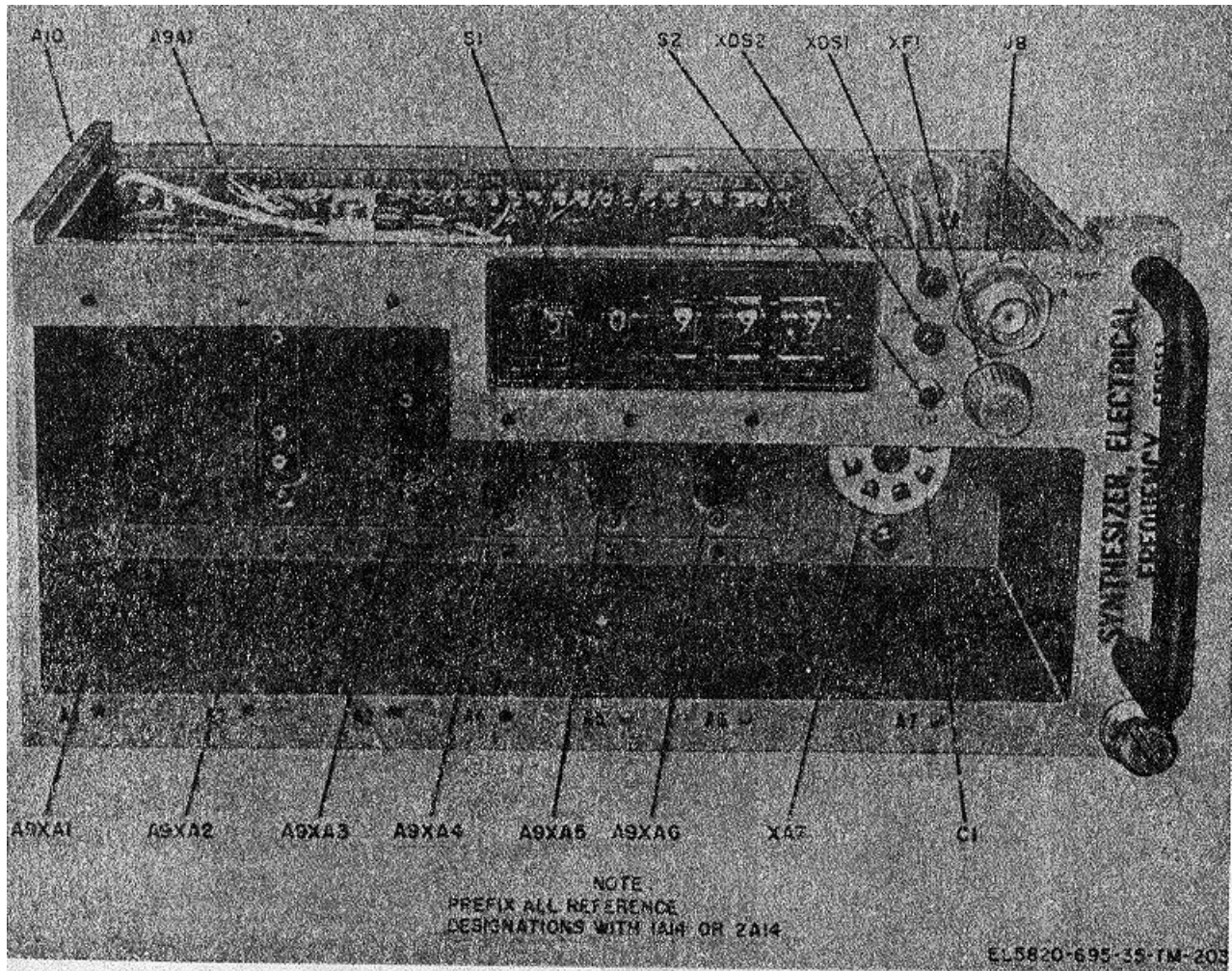


Figure 4-22. Electrical frequency synthesizer 1A14/2A14, partially disassembled, front view, parts location

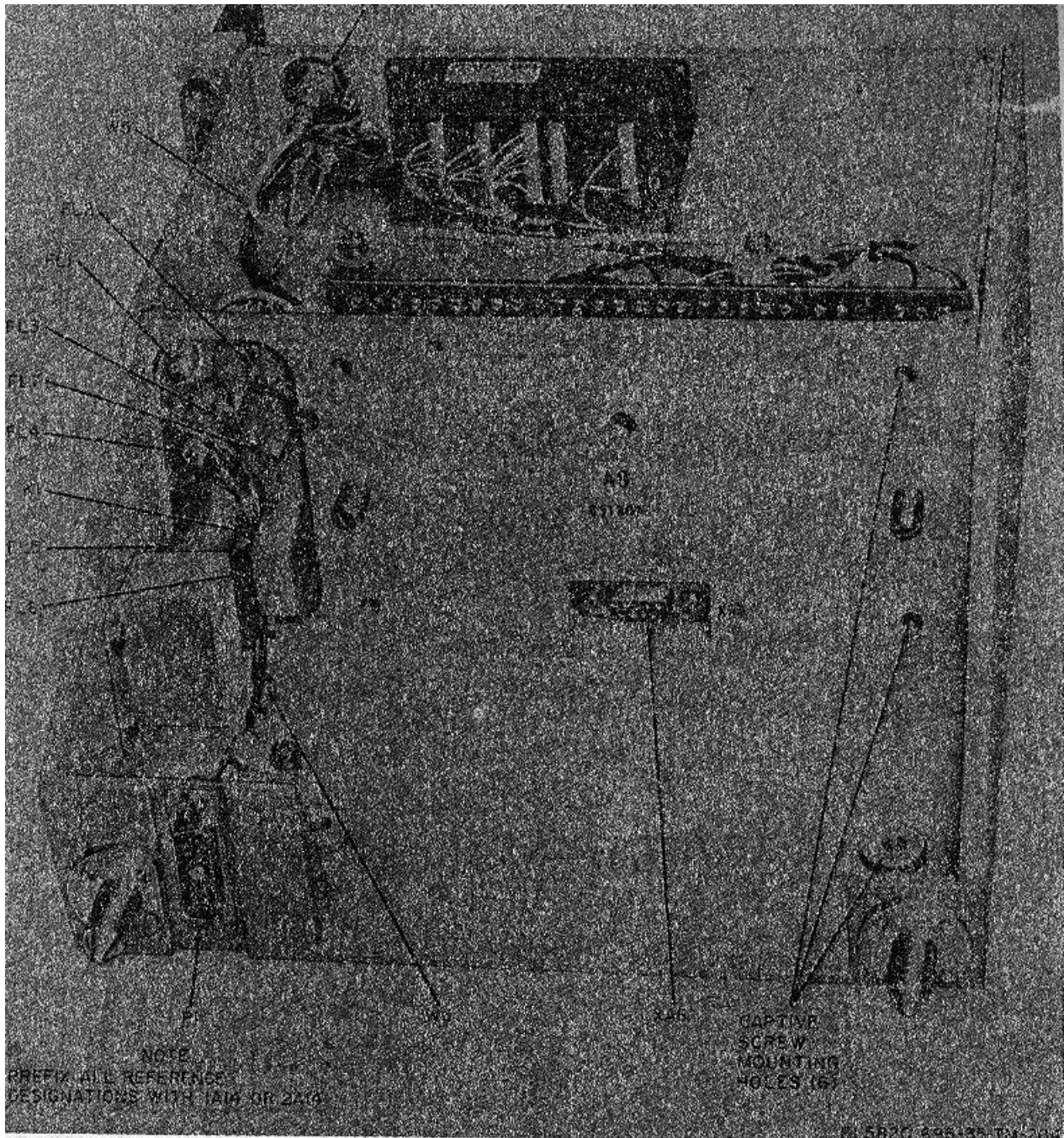
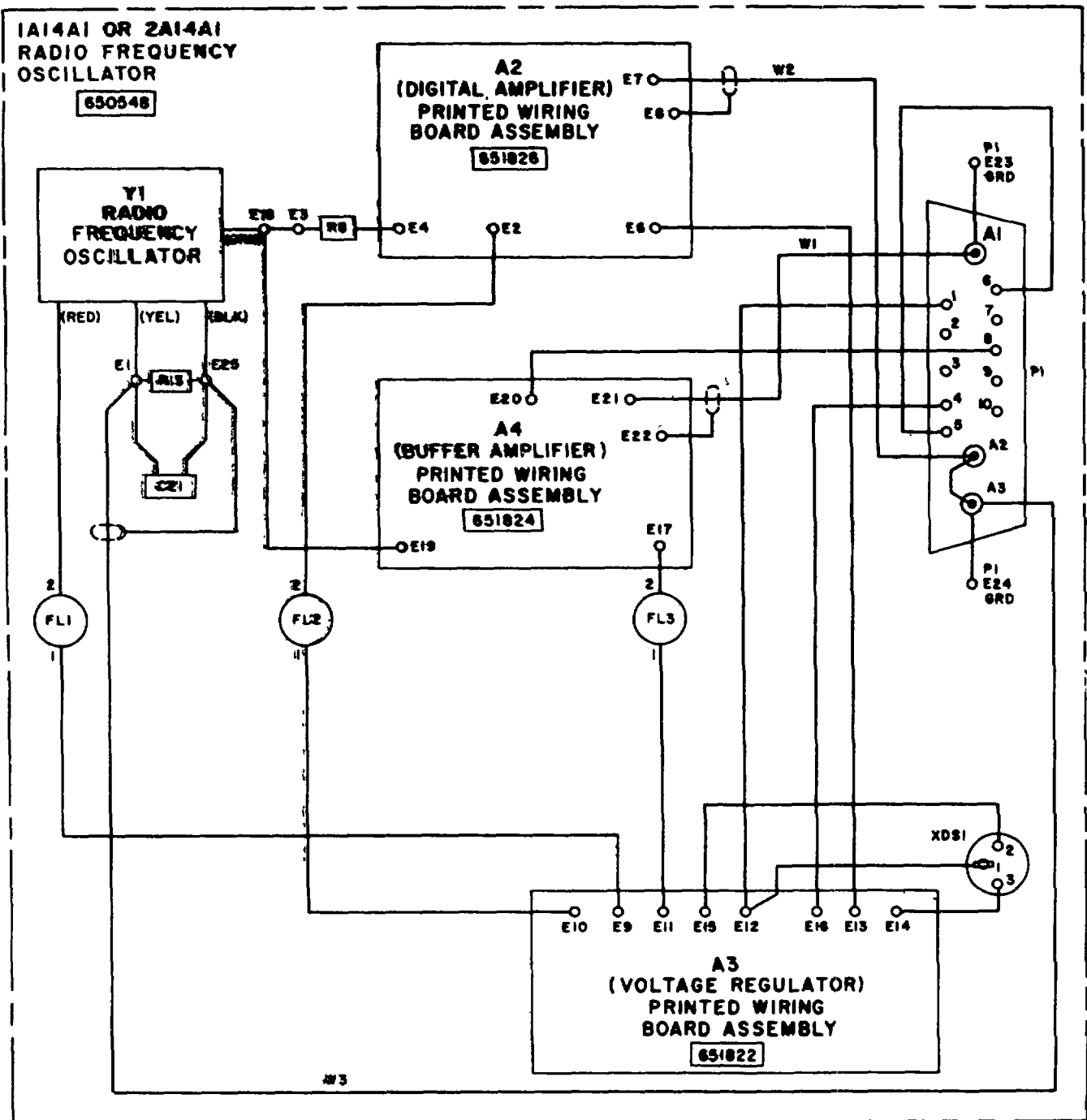


Figure 4-23. Electrical frequency synthesizer 1A14/2A14, partially disassembled,  
rear view, parts location  
4-29



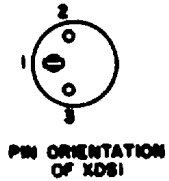
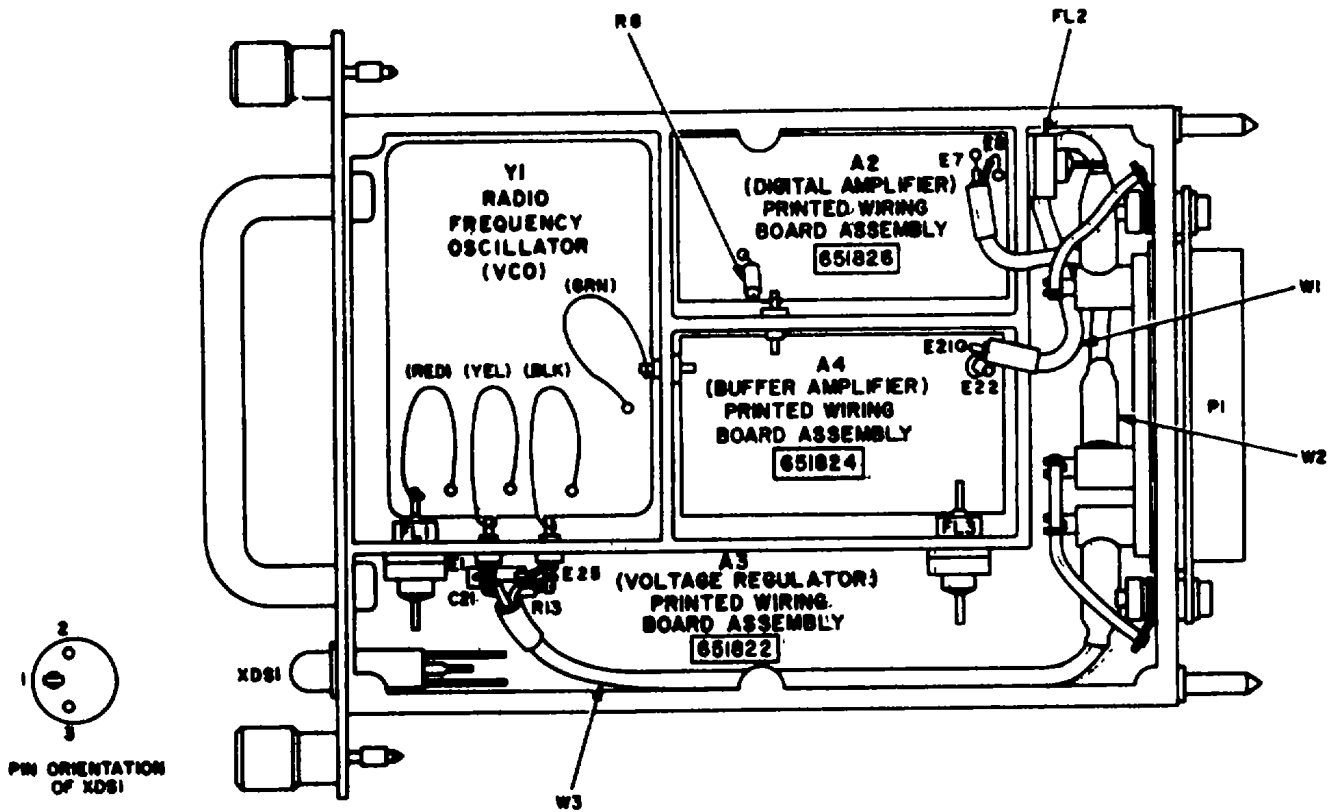
NOTE

- 1 THIS IS A MULTIPLE USE ASSEMBLY PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A14A1 (T-1054/GRD-144) OR 2A14A1 (R-1467/GRD-144).
- 2 ALL WIRE IS NO. 26 AWG.

EL5820-695-35-TM-205

Figure 4-24. Radio frequency oscillator 1A14A1/2A14A1, wiring diagram.

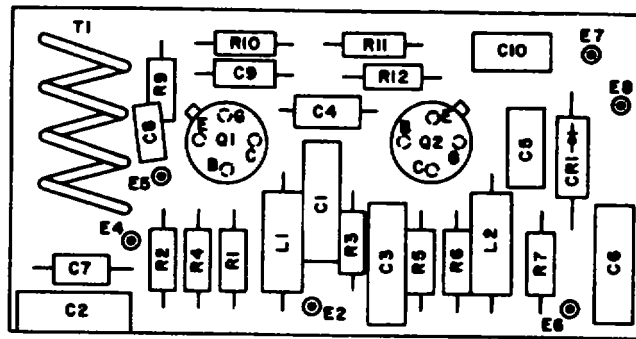




**NOTE**  
 THIS IS A MULTIPLE USE ASSEMBLY.  
 PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN. FOR COMPLETE DESIGNATION,  
 PREFIX WITH 1A14A1 (T-1084/GR-144) OR  
 2A14A1 (R-1467/GR-144).

EL5820-695-35-TM-206 ①

Figure 4-25(1). Radio frequency oscillator 1A11A1/A14,A11, parts location and printed wiring diagram (part 1 of 4)  
 4-31



A. PARTS ON FRONT OF BOARD A2

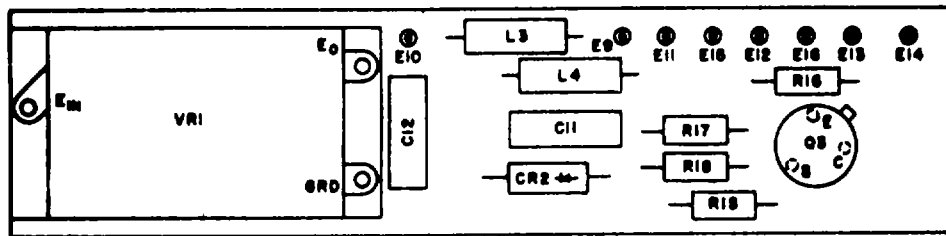


B. WIRING ON-BACK OF BOARD A2  
(VIEWED THROUGH FRONT)

EL5820-695-35-TM-206 (2)

Figure 4-25(1). Radio frequency oscillator 1A11A1/A14,A11, parts location and printed wiring diagram (part 2 of 4)





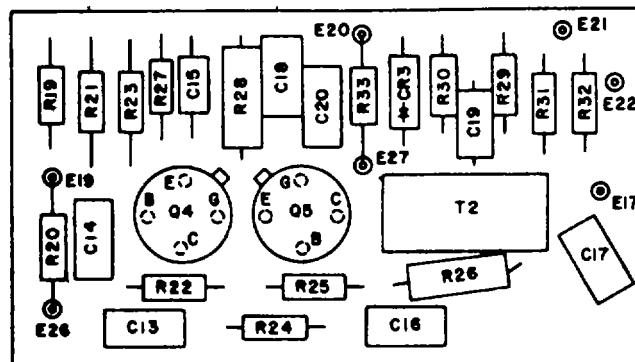
A. PARTS ON FRONT OF BOARD A3



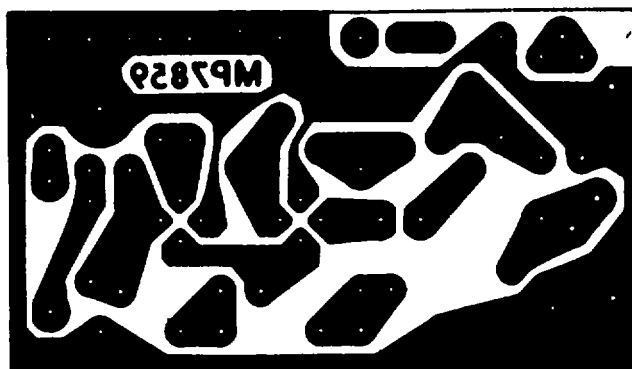
B. WIRING ON BACK OF BOARD A3  
(VIEWED THROUGH FRONT)

EL5820-695-35-TM-206 ③

Figure 4-25(1). Radio frequency oscillator 1A11A1/A14,A11, parts location and printed wiring diagram (part 3 of 4)



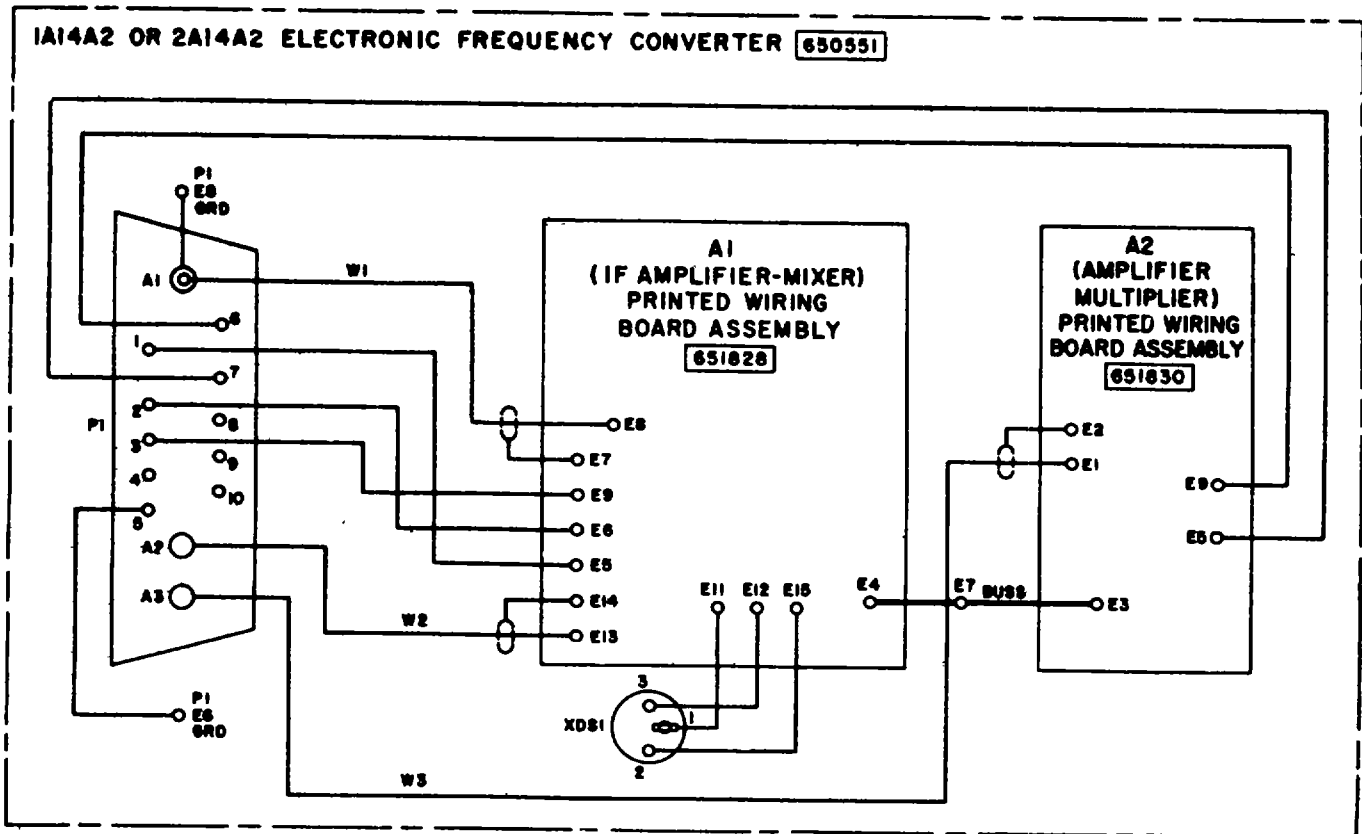
A. PARTS ON FRONT OF BOARD A4



B. WIRING ON BACK OF BOARD A4  
(VIEWED THROUGH FRONT)

EL5820-695-35-TM-206 ④

Figure 4-25(1). Radio frequency oscillator 1A11A1/A14,A11, parts location and printed wiring diagram (part 4 of 4)



**NOTE:**

1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER, AND SUBASSEMBLY DESIGNATION.
2. ALL WIRE IS NO 26 AWG.

EL5820-695-35-TM-C1-12

Figure 4-26. Electronic frequency converter 1A14A2/2A14A2, wiring diagram.  
4-34 Change 1

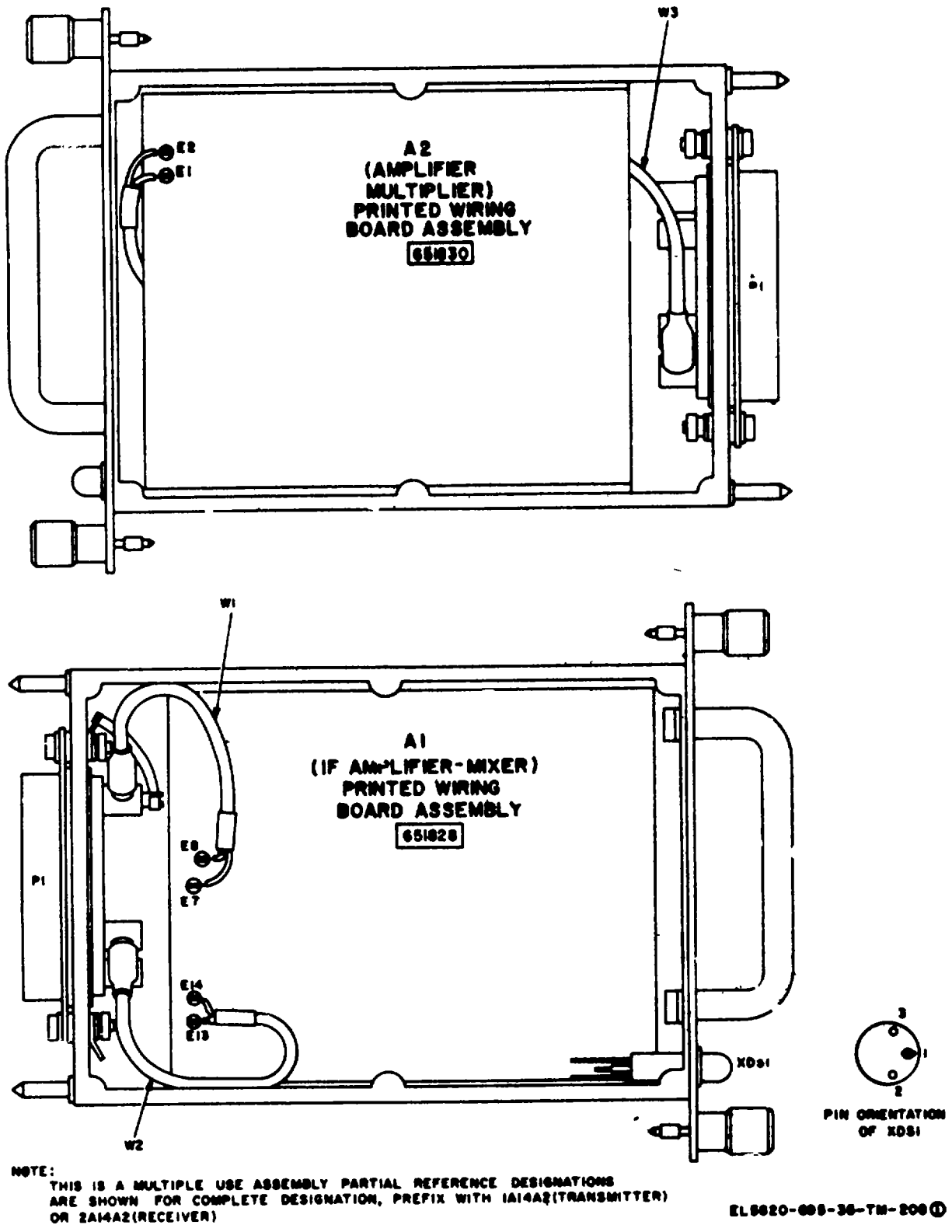
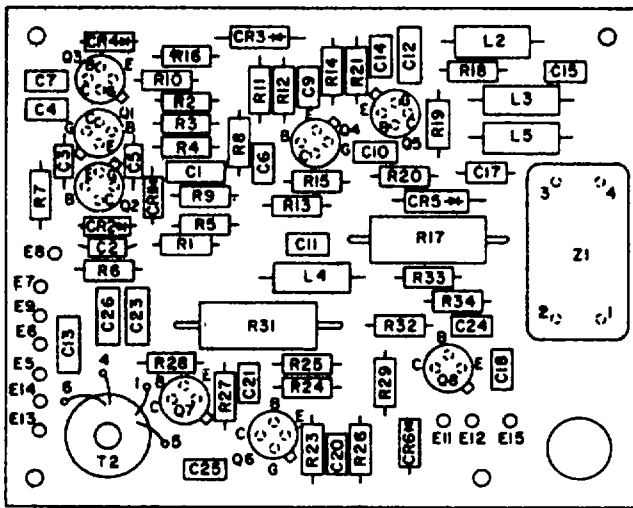
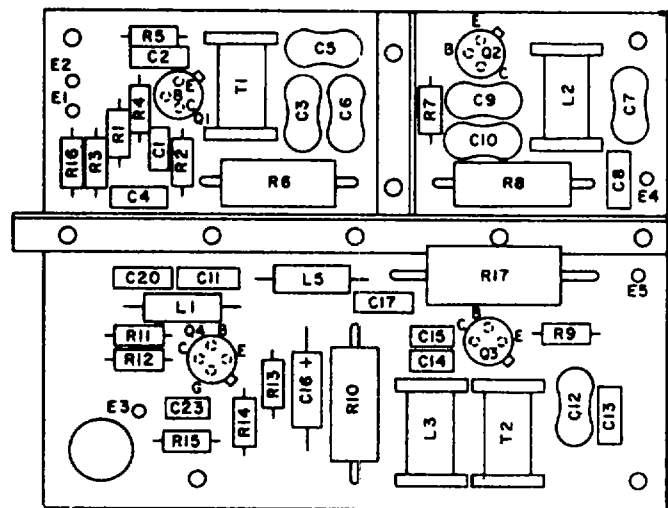


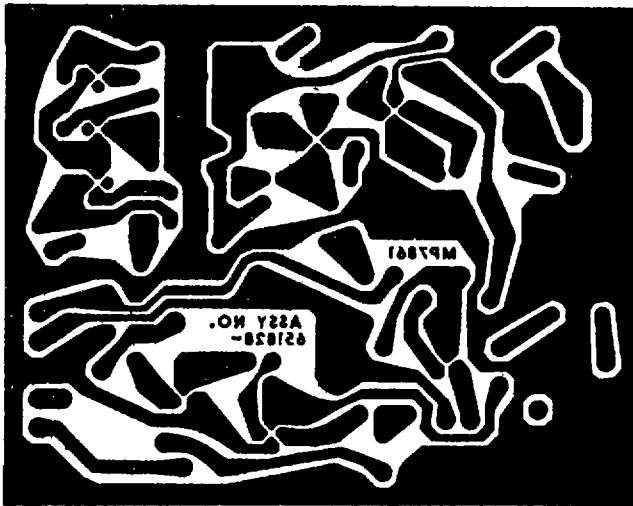
Figure 4-27(1). Electronic frequency converter 1A14A2/2A14A2, parts location and printed wiring diagram (part 1 of 2).



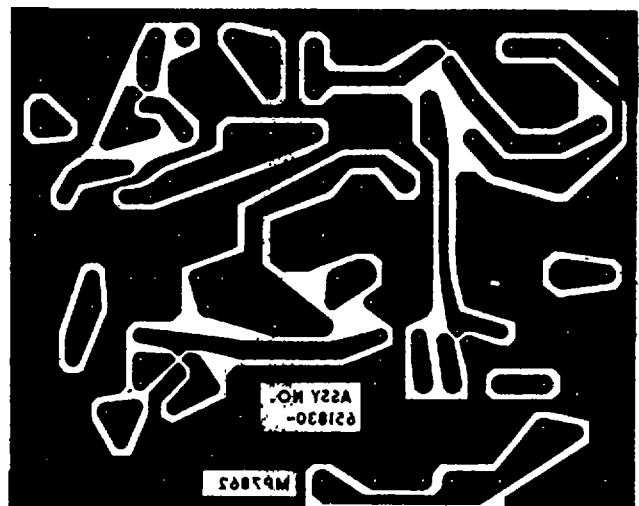
A. PARTS ON FRONT OF BOARD A1  
(SEE NOTE 2)



B. PARTS ON FRONT OF BOARD A2



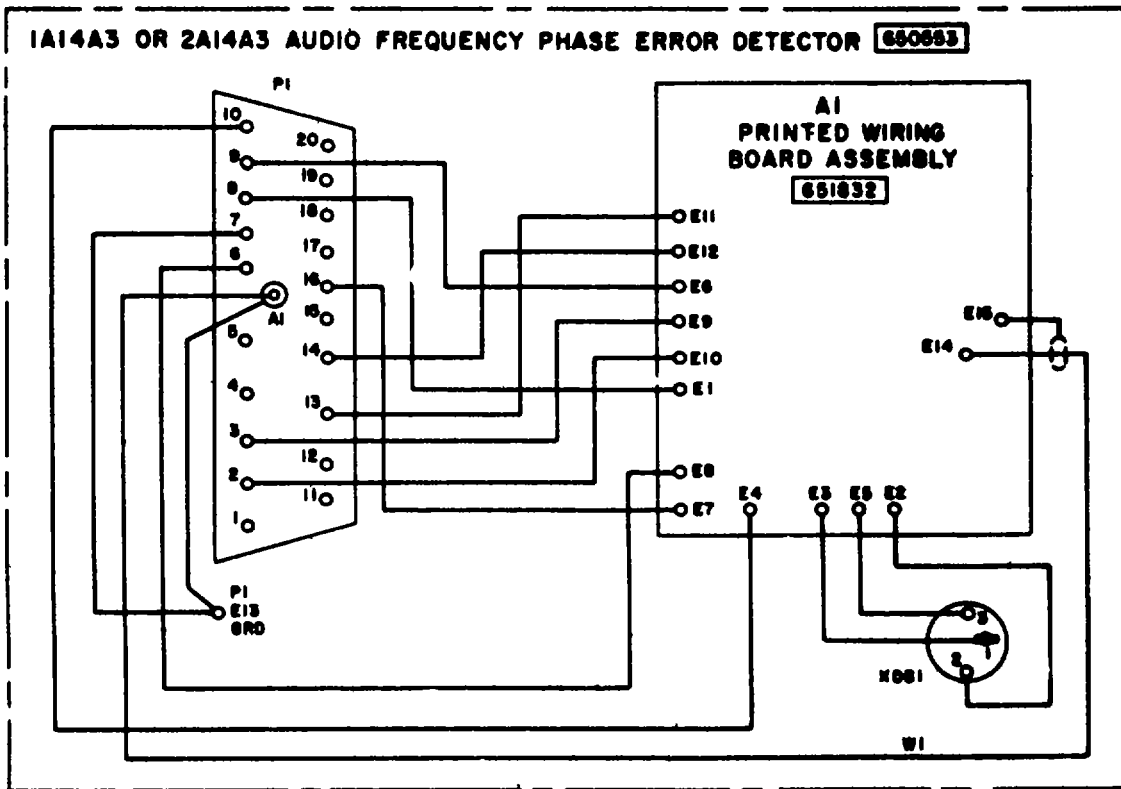
C. WIRING ON BACK OF BOARD A1  
(VIEWED THROUGH FRONT)  
(SEE NOTE 2)



D. WIRING ON BACK OF BOARD A2  
(VIEWED THROUGH FRONT)

EL5820-695-35-TM-CI-13 (2)

Figure 4-27(2). Electronic frequency converter 1A14A2/2A14A2, parts location and printed wiring diagram (part 2 of 2).

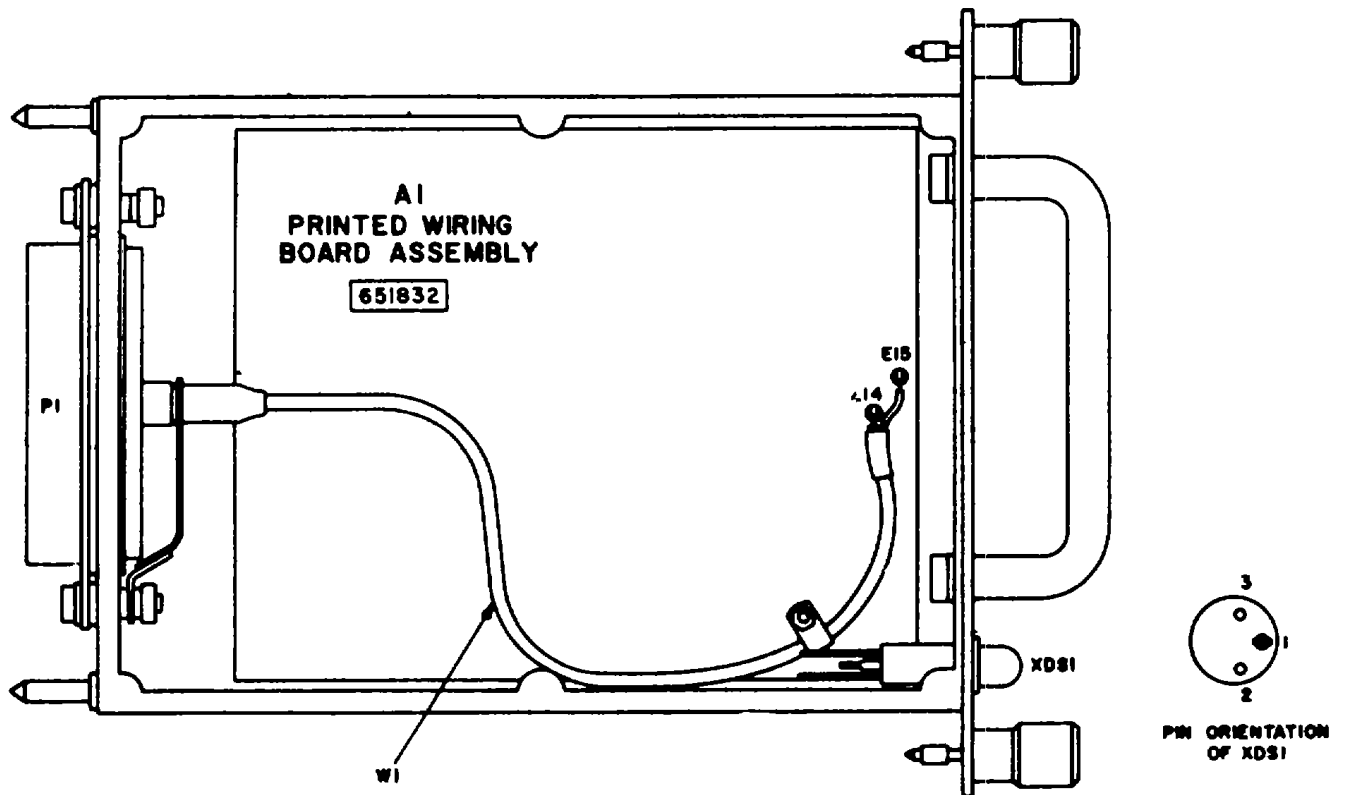


**NOTE:**

1. THIS IS A MULTIPLE USE ASSEMBLY PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER, AND SUBASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 26 AWG.

EL6820-695-35-TM-CI-14

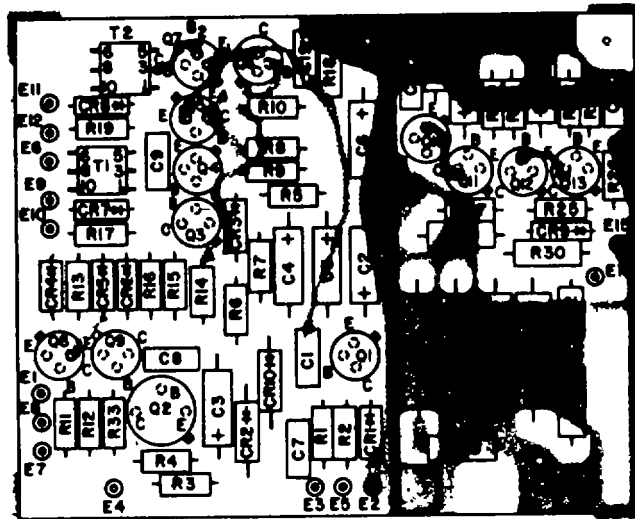
Figure 4-28. Audio frequency phase error detector 1A14A3/2A14A3, wiring diagram.  
Change 1 4-37



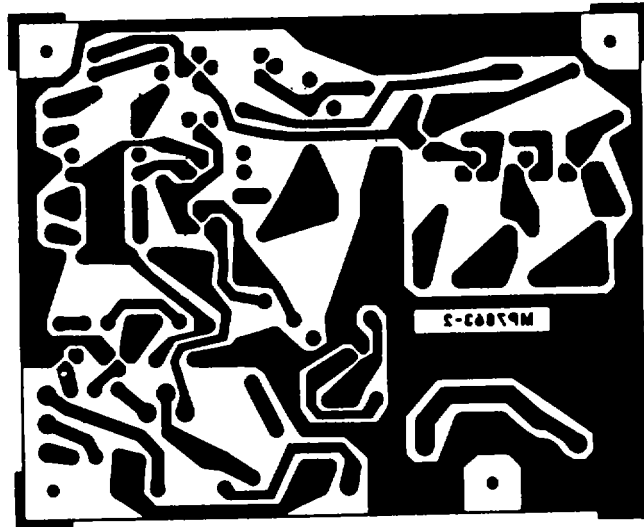
**NOTE:**  
 THIS IS A MULTIPLE USE ASSEMBLY.  
 PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN FOR COMPLETE DESIGNATION,  
 PREFIX WITH 1A14A3 (T-1054/GRC-144) OR  
 2A14A3 (R-1467/GRC-144).

EL5820-695-35-TM-210 ①

Figure 4-29(1). Audio frequency phase error detector 1A14A3/2A14A3, parts location and printed wiring diagram (part 1 of 2).



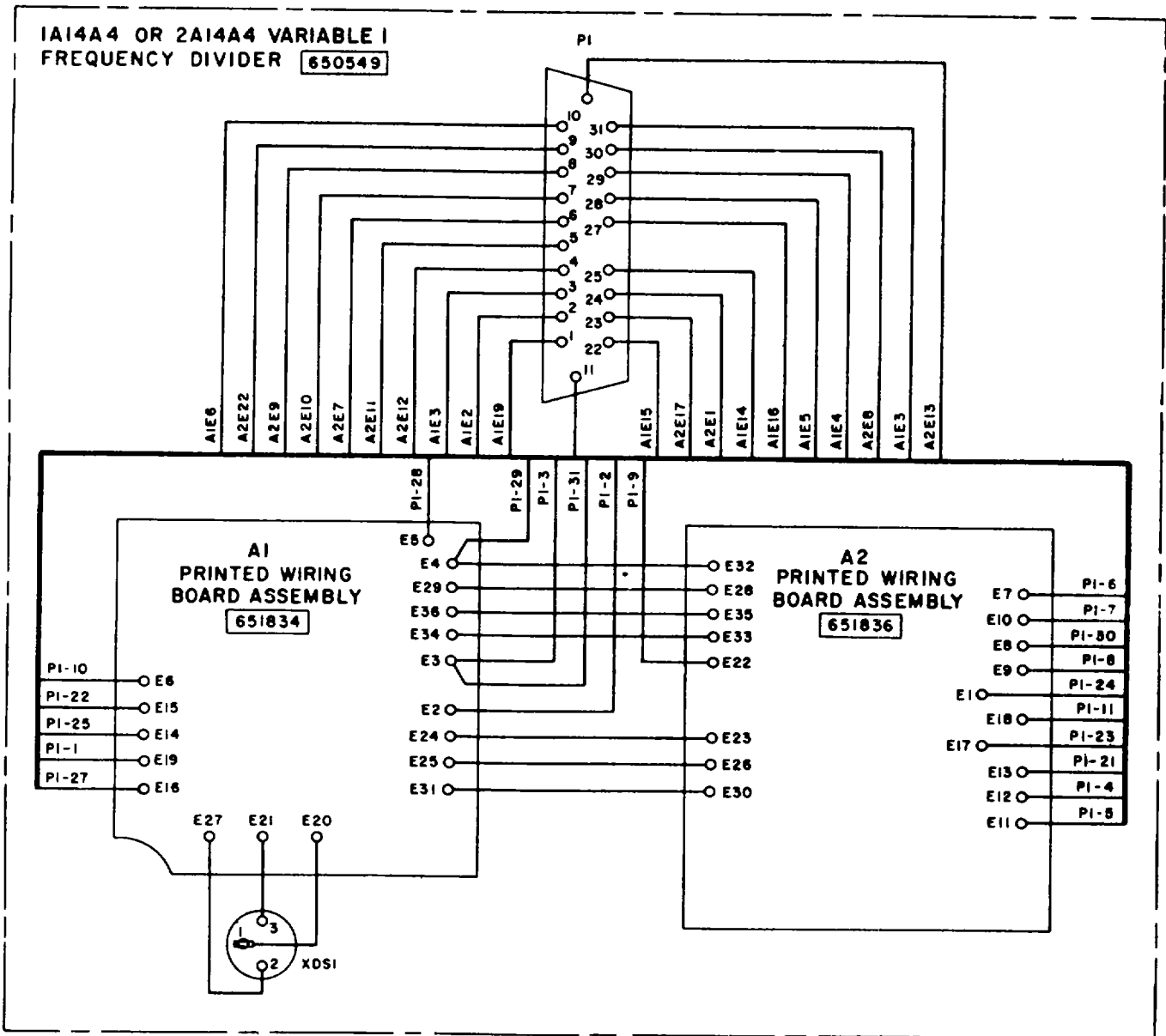
A. PARTS AND WIRING ON FRONT OF BOARD A1



B. WIRING ON BACK OF BOARD A1  
(VIEWED THROUGH FRONT)

EL5820-695-35-TM-210 ②

Figure 4-29(1). Audio frequency phase error detector 1A14A3/2A14A3, parts location and printed wiring diagram (part 2 of 2).



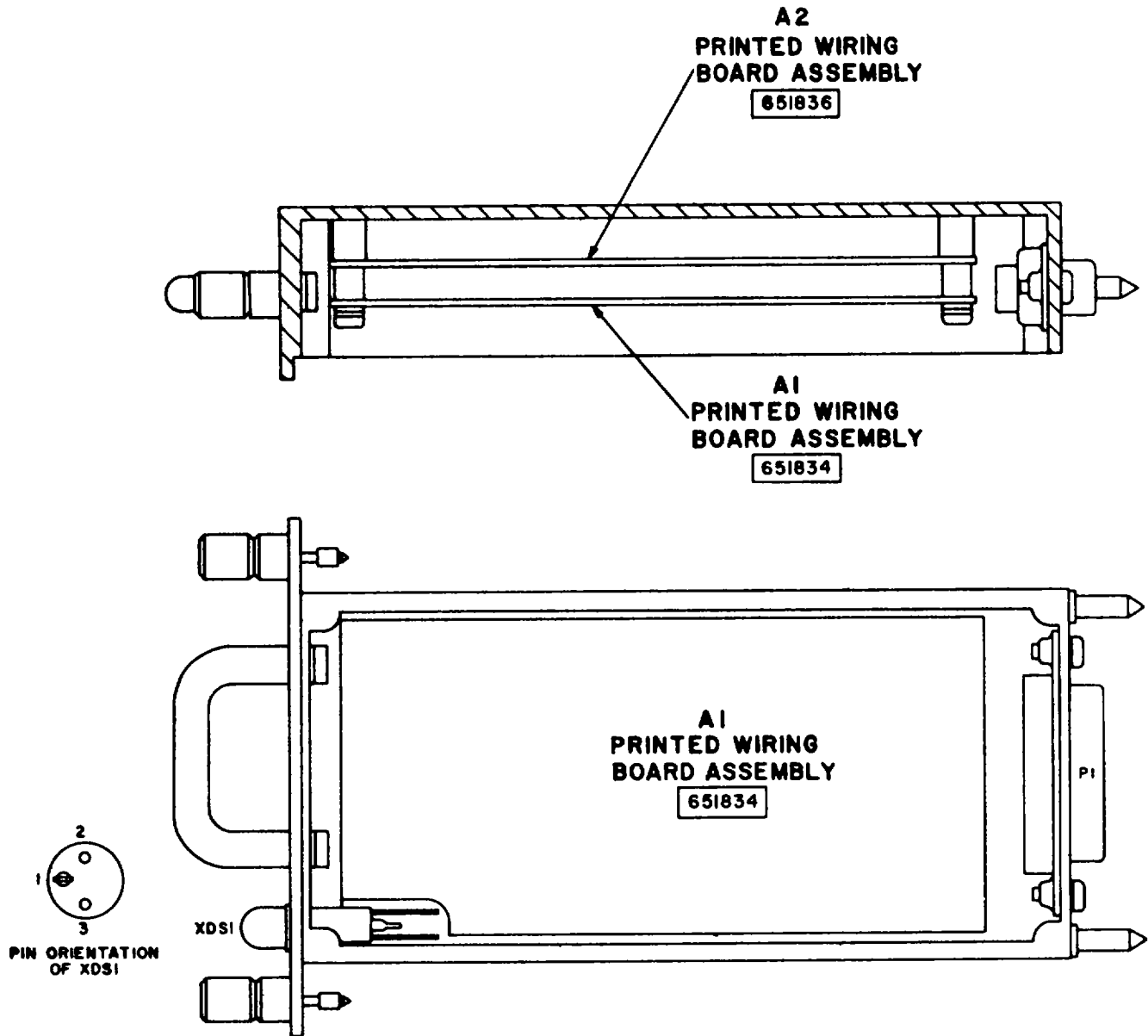
**NOTE**

- 1 THIS IS A MULTIPLE USE ASSEMBLY  
PARTIAL REFERENCE DESIGNATIONS  
ARE SHOWN FOR COMPLETE DESIGNATION,  
PREFIX WITH UNIT, UNIT NUMBER, AND  
SUBASSEMBLY DESIGNATION
- 2 ALL WIRE IS NO 26 AWG

EL5820-695-35-TM-211

Figure 4-30. Variable 1 frequency divider 1A14A4/2A14A44, wiring diagram.



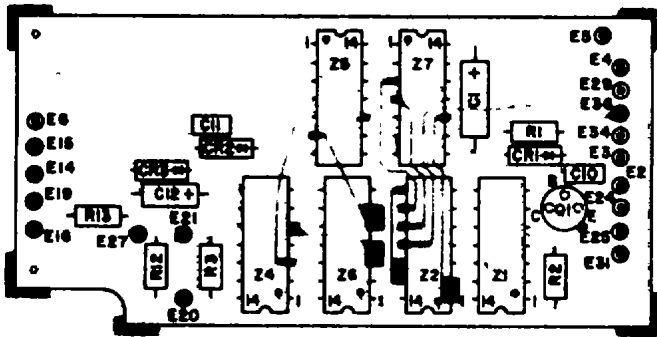


**NOTE**

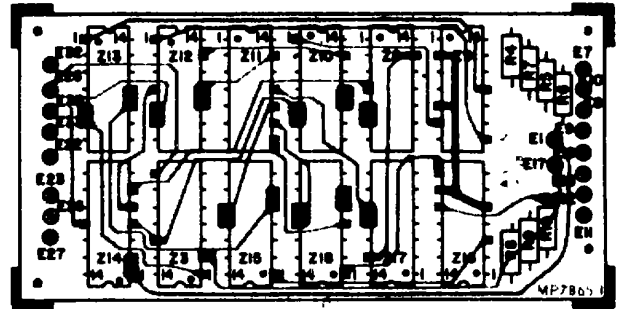
THIS IS A MULTIPLE USE ASSEMBLY  
 PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN FOR COMPLETE DESIGNATION,  
 PREFIX WITH 1A14A4 (TRANSMITTER) OR  
 2A14A4 (RECEIVER) AND SUBASSEMBLY DESIGNATION.

EL5820-695-35-TM-212 (1)

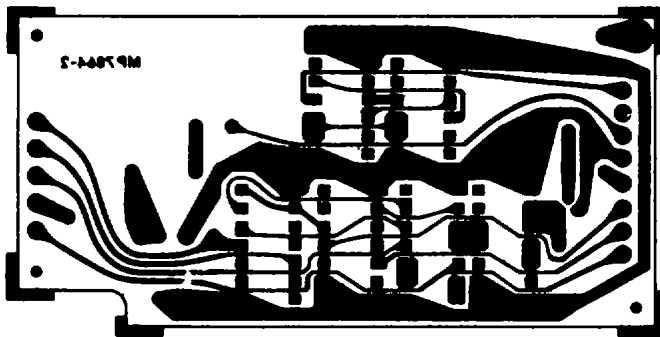
Figure 4-31(1). Variable 1 frequency divider 1A14A4/2A14A4, parts location and printed wiring diagram (part 1 of 3).



A. PARTS AND WIRING ON FRONT OF BOARD A1

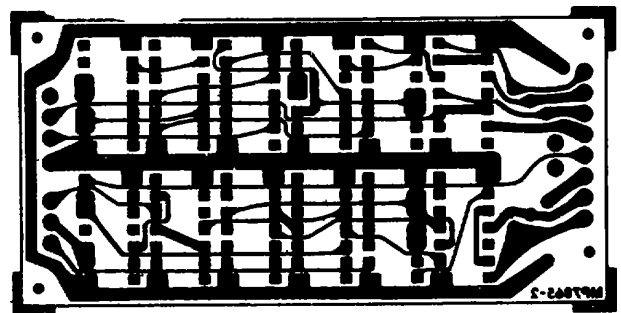


A. PARTS AND WIRING ON FRONT OF BOARD A2



B. WIRING ON BACK OF BOARD A1  
(VIEWED THROUGH FRONT)

EL5820-695-35-TM-212 ②

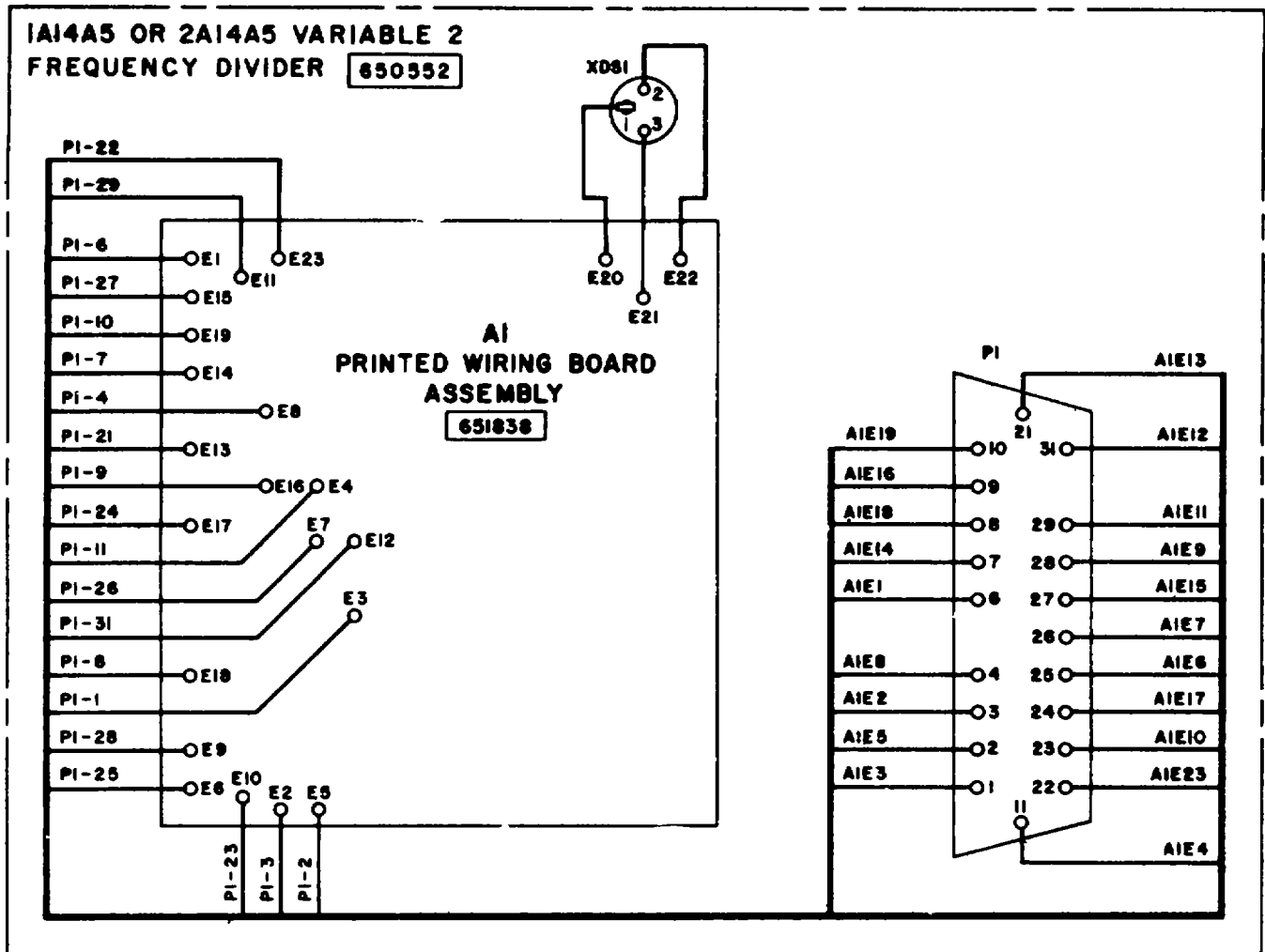


B. WIRING ON BACK OF BOARD A2  
(VIEWED THROUGH FRONT)

EL5820-695-35-TM-212 ③

Figure 4-31(2). Variable 1 frequency divider 1A14A4/2A14A4, parts location and printed wiring diagram (part 2 of 3).

Figure 4-31(2). Variable 1 frequency divider 1A14A4/2A14A4, parts location and printed wiring diagram (part 3 of 3).

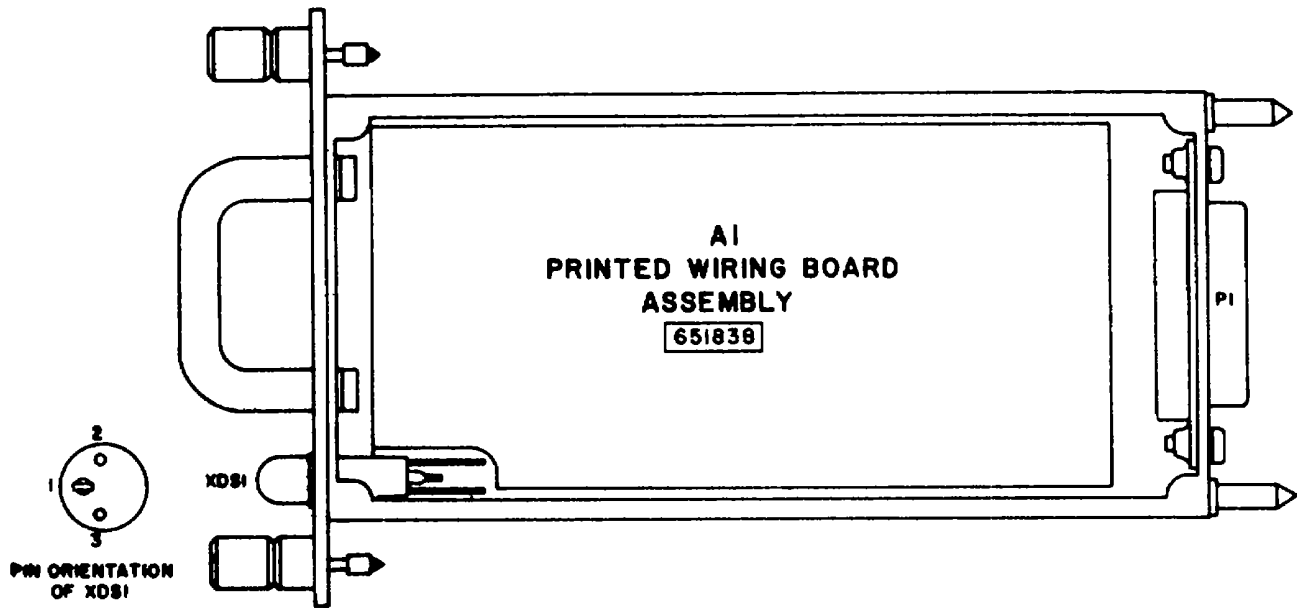


**NOTES:**

1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS, PREFIX WITH 1A14A5 (T-1054/GRC-144) OR 2A14A5 (R-1487/GRC-144) AND SUBASSEMBLY DESIGNATION.
2. ALL WIRE IS NO 26 AWG.

EL5820-695-35-TM-213

Figure 4-32. Variable 2 frequency divider 1A14A5/2A14A5, wiring diagram.

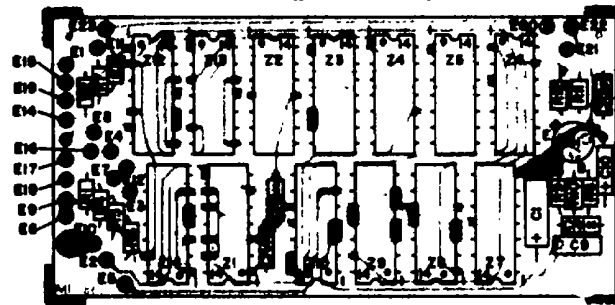


**NOTE.**

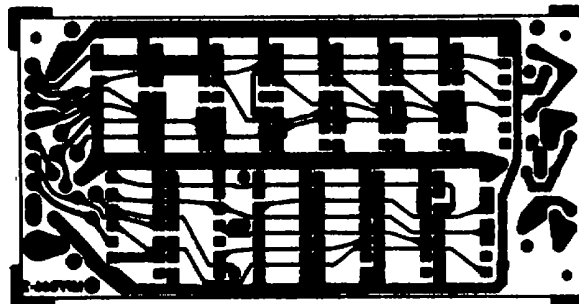
THIS IS A MULTIPLE USE ASSEMBLY.  
 PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN. FOR COMPLETE DESIGNATION,  
 PREFIX WITH 1A14A5 (T-1054/GRC-144) OR  
 2A14A5 (R-1467/BRC-144).

EL5820-695-35-TM-214 ①

Figure 4-32 (1). Variable 2 frequency divider 1A14A5/  
 2A14A5, parts location and printed wiring diagram  
 (part 1 of 2)



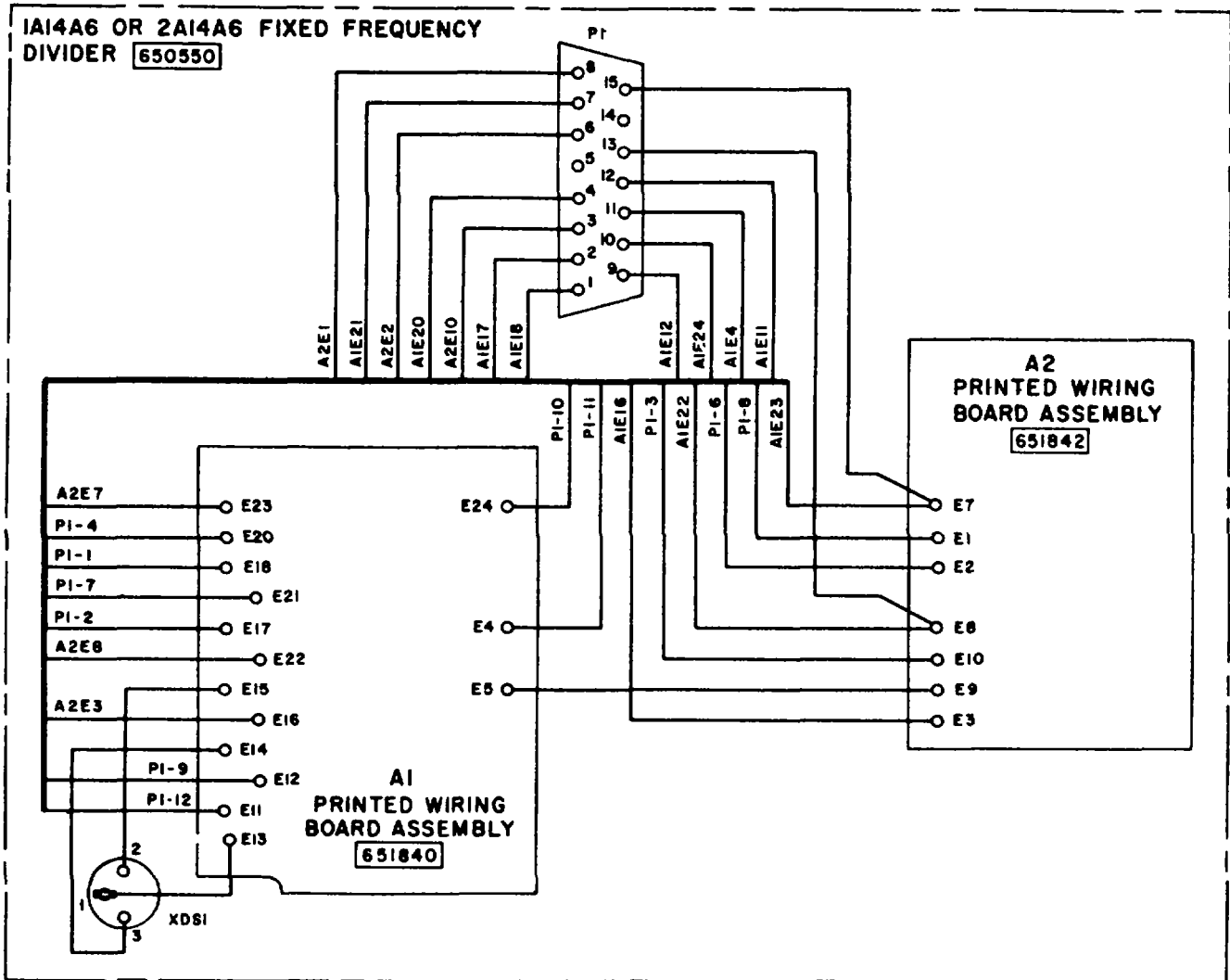
A. PARTS AND WIRING ON FRONT OF BOARD A1



B. WIRING ON BACK OF BOARD A1  
 (VIEWED THROUGH FRONT)

EL5820-695-35-TM-214 ②

Figure 4-33 (2). Variable 2 frequency divider 1A14A5/  
 2A14A5, parts location and printed wiring diagram  
 (part 2 of 2)

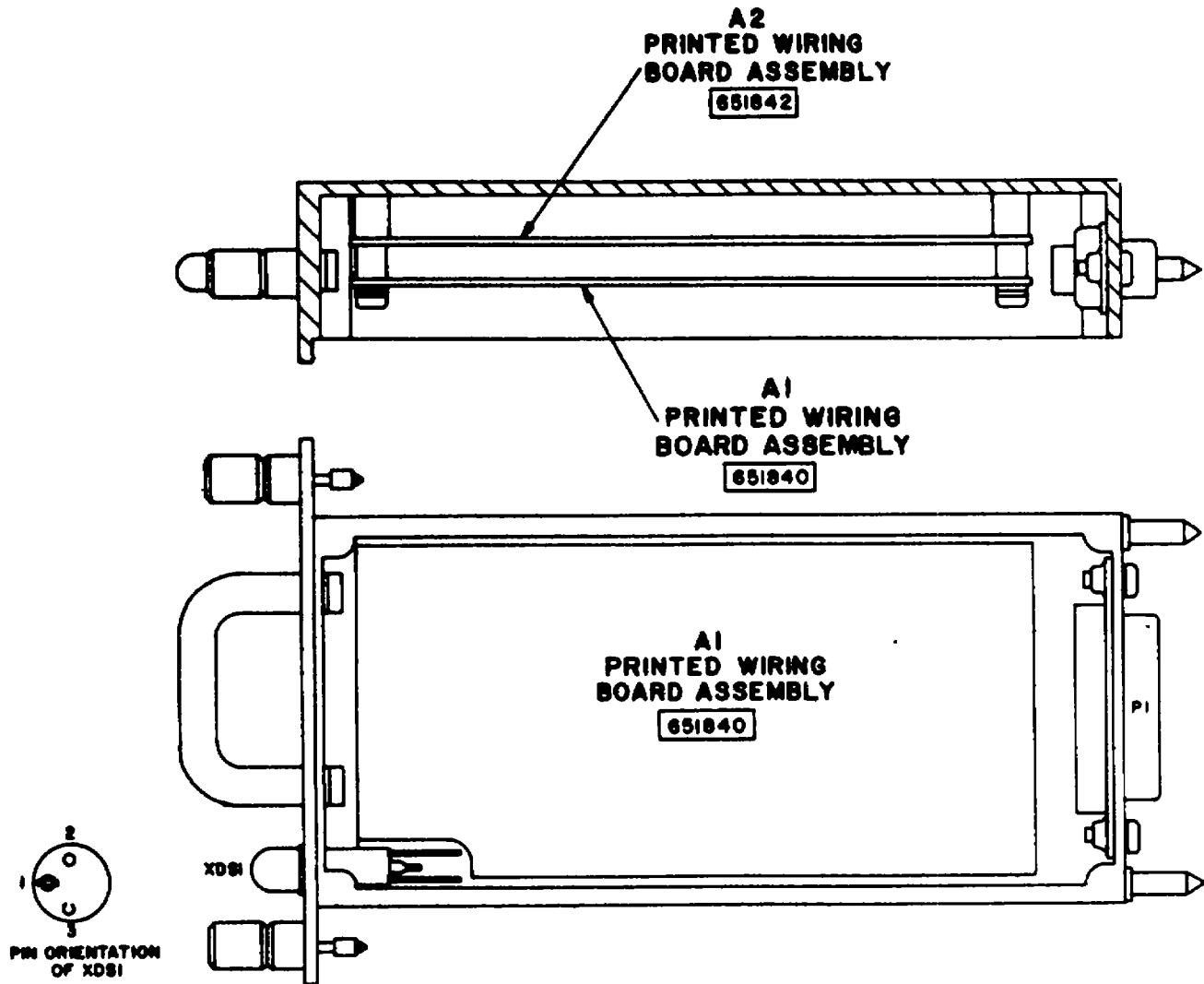


**NOTE**

1. THIS IS A MULTIPLE USE ASSEMBLY  
PARTIAL REFERENCE DESIGNATIONS  
ARE SHOWN FOR COMPLETE DESIGNATION.  
PREFIX WITH 1A14A6 (T-1054/GRC-144) OR  
2A14A6 (R-1467/GRC-144) AND SUBASSEMBLY DESIGNATION.
2. ALL WIRE IS NO 26 AWG

EL5820-695-35-TM-215

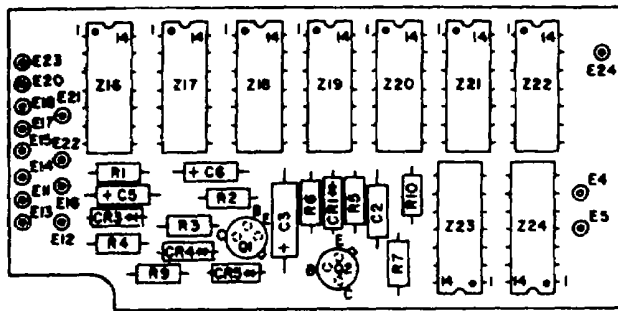
Figure 4-34. Fixed frequency divider 1A14A6/2A14A6, wiring diagram.



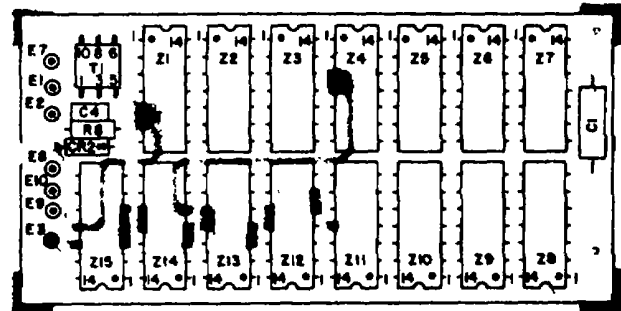
**NOTE:**  
 THIS IS A MULTIPLE USE ASSEMBLY  
 PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN. FOR COMPLETE DESIGNATION,  
 PREFIX WITH 1A14A6 (T-1054/8RC-144) OR  
 2A14A6 (R-1487/8RC-144) AND SUBASSEMBLY DESIGNATION.

EL5820-695-35-TM-216 ①

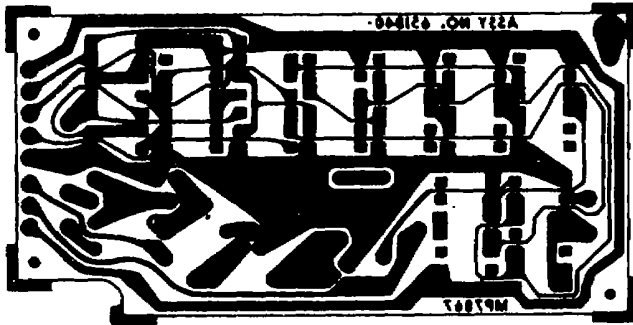
Figure 4-35 (1). Fixed frequency divider 1A14A6/2A14A6, parts location and printed wiring diagram (part 1 of 3).



A. PARTS ON FRONT OF BOARD A1

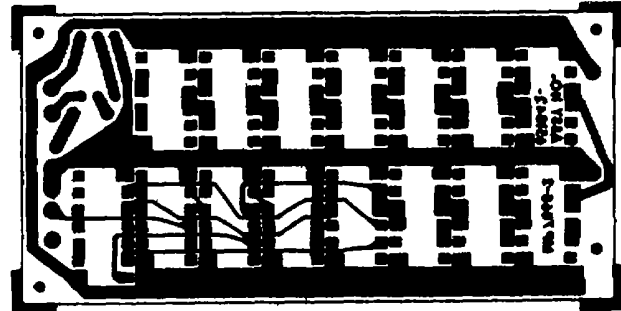


A. PARTS AND WIRING ON FRONT OF BOARD A2.



B. WIRING ON BACK OF BOARD A1  
(VIEWED THROUGH FRONT)

EL5820-695-35-TM-216 ②

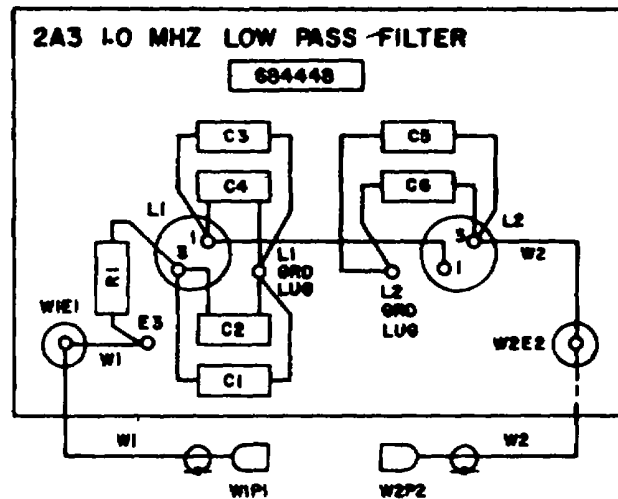


B. WIRING ON BACK OF BOARD A2  
(VIEWED THROUGH FRONT)

EL5820-695-35-TM-216 ③

Figure 4-35 (2). Fixed frequency divider 1A14A6/2A14A6, parts location and printed wiring diagram (part 2 of 3).

Figure 4-35 (3). Fixed frequency divider 1A14A6/2A14A6, parts location and printed wiring diagram (part 3 of 3).



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 2A3.

2. WIRING IS NO. 22 AWG STRANDED WIRE, TEFLON INSULATED, EXCEPT CABLES W1 AND W2.

EL5820-695-35-TM-217

Figure 4-36. 1.0 MHz low pass filter 2AS, wiring diagram.

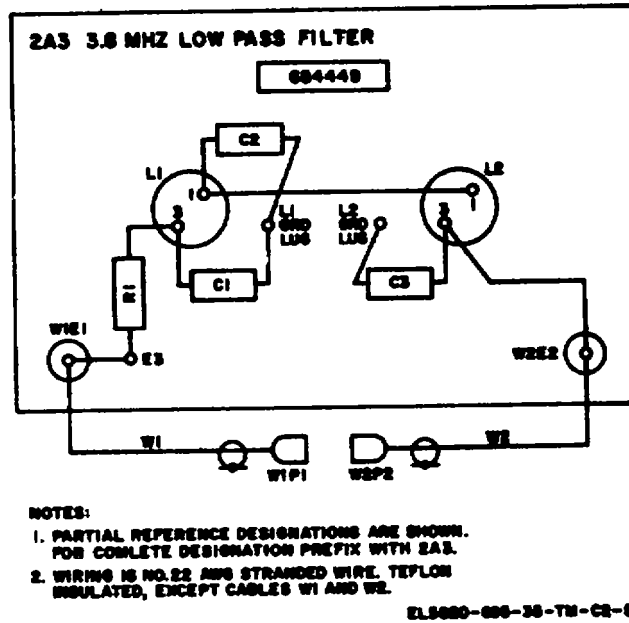
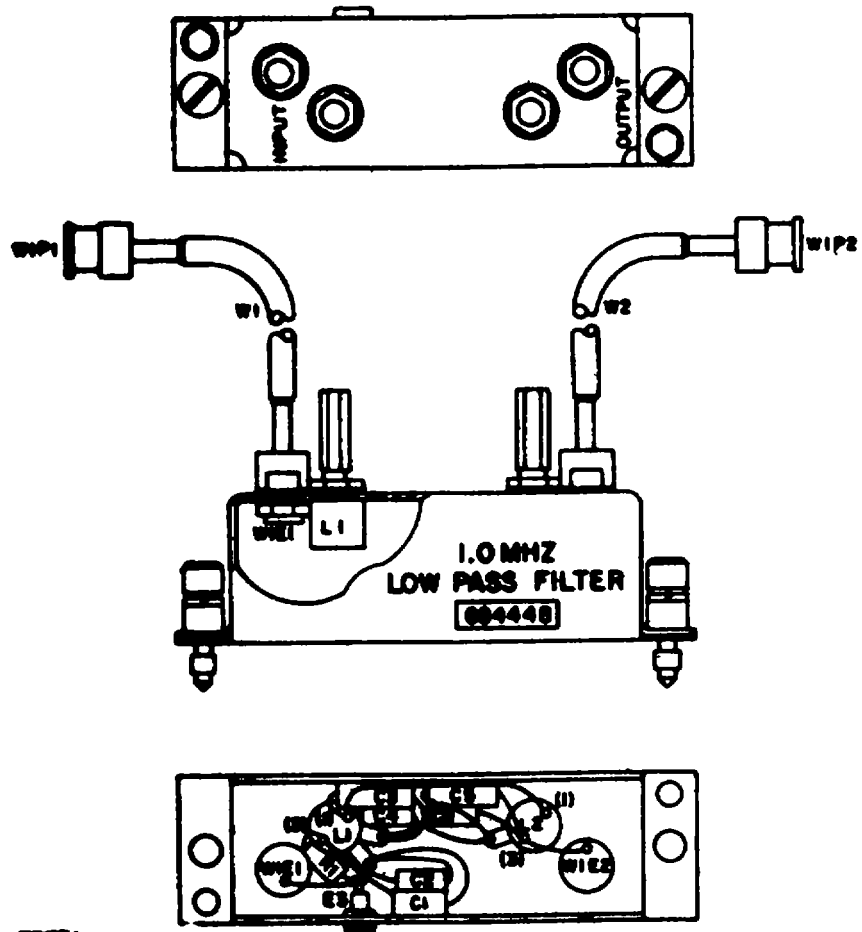


Figure 4-36.1. 3.8 MHz low pass filter 2A2, wiring diagram.

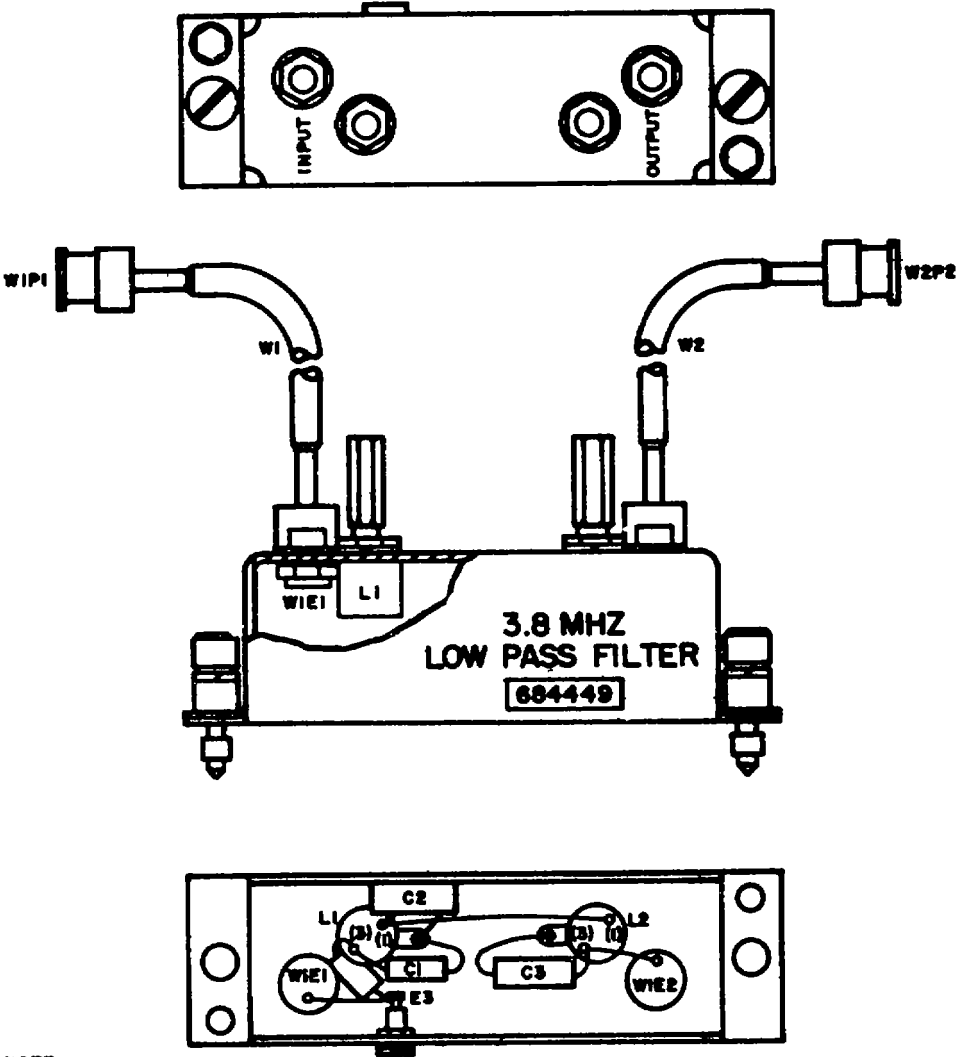




**NOTE:**  
PARTIAL REFERENCE DESIGNATIONS  
ARE SHOWN. FOR COMPLETE  
CORRELATION, PREFIX WITH 2A3.

EL9820-695-35-TM-218

Figure 4-37. 1.0 Mhz low pass filter 2A3, parts location.

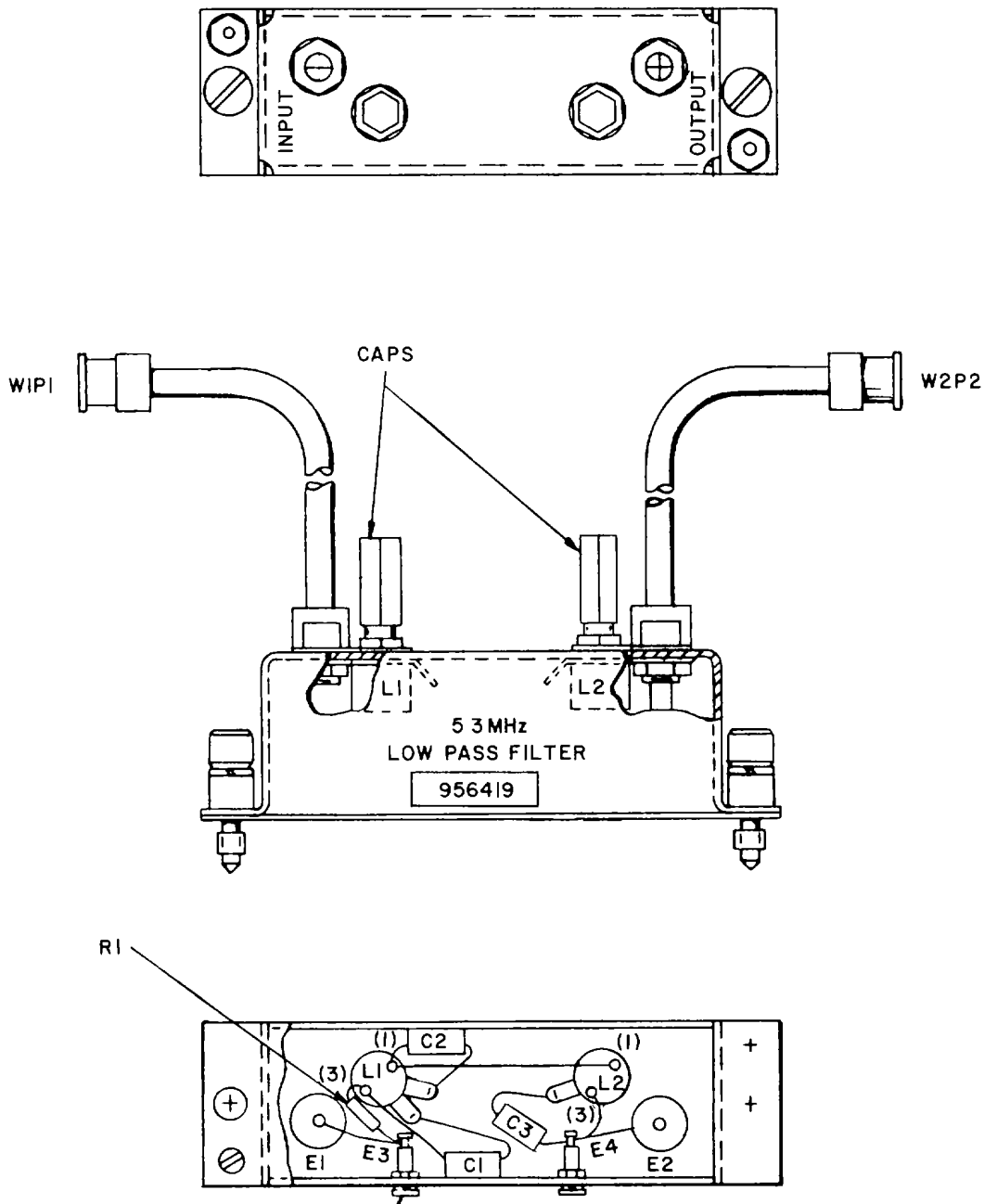


**NOTE:**  
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.  
FOR COMPLETE DESIGNATION PREFIX WITH 2A17.

EL5820-695-35-TM-C2-6

Figure 4-37.1. 3.8 MHz low pass filter 2A3, parts location.

4-48.2 Change 1

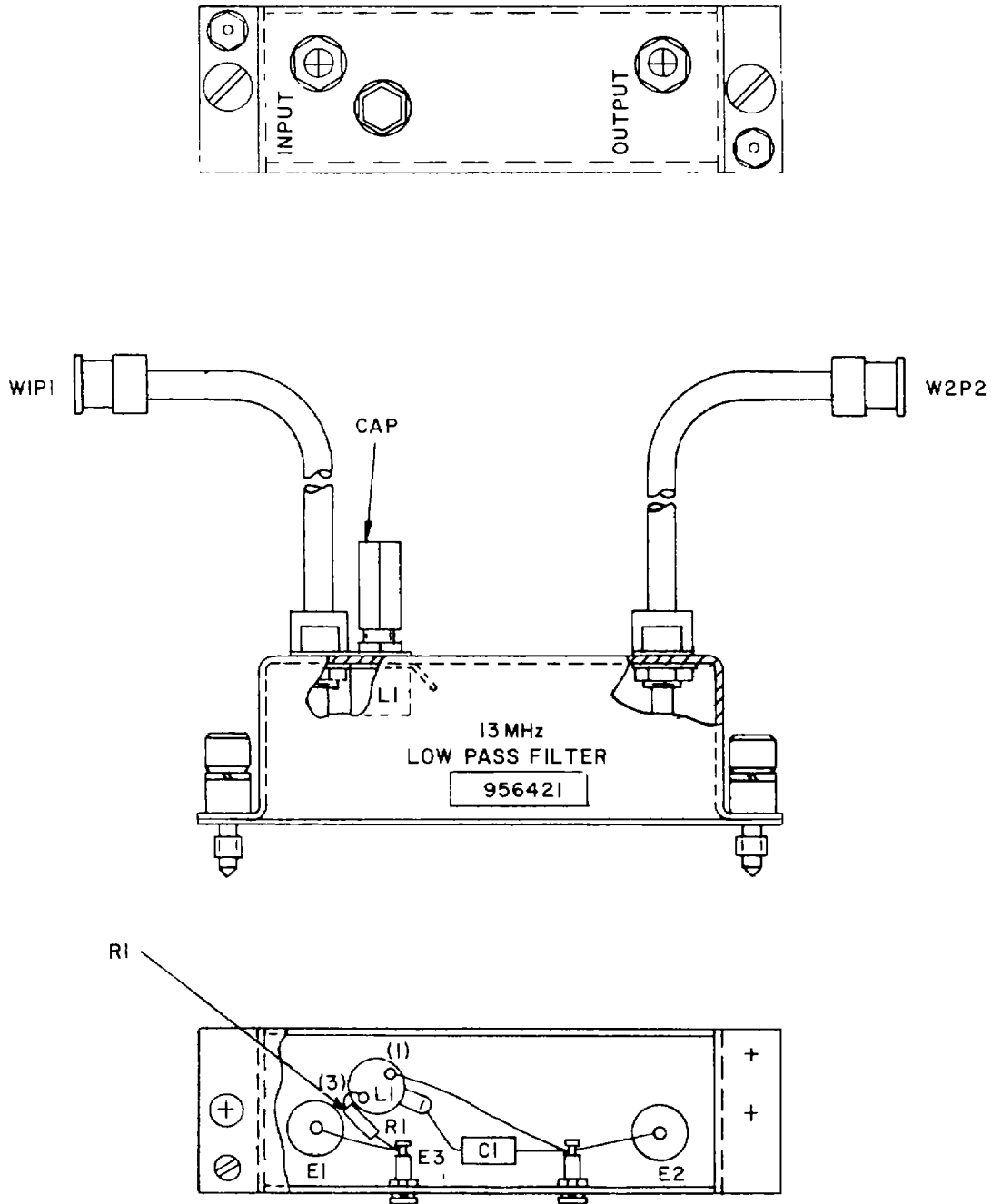


NOTE

PARTIAL REFERENCE DESIGNATION ARE SHOWN FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION

EL2IBIO5

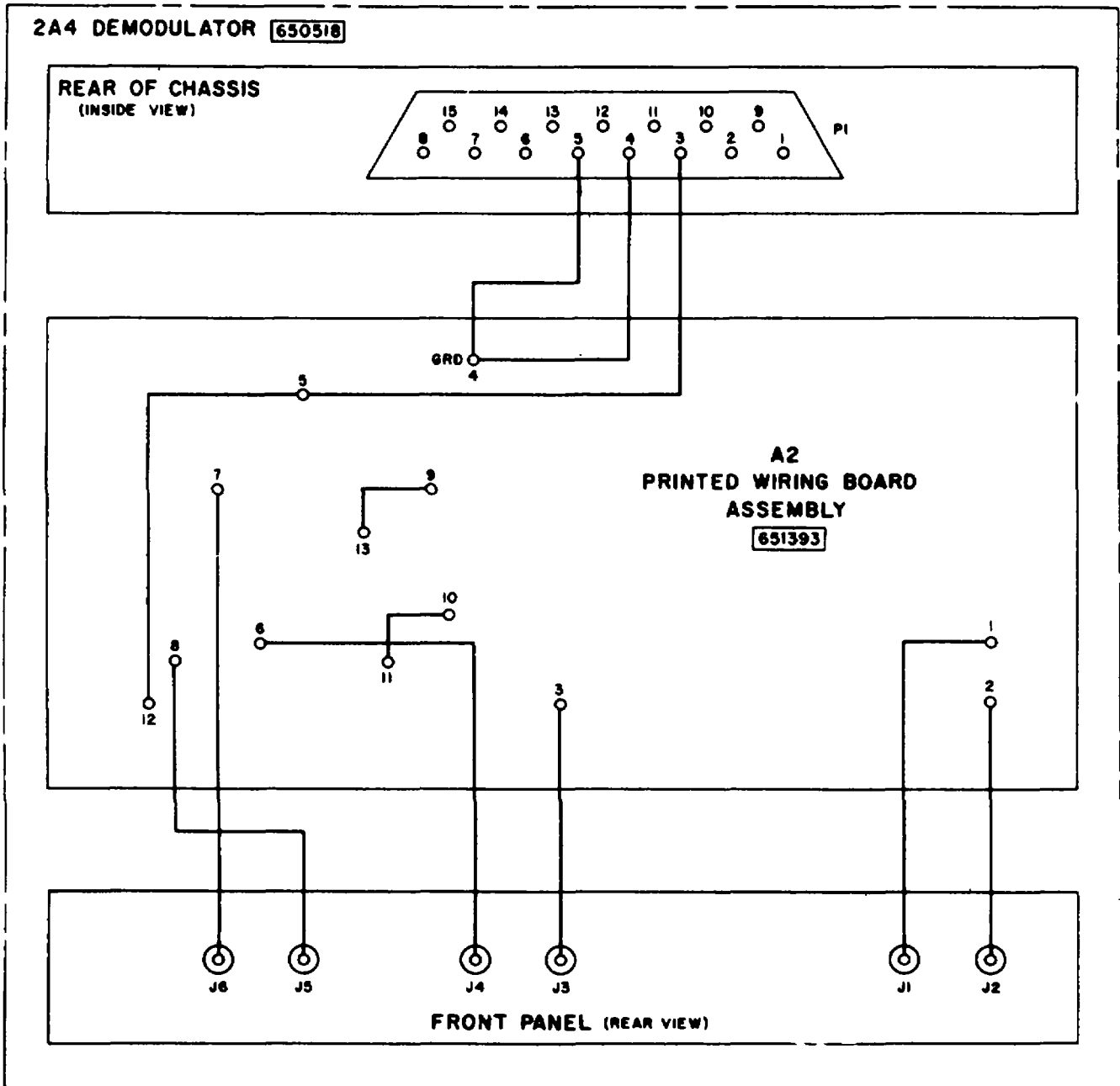
Figure 4-37.2. 5.3 MHz Low Pass Filter 2A3 (956419), Parts Location Diagram.



EL2IBI06

Figure 4-37.3. 13 MHz Low Pass Filter 2A3 (956421), Parts Location Diagram.

4-48.4 Change 6



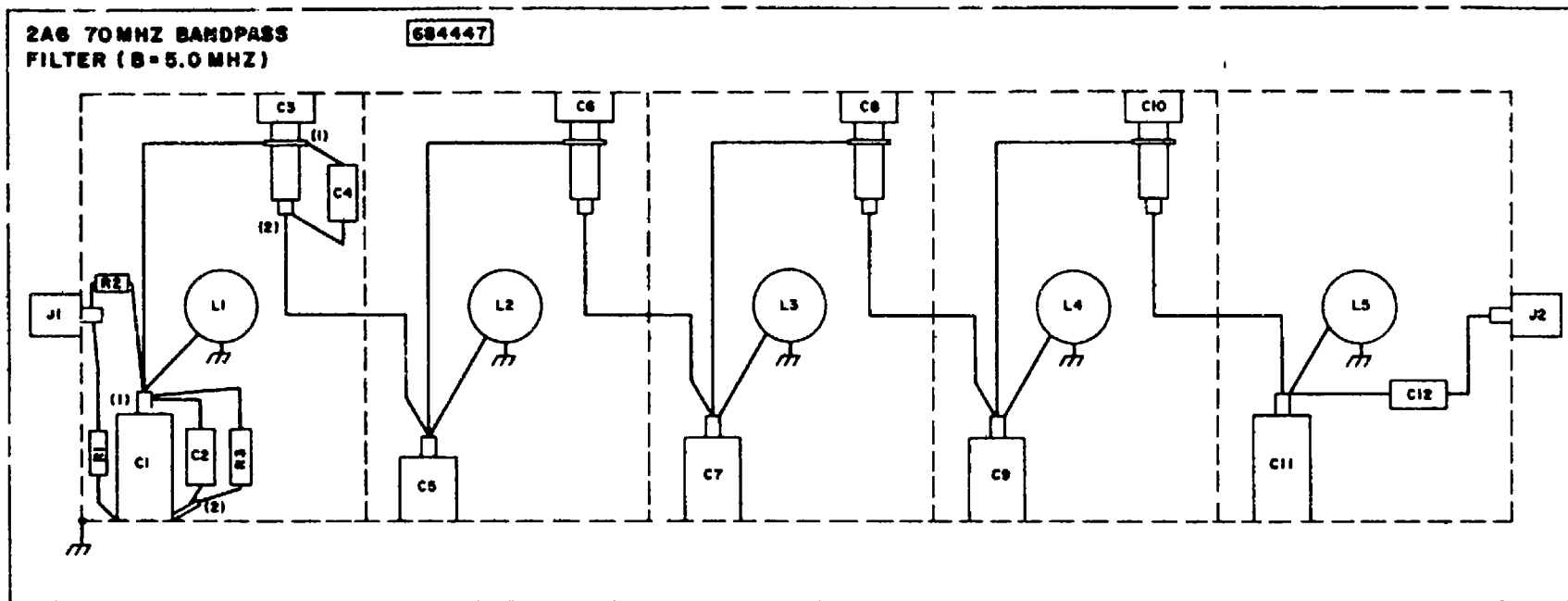
NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION.

2. ALL WIRE IS NO. 22 AWG STRANDED, TEFLON INSULATED.

EL5820-695-35-TM-219

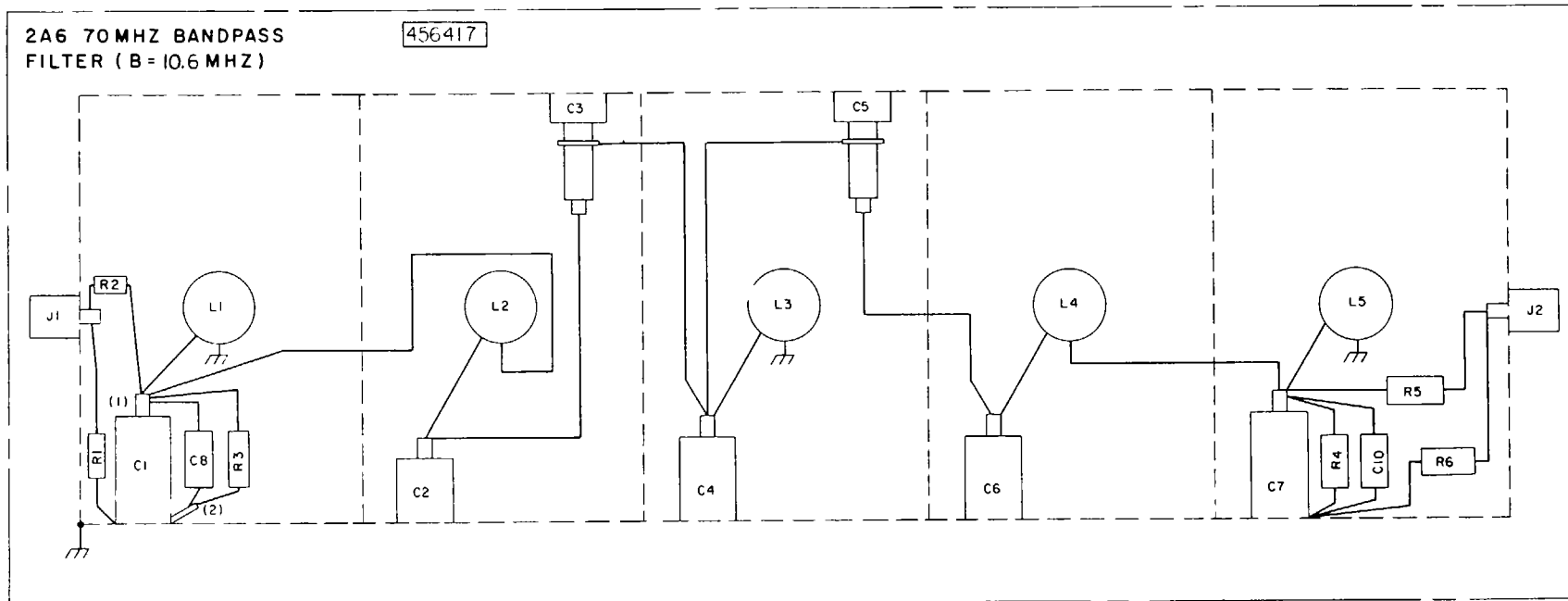
Figure 4-38. Demodulator 2A4, wiring diagram.



NOTE:  
 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.  
 FOR COMPLETE DESIGNATION PREFIX WITH 2A6.

EL 5820-695-35-TM-223

Figure 4-39. 70 MHz bandpass filter (B = 5.0 MHz 2A6, wiring diagram).



NOTE  
 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN  
 FOR COMPLETE DESIGNATION PREFIX WITH 2A6

Figure 4-39.1. 70 MHz Band Pass Filter (B=10.6 MHz) 2A6 (956417), Wiring Diagram.

Change 6 4-50.1

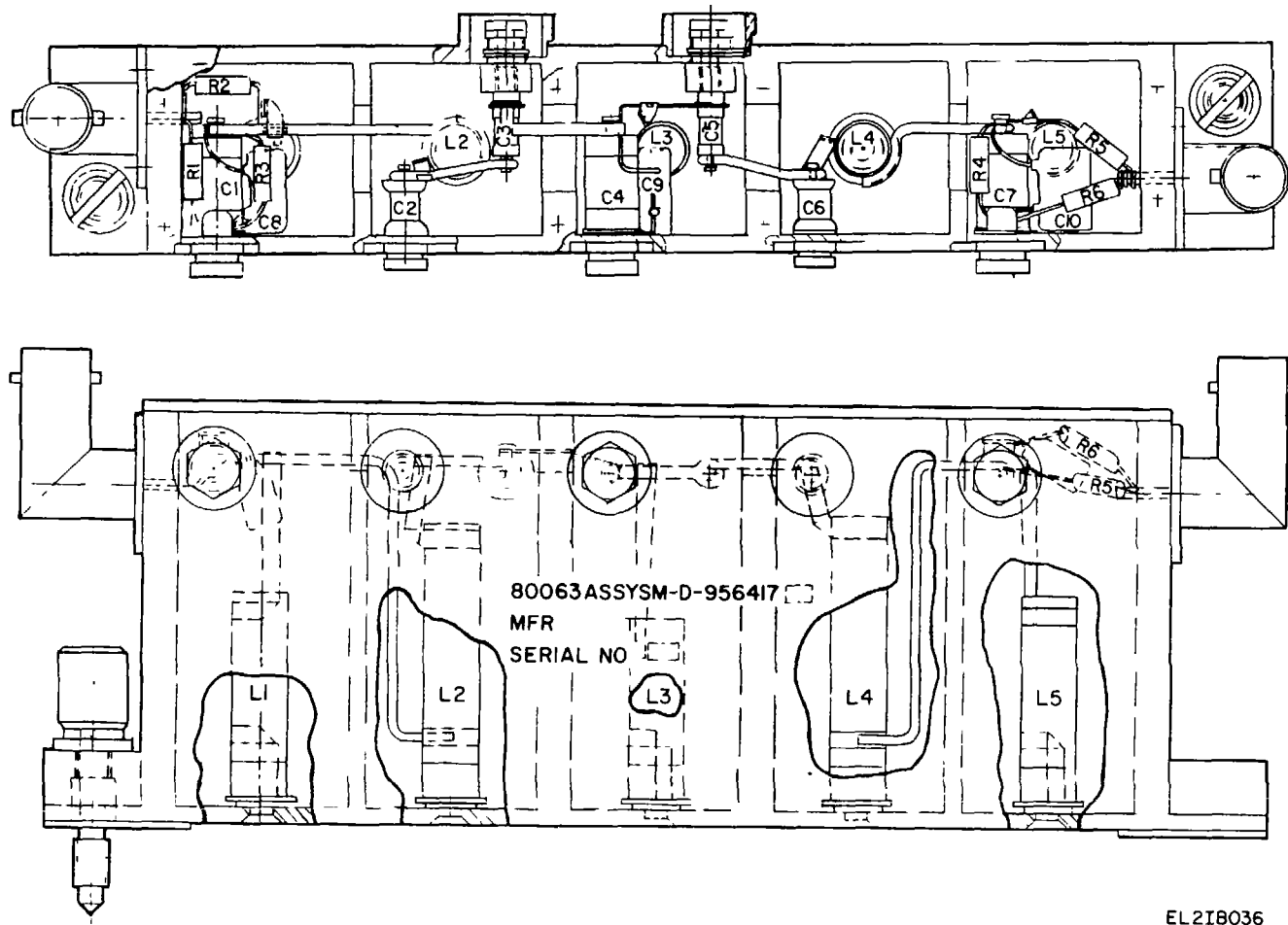
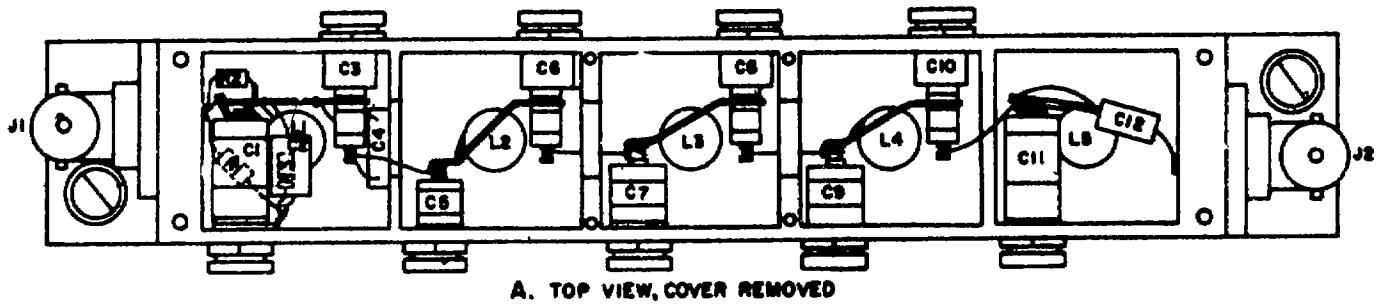


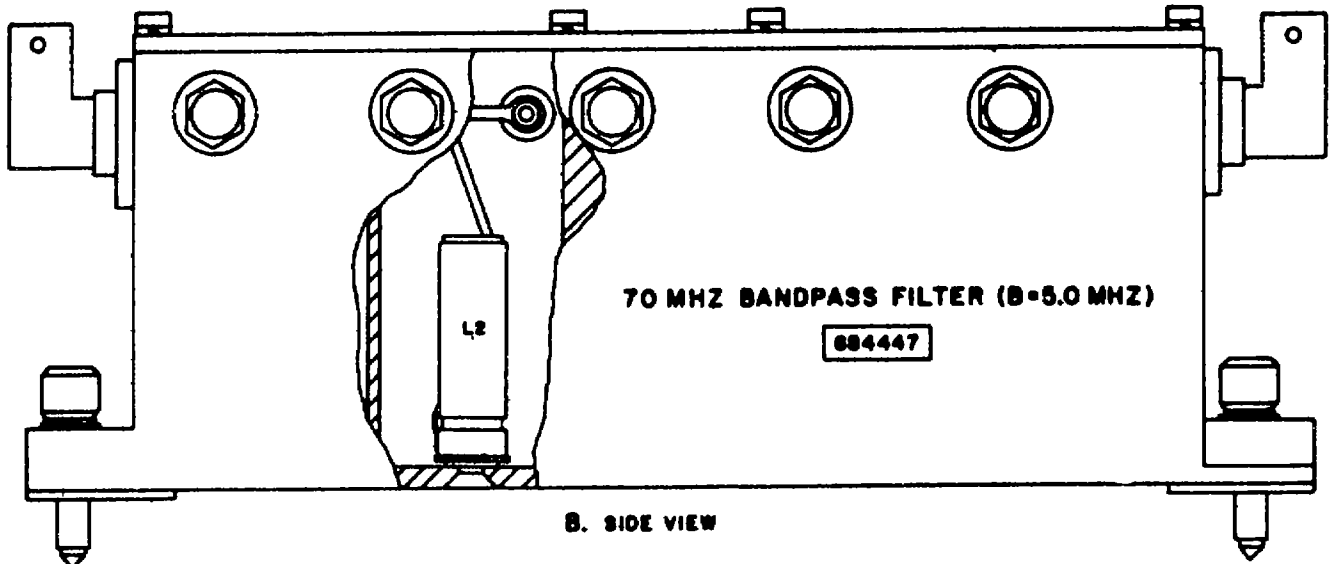
Figure 4-39.2. 70 MHz Band Pass Filter (B=10.6 MHz) 2A6 (956417), Parts Location Diagram.

4-50.2 Change 6





A. TOP VIEW, COVER REMOVED



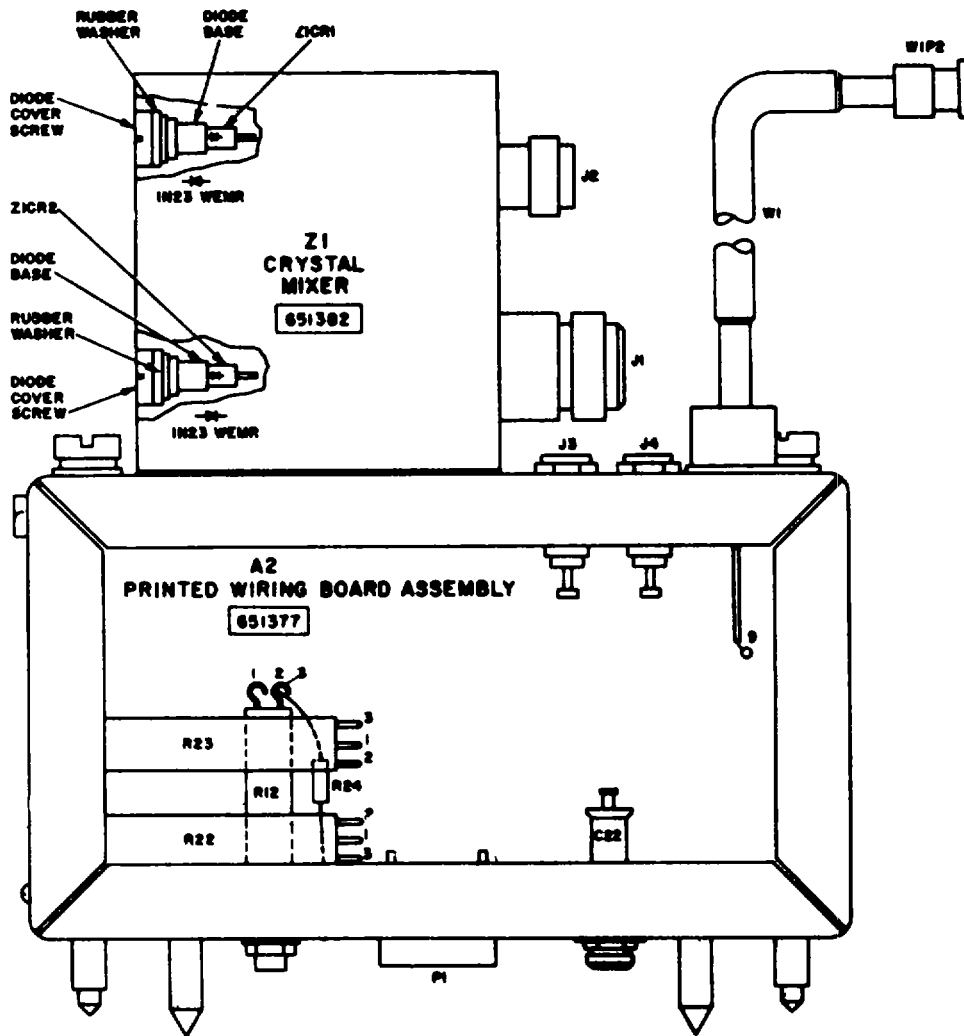
B. SIDE VIEW

**NOTE:**

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.  
FOR COMPLETE DESIGNATION, PREFIX WITH 2A6.

EL5920-695-35-TM-224

Figure 4-40. 70 MHz bandpass filter (B = 5.0 MHz) 2A6, parts location.

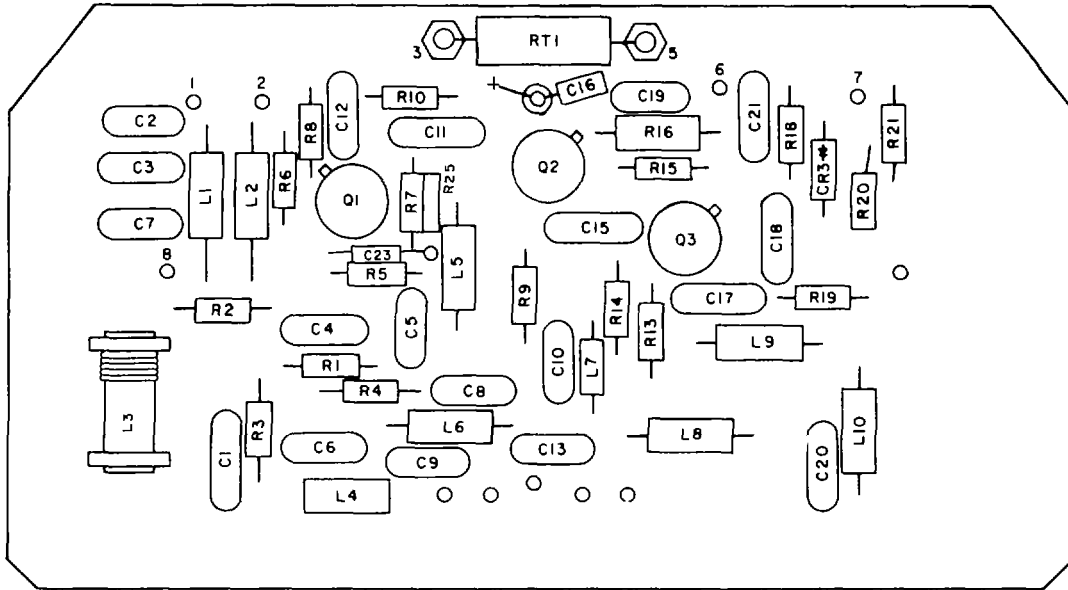


NOTE  
 PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN FOR COMPLETE DESIGNATION,  
 PREFIX WITH 2A7 AND  
 SUBASSEMBLY DESIGNATION.

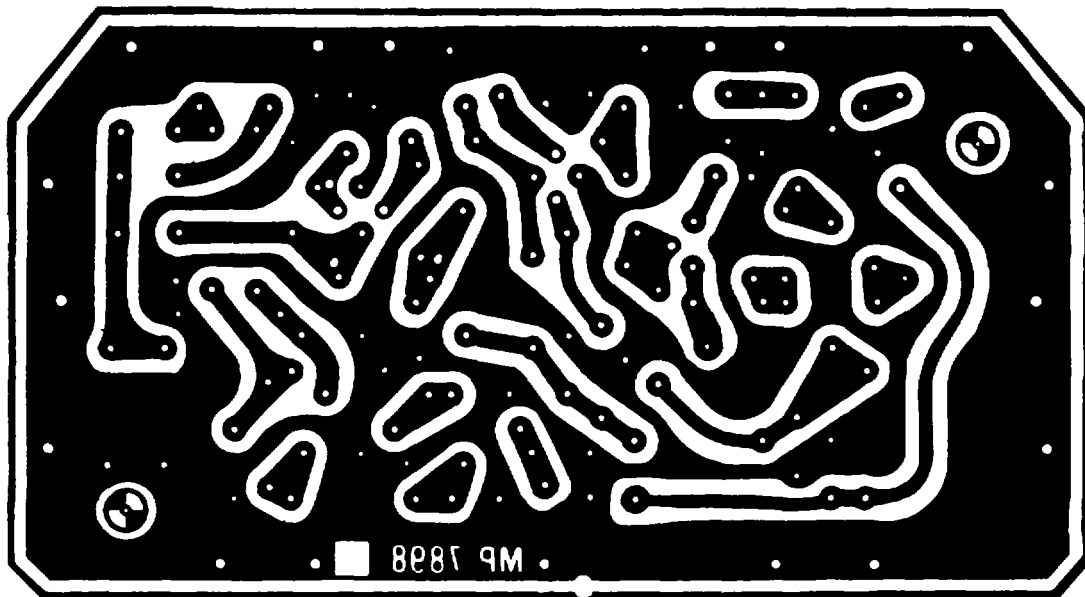
CL6820-695-35-TM-226 U

Figure 4-41 (1). Amplifier-mixer 2A7, parts location and printed wiring diagram (part 1 of 2).

NOTE  
 PARTIAL REFERENCE DESIGNATIONS ARE  
 SHOWN. FOR COMPLETE DESIGNATION,  
 PREFIX WITH 2A7



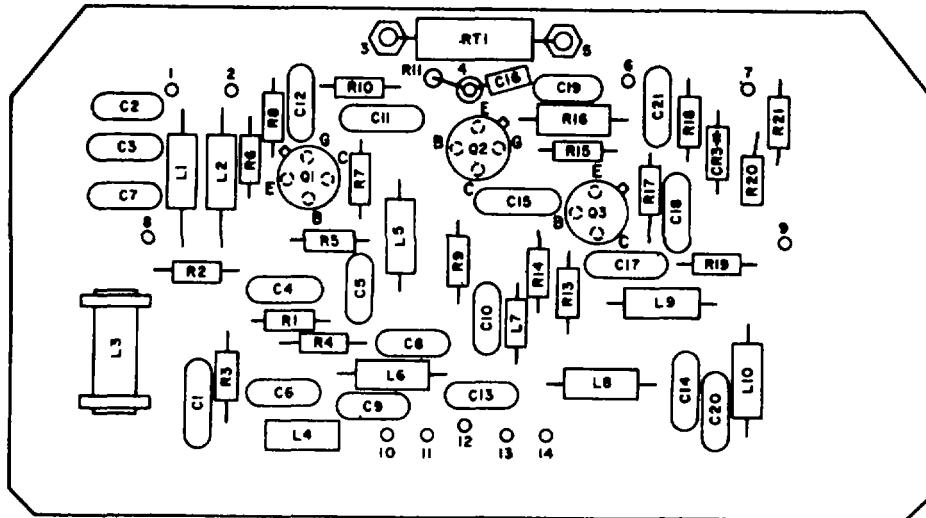
A. PARTS ON FRONT OF BOARD A2



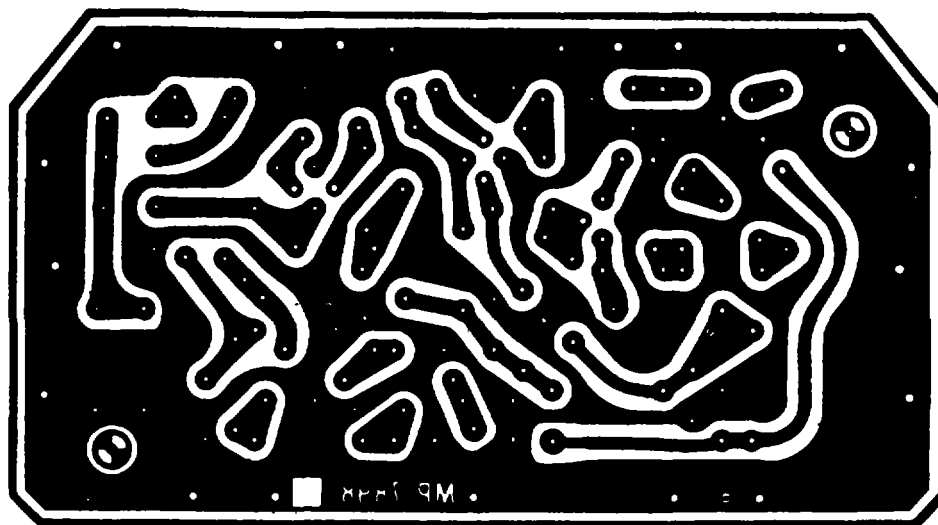
B WIRING ON BACK OF BOARD A2 (VIEWED THROUGH FRONT)

EL21B037

Figure 4-41.1. Amplifier Mixer 2A7, (956425), parts location and Printed Wiring Diagram.



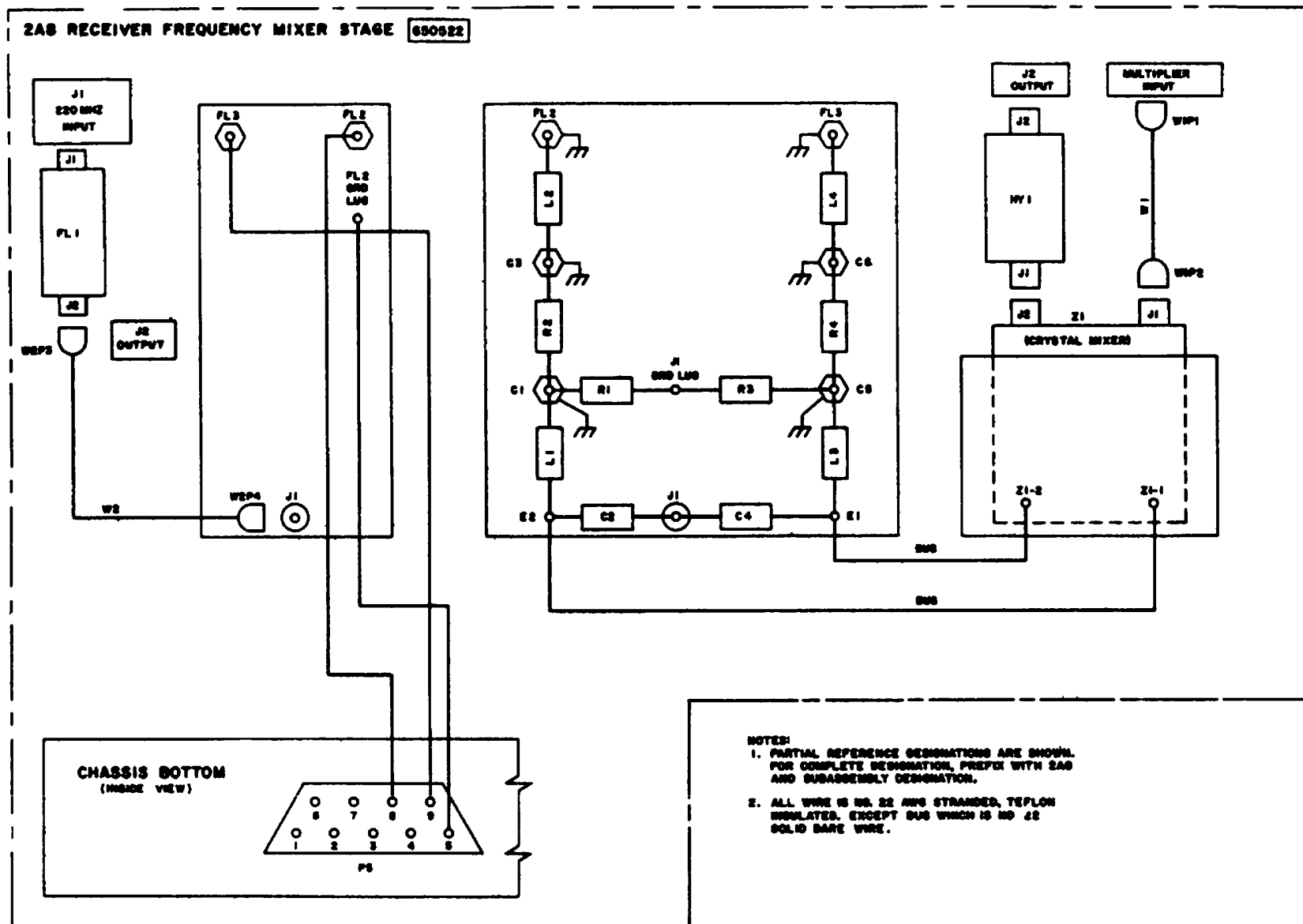
A. PARTS ON FRONT OF BOARD A2.



B. WIRING ON BACK OF BOARD A2 (VIEWED THROUGH FRONT).

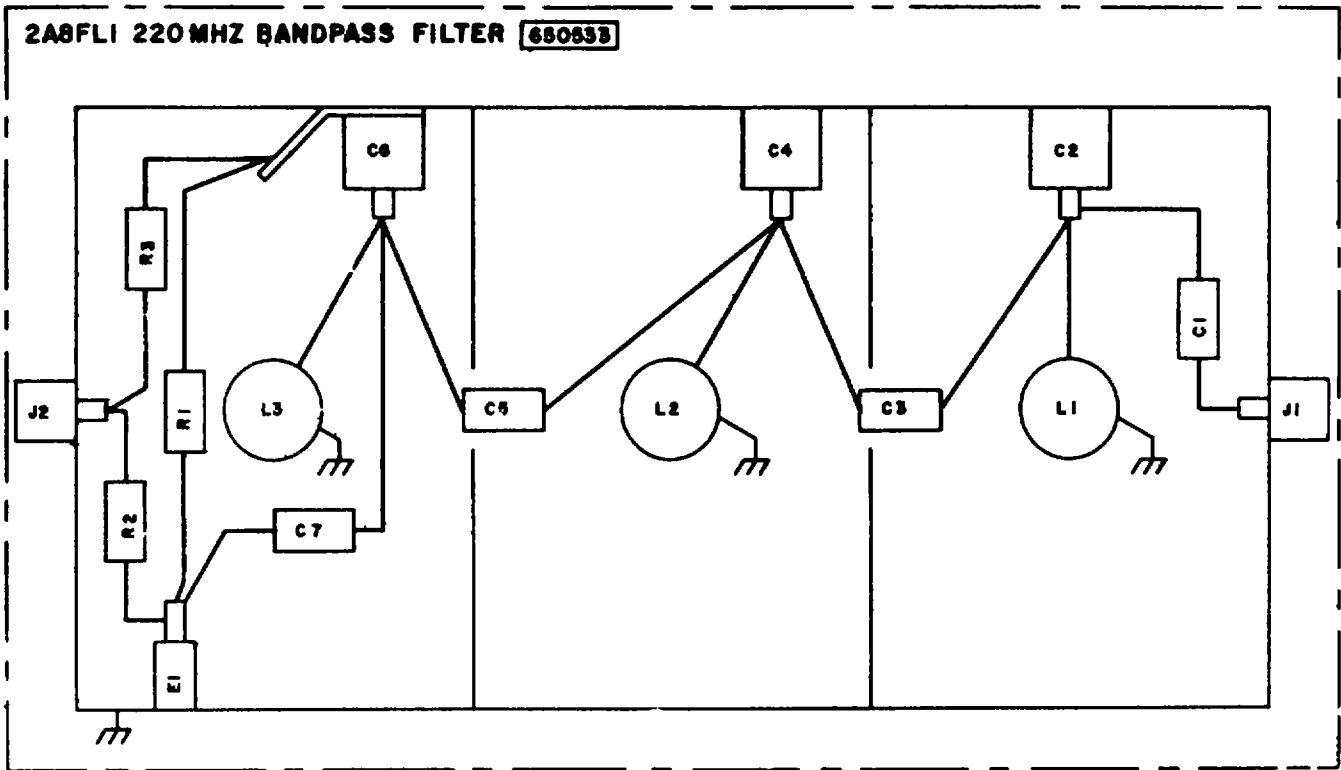
EL5820-695-35-TM-226 ②

Figure 4-41 (2). Amplifier-mixer 2A7, parts location and printed wiring diagram (part 2 of 2).



CL6920-695-35-TM-227

Figure 4-43. Receiver frequency mirror stage 2A3, wiring diagram.

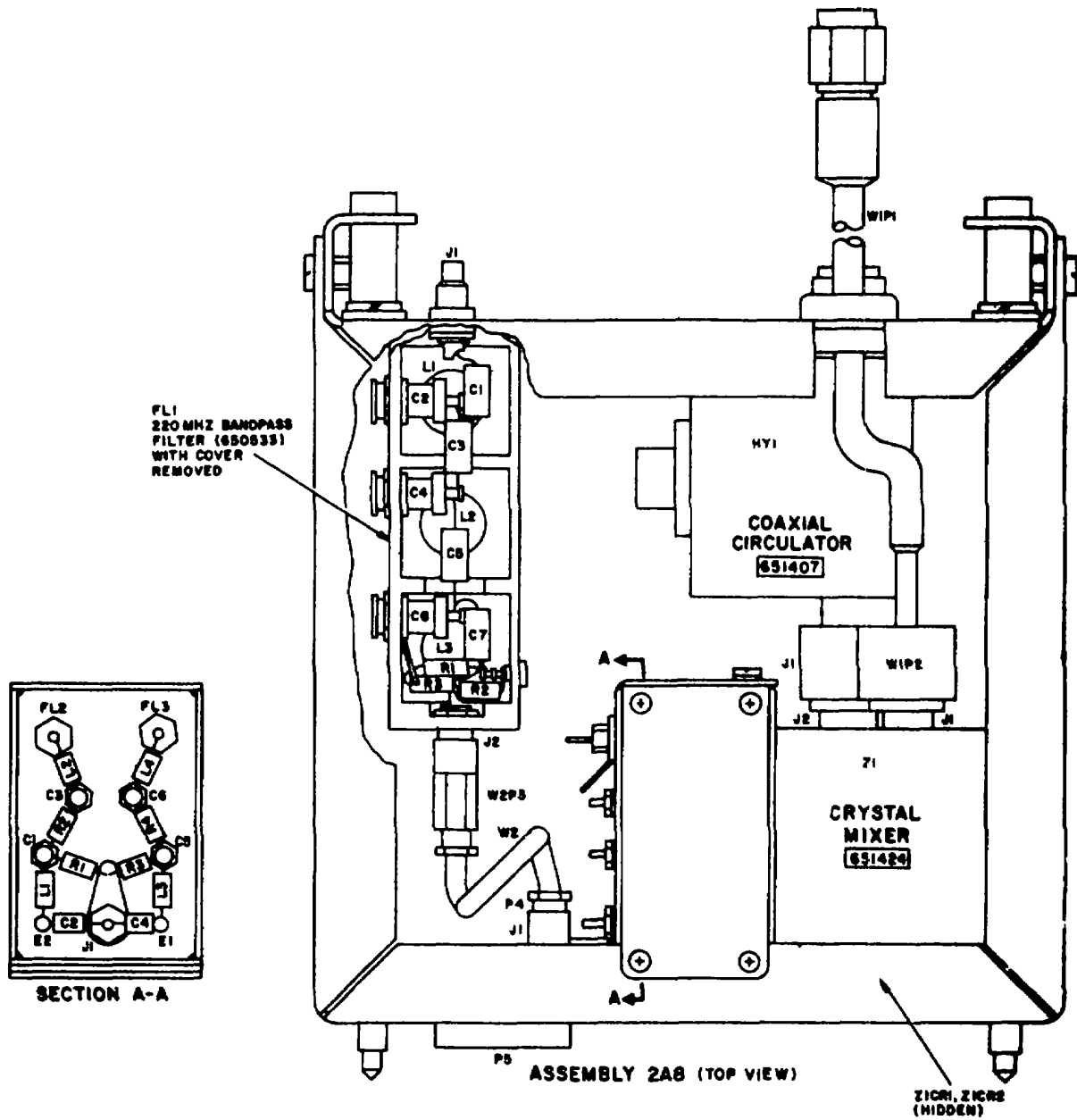


**NOTE:**

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.  
 FOR COMPLETE DESIGNATION, PREFIX WITH 2A8FL1.

EL5820-695-35-TM-239

Figure 4-43. 220 MHz bandpass filter 2A8FL1, wiring diagram.



NOTE.  
PARTIAL REFERENCE DESIGNATIONS  
ARE SHOWN FOR COMPLETE  
DESIGNATION, PREFIX WITH 2A8  
AND SUBASSEMBLY DESIGNATION.

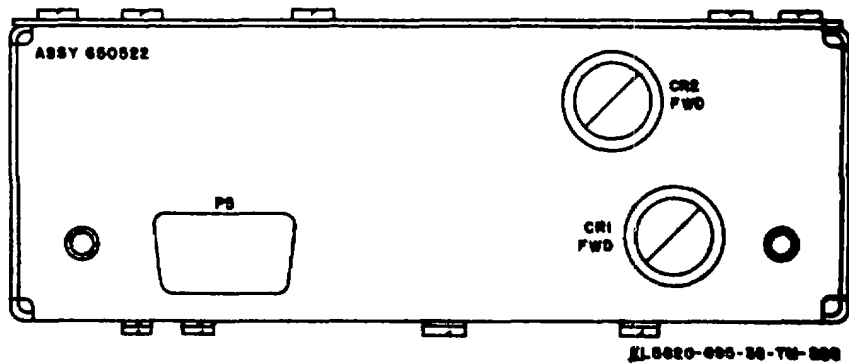
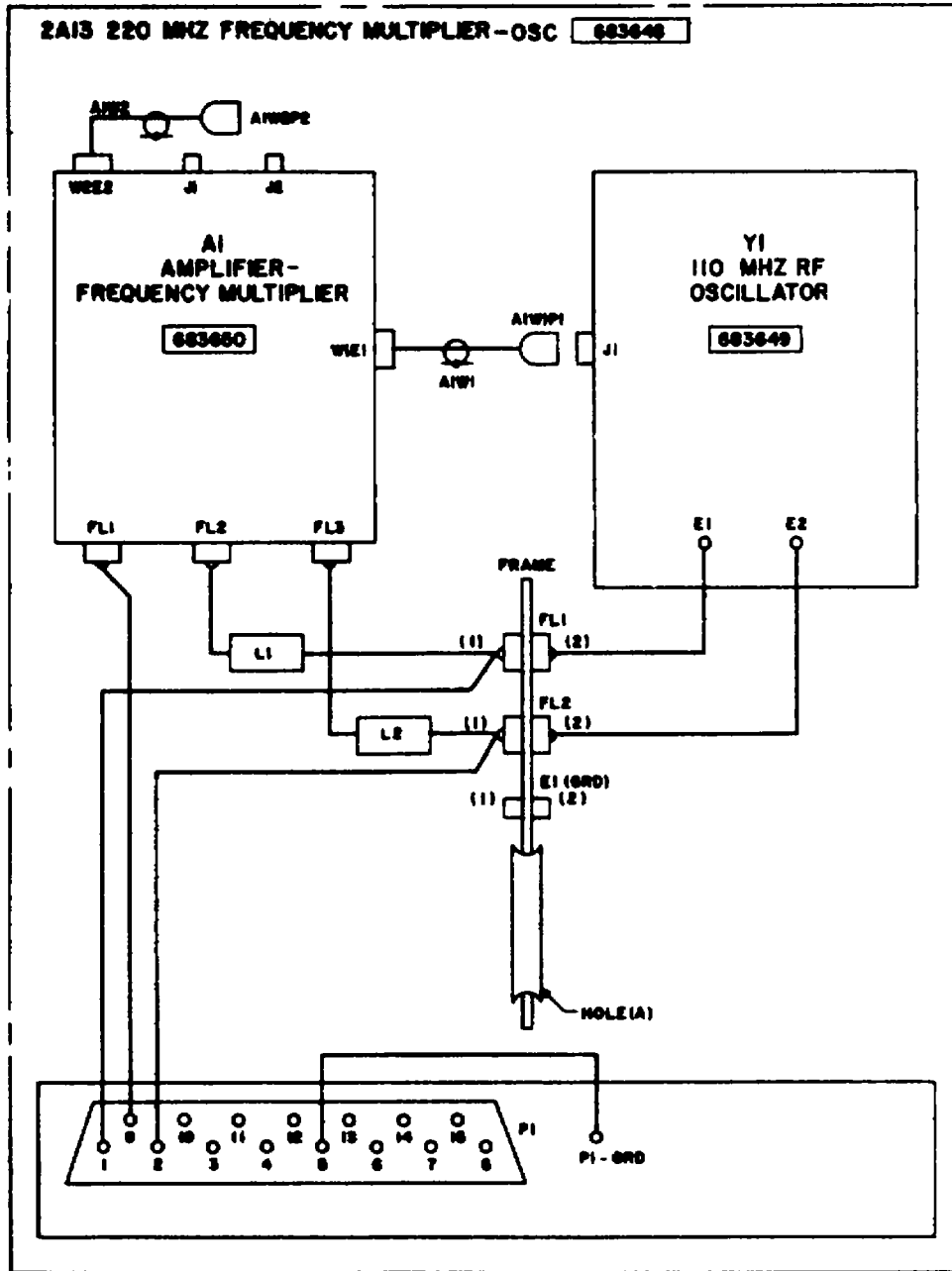


Figure 4-44. Receiver frequency mixer stage 2A8, parts location.



**NOTES:**

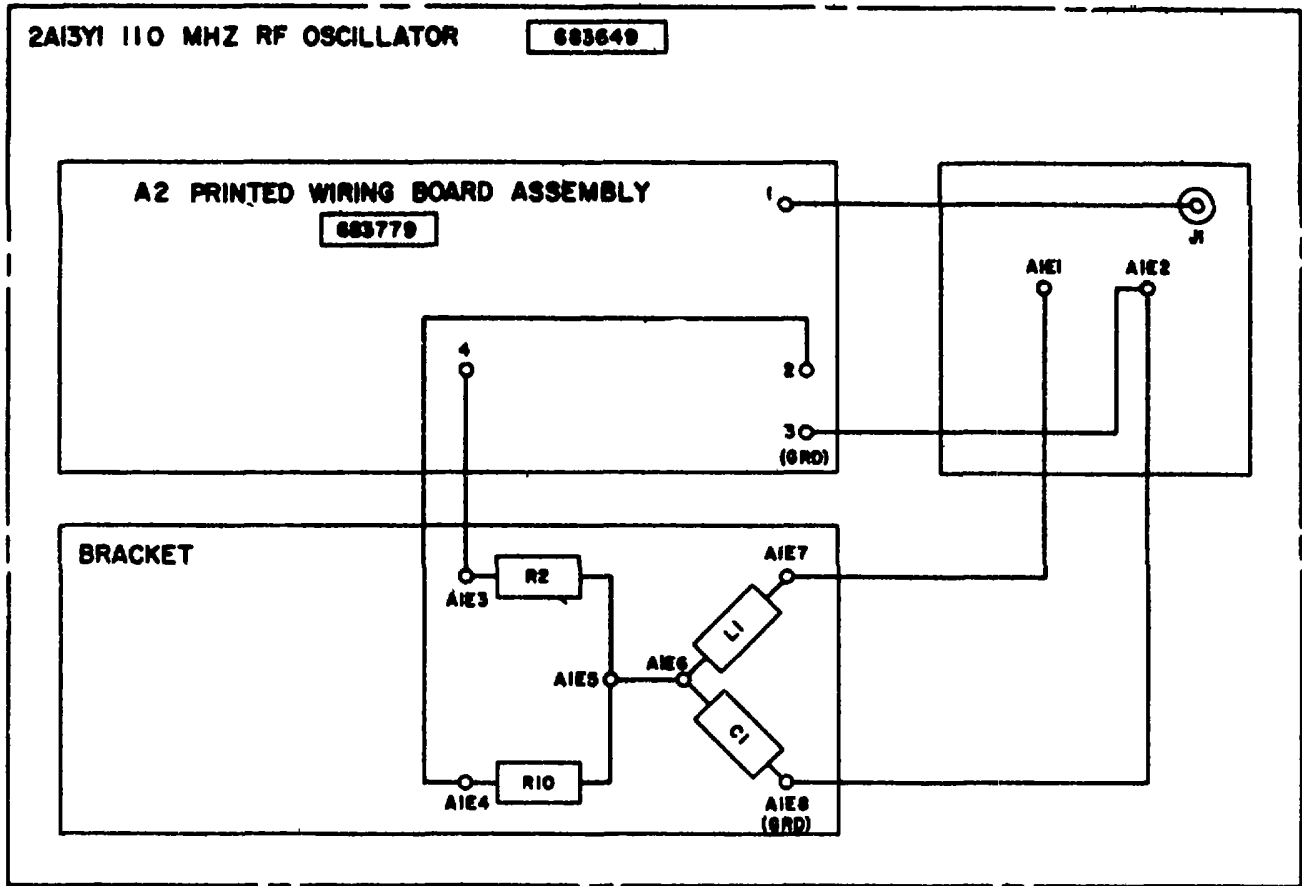
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 2A13 AND SUBASSEMBLY DESIGNATION.

2. ALL WIRE IS NO. 22 AWG STRANDED, TEFLON INSULATED.

EL6820-695-35-TM-23

Figure 4-45. 220 MHz frequency multiplier-osc 2A13, wiring diagram.





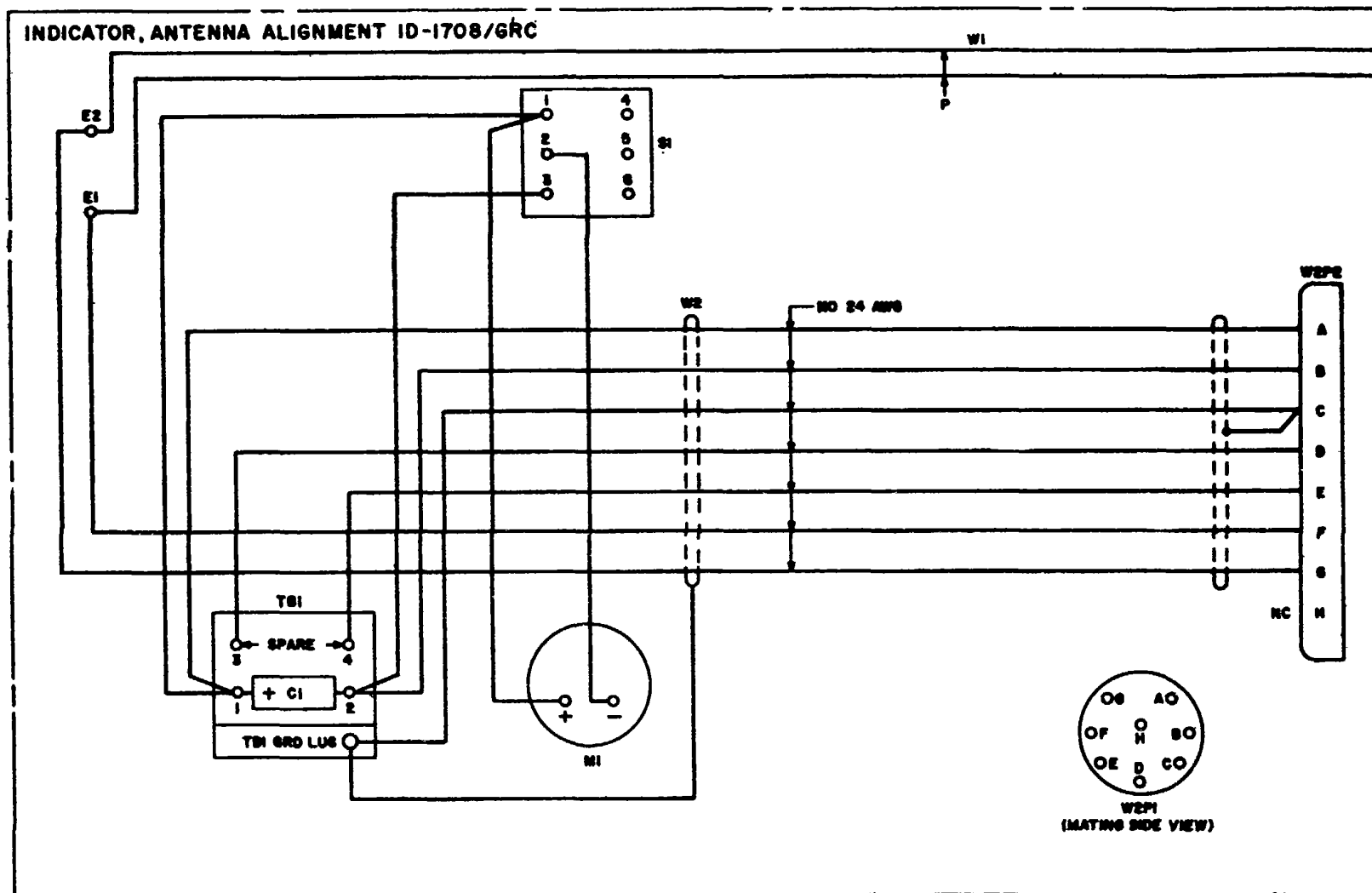
**NOTES:**

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 2A13Y1 AND SUBASSEMBLY DESIGNATION.

2. ALL WIRE IS NO. 22 AWG STRANDED, TEFLON INSULATED.

EL 5820-695-35-TM-233

Figure 4-46. 110 MHz rf oscillator 2A13Y1, wiring diagram.



**NOTES:**

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER 3.

2. ALL WIRE IS NO. 22 AWG STRANDED, TEFLON INSULATED, UNLESS OTHERWISE SPECIFIED.

EL6820-695-35-TM-237

Figure 4-47. Indicator, Antenna Alignment ID-1708/GRC, wiring diagram.

CHAPTER 5

DIAGRAMS

5-1. General

All foldout illustrations referenced in chapters 1 through 4 are contained at the end of this manual. Color code marking, block diagrams, schematics, timing diagrams, interconnecting diagrams, wiring diagrams, and parts location diagrams are included in this group.

- Figure 5-6.1
- Figure 5-8.2
- Figure 5-8.3
- Figure 5-9
- Figure 5-11.1
- Figures 5-12 through 5-14
- Figures 5-16 and 5-17

5-2. Radio Set AN/GRC-144(V) and AN/GRC-144(V) 3

Radio Set AN/GRC-144(V) can be used in four different configurations. Figures 5-2 through 5-2.1 are block diagrams illustrating the four configurations of the AN/GRC-144(V). Figure 5-2 is also a block diagram illustrating Radio Set AN/GRC-144(V)3 which operates in the cable terminal configuration only, with radio patch panel plug 1A15W27P2 always connected in jack 1A15W27J13.

5-2.1 Radio Set AN/GRC-144(V)4

Figure 5-2.1 block diagram illustrates AN/GRC-144(V)4 cable terminal operating configuration.

5-3. Transmitter, Radio T-1054(P)/GRC-144(V) and T-1054(P)A/GRC-144(V)

a. Block Diagrams.

(1) T-1054(P)/GRC-144(V). The figures listed below are T-1054(P)/ GRC-144(V) block diagrams.

- Figure 5-6
- Figure 5-7
- Figure 5-8
- Figure 5-8.1
- Figures 5-9 through 5-11
- Figures 5-12 through 5-14

(2) T-1054(P)A/GRC-144(V). The figures listed below are T-1054(P)A/ GRC-144(V) block diagrams.

b. Interconnecting Diagrams and Schematics.

(1) T-1054(P)/GRC-144(V). The figures listed below are T-1054(P)/ GRC-144(V) interconnecting diagrams and schematics.

- Figure 5-15
- Figure 5-17
- Figures 5-23, 5-24, 5-25 and 5-26
- Figures 5-27 through 5-38
- Figures 5-39 through 5-51
- Figure 5-53

(2) T-1054(P)A/GRC-144(V). The figures listed below are T-1054(P)A/ GRC-144(V) interconnecting diagrams and schematics.

- Figure 5-15.1
- Figure 5-24.1
- Figure 5-25
- Figure 5-26.1
- Figure 5-27
- Figure 5-38.2 through 5-38.10
- Figure 5-39 through 5-51
- Figure 5-53

c. Timing Diagram. Figure 5-52.

d. Wiring Diagrams and Parts Location Diagrams.

(1) T-1054(P)/GRC-144(V). The figures listed below are T-1054(P)/ GRC-144(V) wiring diagrams and parts location diagrams.

Figures 5-65 through 5-69  
 Figure 5-70  
 Figures 5-71 through 5-83  
 Figures 5-84 through 5-89

(2) T-1054(P)/A/GRC-144(V)

Figures 5-59 through 5-63  
 Figures 5-64.1 and 5-64.2  
 Figures 5-65 through 5-68  
 Figure 5-70.1  
 Figure 5-71 through 5-74  
 Figures 5-83.1 through 5-89

5-4. Receiver, Radio R-1467(P)/GRC-144(V):  
 and R-1467(P)/A/GRC-144

a. Block Diagrams.

(1) R-1467(P)/GRC-144(V). The figures listed below are R-1467(P)/ GRC-144(V) block diagrams.

Figure 5-18  
 Figure 5-19  
 Figure 5-20

(2) R-1467(P)/A/GRC-144(V). The figures listed below are R-1467(P)/A/ GRC-144(V) block diagrams.

Figure 5-18.1  
 Figure 5-19.1  
 Figure 5-20

b. Interconnecting Diagrams and Schematics.

(1) R-1467(P)/GRC-144(V). The figures listed below are R-1467(P)/GRC-144(V) interconnecting diagrams and schematics.

Figures 5-24 and 5-22  
 Figures 5-45 through 5-54

Figure 5-55  
 Figures 5-56 through 5-58

(2) R-1467(P)/A/GRC-144(V). The figures listed below are R-1467(P)/A/ GRC-144(V) block diagrams.

Figure 5-21.1 and 5-22  
 Figures 5-45 through 5-53  
 Figure 5-54.1  
 Figure 5-55.1  
 Figures 5-56 through 5-58

c. Wiring Diagrams and Parts Location Diagrams.

(1) R-1467(P)/GRC-144(V). The figures listed below are R-1467(P)/ GRC-144(V) wiring diagrams and parts location diagrams.

Figure 5-90  
 Figure 5-92  
 Figures 5-93 through 5-97

(2) R-1467(P)/A/GRC-144(V). The figures listed below are R-1467(P)/A/GRC-144(V) wiring diagrams and parts location diagrams.

Figure 5-90.1  
 Figures 5-92.1 and 5-92.2  
 Figures 5-94 through 5-97

5-5. Converter-Multiplier CV-3633/  
 GRC-144(V)

a. Interconnecting Diagrams and Schematics. Figures 5-98 through 5-106 are interconnecting diagrams and schematics of the CV-3633/GRC-144(V).

b. Parts Location Diagrams. Figures 5-107 through 5-118 are parts location diagrams for the CV-3633/GRC-144(V).

## APPENDIX A

## REFERENCES

AR-708-1 (AMDF)	Preservation, Packaging, Packing, Packing Segment of Referenced Army Regulation.
DA Pam 310-1	Consolidated Index of Army Publications and Blank Forms.
DA Pam 738-750 update.	The Army Maintenance Management System (TAMMS), Part of Maintenance Management
TB 43-0127	Maintenance and Repair of Printed Circuit Boards and Printed Wiring Assemblies.
TM 11-5820-695-12	Operator's and Organizational Maintenance Manual Radio Sets AN/GRC-144(V)1 (NSN 5820-01-048-9110), AN/GRC-144(V)2 (NSN 5820-01-0617029), AN/GRC-144(V)3 (NSN 5820-01-100-3303), and AN/GRC-144(V)4 (NSN 5820-01-099-7798) TM 11-5995-205-15 Operator Organizational, Direct Support, General Support, and Depot Maintenance Manual Including Repair Parts and Special Tools Lists: Cable Assembly, Special Purpose Electrical CX-4245/G.
TM 11-6625-203-13	Operator and Organizational Maintenance Manual: Multimeter AN/URM-105 and AN/URM-105C (Including Multimeters, ME-77/U and ME-77C/U).
TM 11-6625-214-12	Operator's Manual and Organizational Maintenance Manual for Signal Generators AN/URM-52 (NSN 6625-00-556-8107), AN/URM-52A (NSN 6625-00-592-5742) and AN/URM 52B (NSN 6625-00-965-1501).
TM 11-6625-226-12	Operator and Organizational Maintenance Manual: Test Set, Electrical Meter TS-656/U.
TM 11-6625-366-15	Operator's, Organizational, DS, GS, and Depot Maintenance Manual: Multimeter TS-352B/U (NSN 6625-00-553-0142).
TM 11-6625-498-12	Operator's and Organizational Maintenance Manual: Test Sets, Radio Frequency Power AN/USM-161 (NSN 6625-00-892-5541) and AN/USM-161A.
TM 11-6625-700-10	Operator's Manual: Digital Readout, Electronic Counter AN/USM-207 (NSN 6625-00-911-6368).
TM 11-6625-2658-14	Operator's, Organizational and General Support Maintenance Manual for Oscilloscope AN/USM-281C (NSN 6625-00-106-9266).

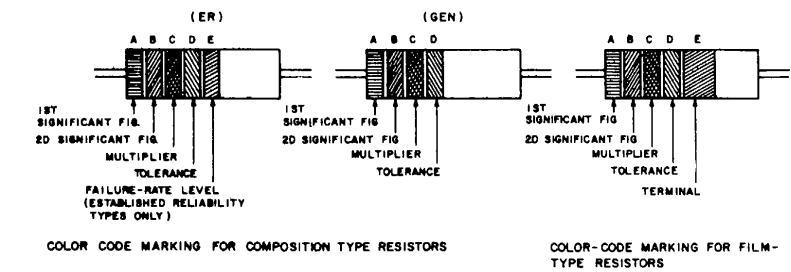


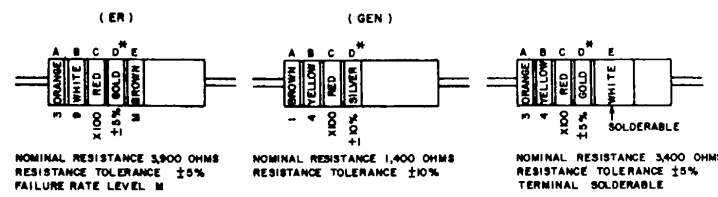
TABLE 1  
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS

BAND A		BAND B		BAND C		BAND D		BAND E	
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL
BLACK	0	BLACK	0	BLACK	1			BROWN	M
BROWN	1	BROWN	1	BROWN	10			RED	P
RED	2	RED	2	RED	100			ORANGE	R
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP TYPE ONLY)	WHITE	
GREEN	5	GREEN	5	GREEN	100,000	BOLD	±5		
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±8 (NOT APPLICABLE TO ESTABLISHED RELIABILITY)		
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7						
GRAY	8	GRAY	8	SILVER	0.01				
WHITE	9	WHITE	9	GOLD	0.1				

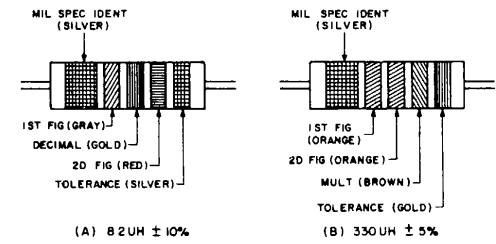
BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH)  
 BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE  
 BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE)  
 BAND D — THE RESISTANCE TOLERANCE  
 BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL. ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1-1/2 TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS (THESE ARE NOT COLOR CODED)  
 SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED FOR EXAMPLE  
 ZR7 = 2.7 OHMS 10R0 = 10.0 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED. IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS

EXAMPLES OF COLOR CODING



A COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS



COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES AT A, AN EXAMPLE OF THE CODING FOR AN 82 uH CHOKE IS GIVEN AT B, THE COLOR BANDS FOR A 330 uH INDUCTOR ARE ILLUSTRATED

TABLE 2  
COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES

COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL

CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB

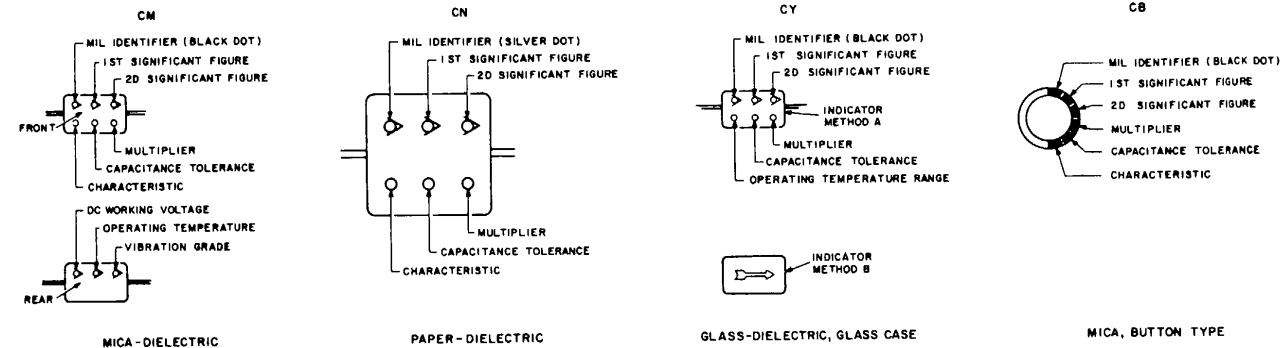


TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB

COLOR	MIL ID	1ST SIG FIG	2D SIG FIG	MULTIPLIER	CAPACITANCE TOLERANCE			CHARACTERISTIC	DC WORKING VOLTAGE	OPERATING TEMP RANGE	VIBRATION GRADE
					CM	CN	CY				
BLACK	CM, CY, CB	0	0	1							
BROWN		1	1	10				B E B			
RED		2	2	100	±2%	±2%	±2%	C		-55° TO +70°C	
ORANGE		3	3	1,000		±30%		D	D	300	
YELLOW		4	4	10,000				E			10-2,000 Hz
GREEN		5	5		±5%			F		300	
BLUE		6	6								-55° TO +150°C
PURPLE (VIOLET)		7	7								
GREY		8	8								
WHITE		9	9								
GOLD				0.1	±5%	±5%					
SILVER	CN				±10%	±10%	±10%				

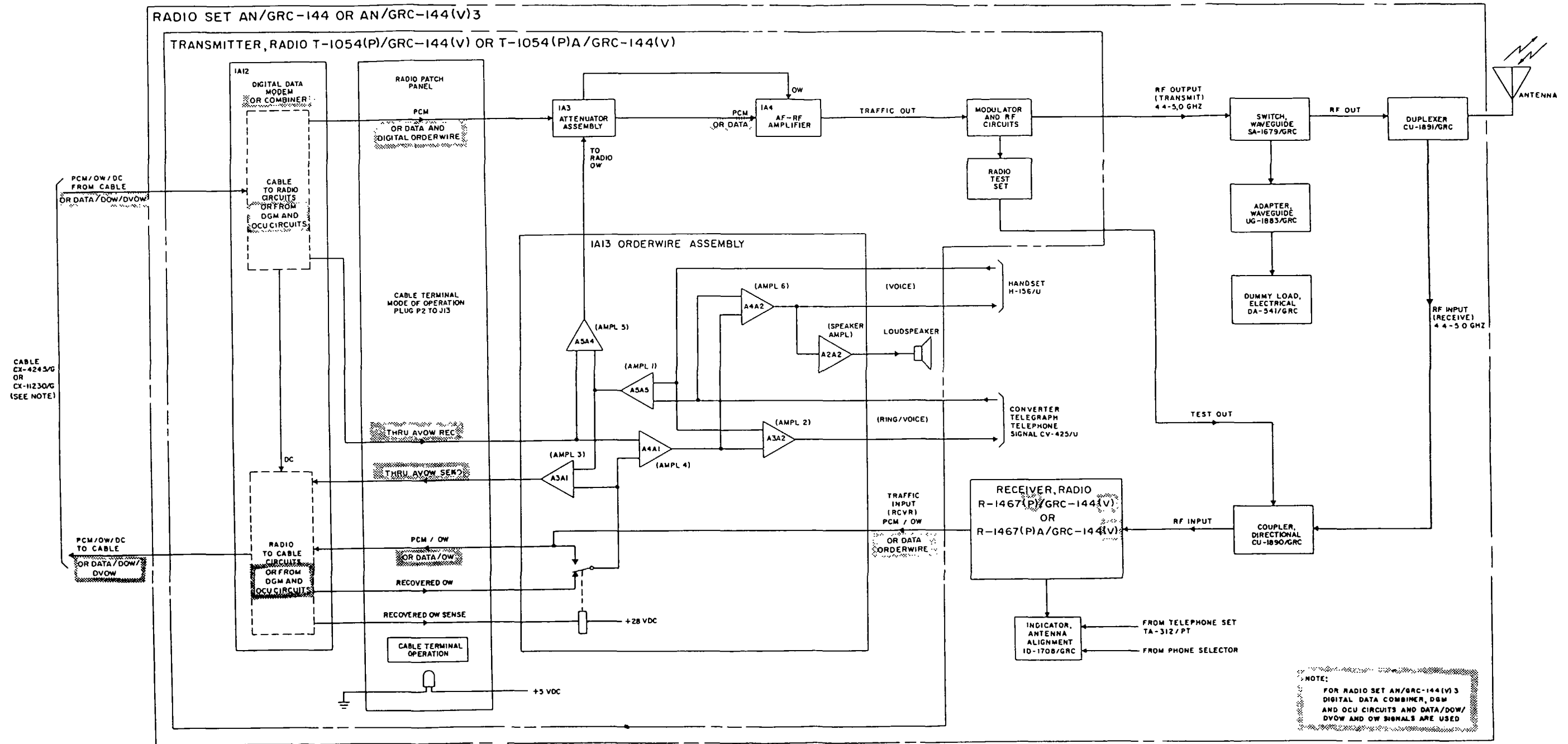
TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC

COLOR	TEMPERATURE COEFFICIENT*	1ST SIG FIG	2D SIG FIG	MULTIPLIER	CAPACITANCE TOLERANCE		MIL ID
					OVER 10 UUF	10 UUF OR LESS	
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	-30	1	1	10		±1%	
RED	-80	2	2	100		±2%	±0.25 UUF
ORANGE	-150	3	3	1,000			
YELLOW	-220	4	4				
GREEN	-330	5	5			±5%	±0.5 UUF
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GREY		8	8	0.01			
WHITE		9	9	0.1		±10%	
GOLD	+100						±1.0 UUF
SILVER							

- THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF
- LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS MIL-C-5, MIL-C-25D, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY
- LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-1015D
- TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE

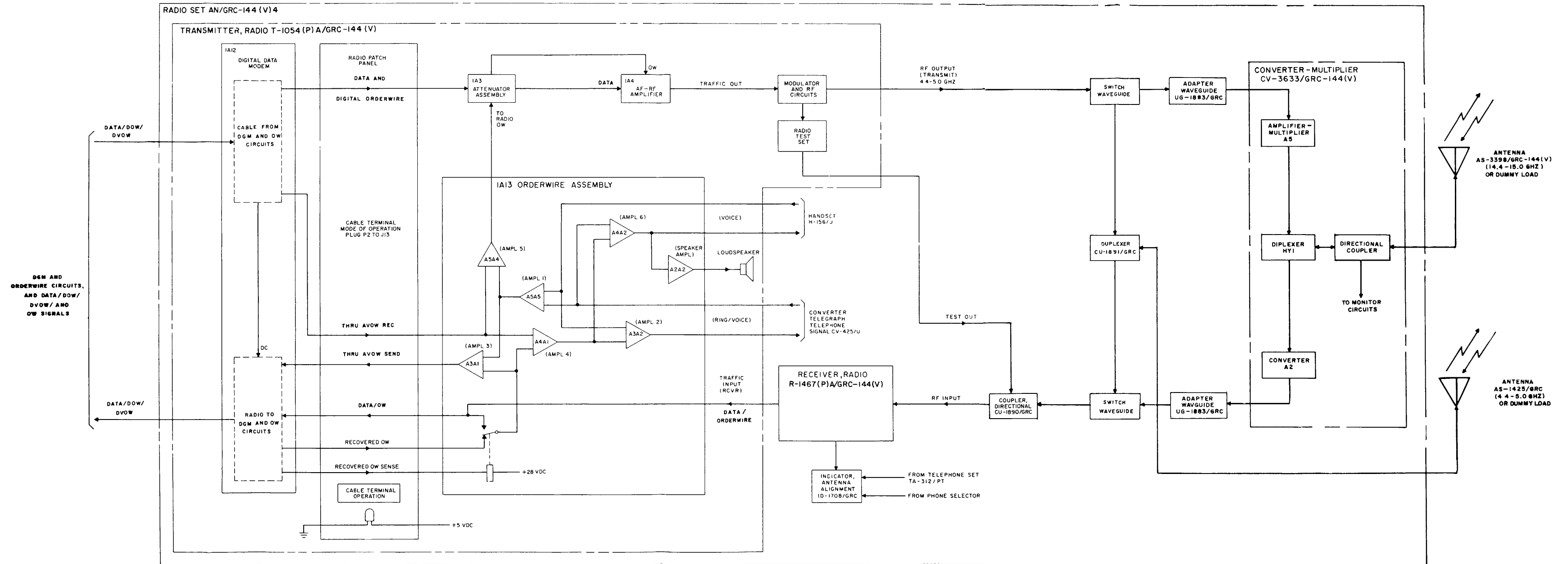
C COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS

Figure 5-1. Color code marking for MIL-STD resistors, and capacitors.  
5-3



EL5820-695-35-TM-C2-10

Figure 5-2. AN/GRC-144 (V) and AN/GRC-144 (V) 3 standard cable terminal configuration.



EL21B038

Figure 5-2.1. AN/GRC-144 (V) 4 standard cable terminal configuration block diagram.



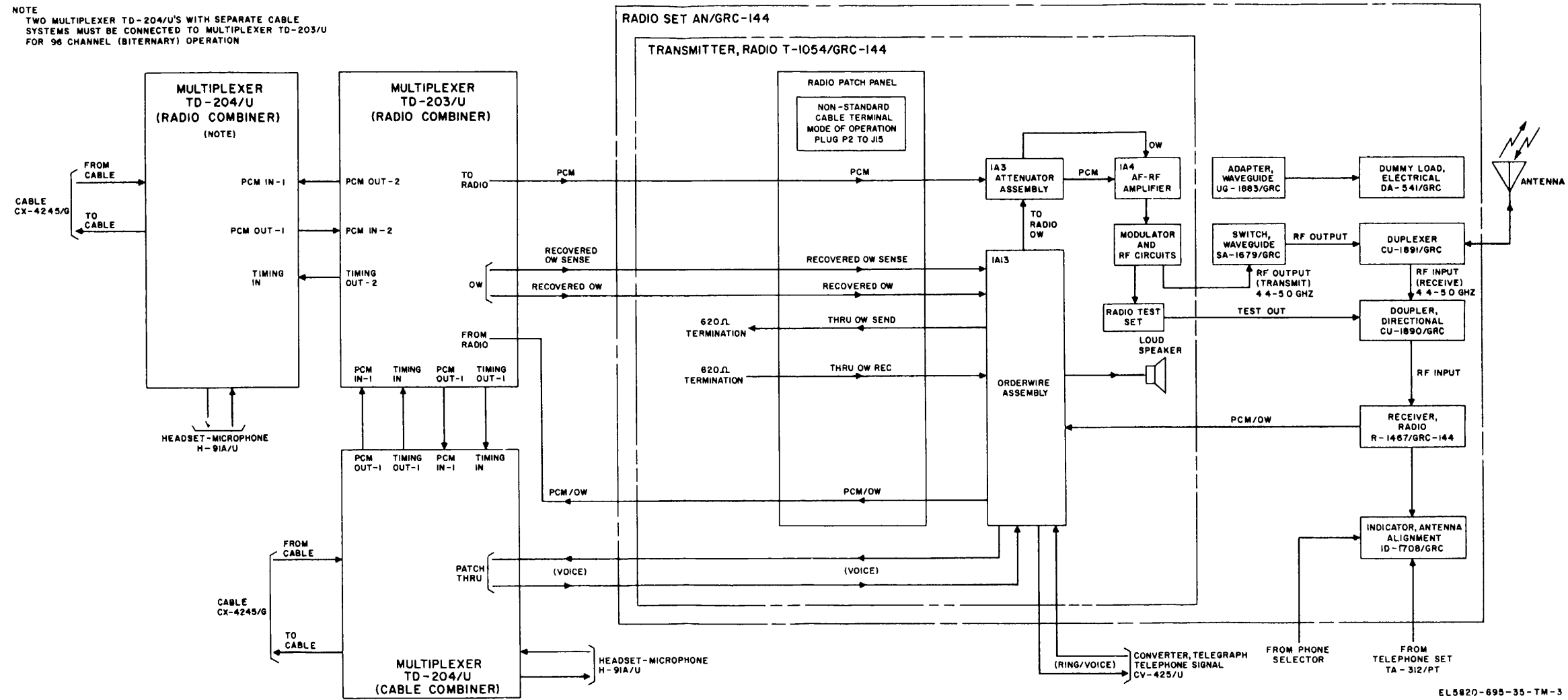
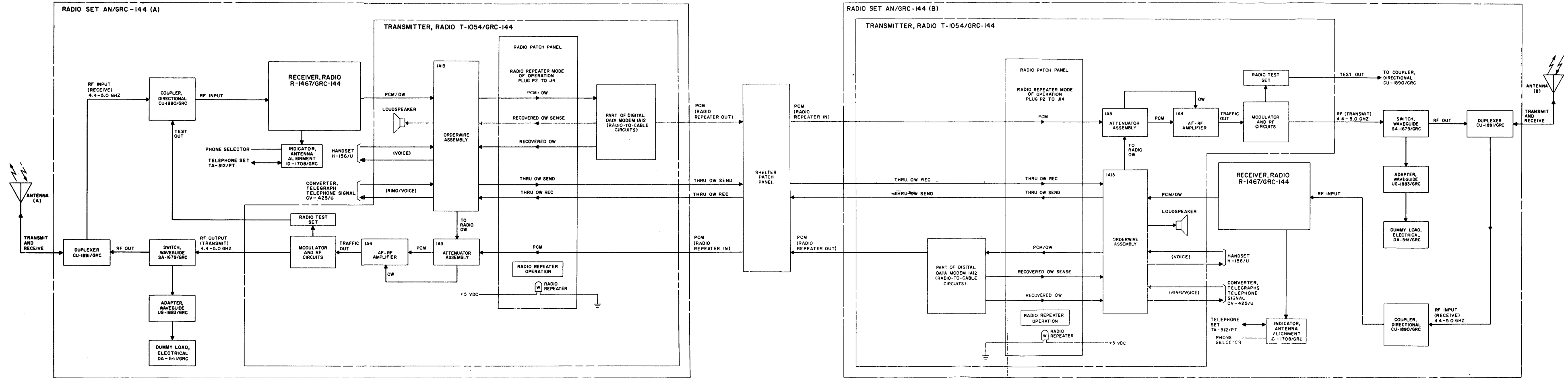


Figure 5-3. AN/GRC-144 nonstandard cable terminal configuration, block diagram.



EL 5820-695-35-TM-2

Figure 5-4. AN/GRC-144 standard radio repeater configuration, block diagram.

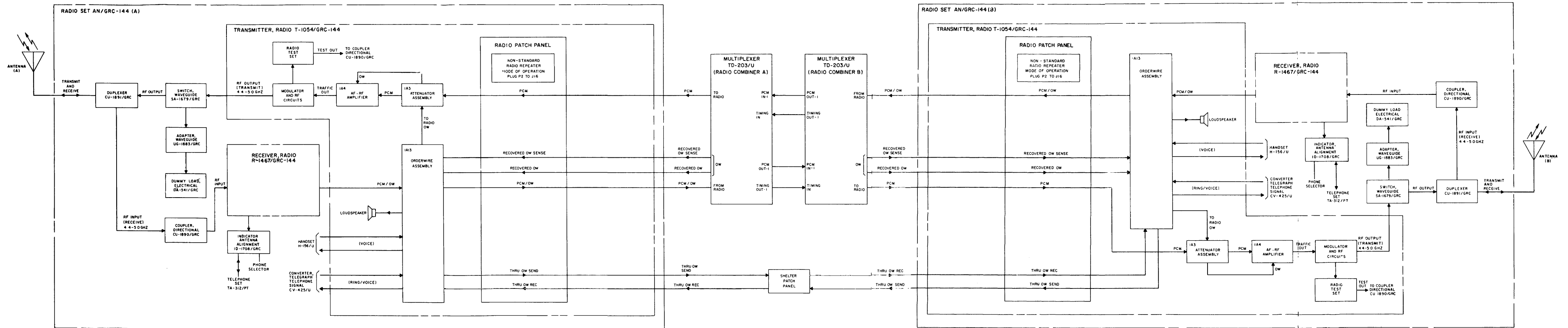


Figure 5-5. AN/GRC-144 nonstandard radio repeater configuration, block diagram.

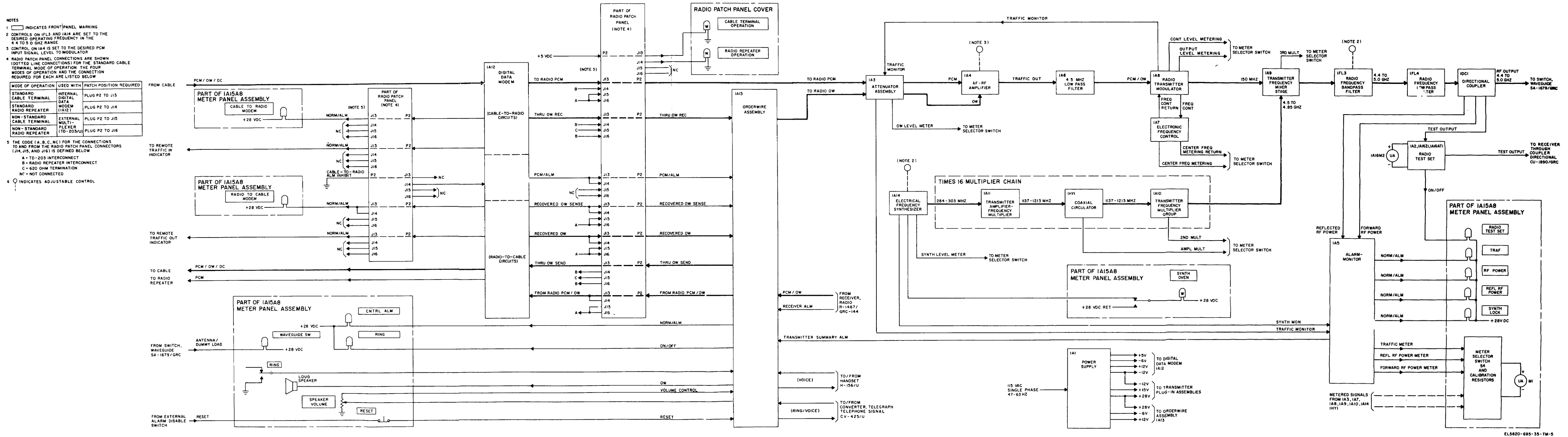


Figure 5-6. Transmitter, Radio T-1054/ GRC-144, block diagram.

- NOTES
- 1 [ ] INDICATES FRONT PANEL MARKING
  - 2 CONTROLS ON P1.3 AND P1.4 ARE SET TO THE DESIRED OPERATING FREQUENCY IN THE 4.4 TO 5.0 GHz RANGE
  - 3 CONTROL ON P1.4 IS SET TO THE DESIRED DATA/CVDDW WAVE SIGNAL LEVEL TO MODULATOR
  - 4 AT RADIO PATCH PANEL, PLUS HIGHWETTS IS ALWAYS PATCHED INTO JACK 1A2W27J15 JACK 1A2W27J14 IS NOT USED IN THIS CONFIGURATION
  - 5 NC=NOT CONNECTED
  - 6 [ ] INDICATES ADJUSTABLE CONTROL
  - 7 CABLE BYPASS ASSEMBLY USED FOR 9 AND 18 MB/SEC OPERATION ONLY

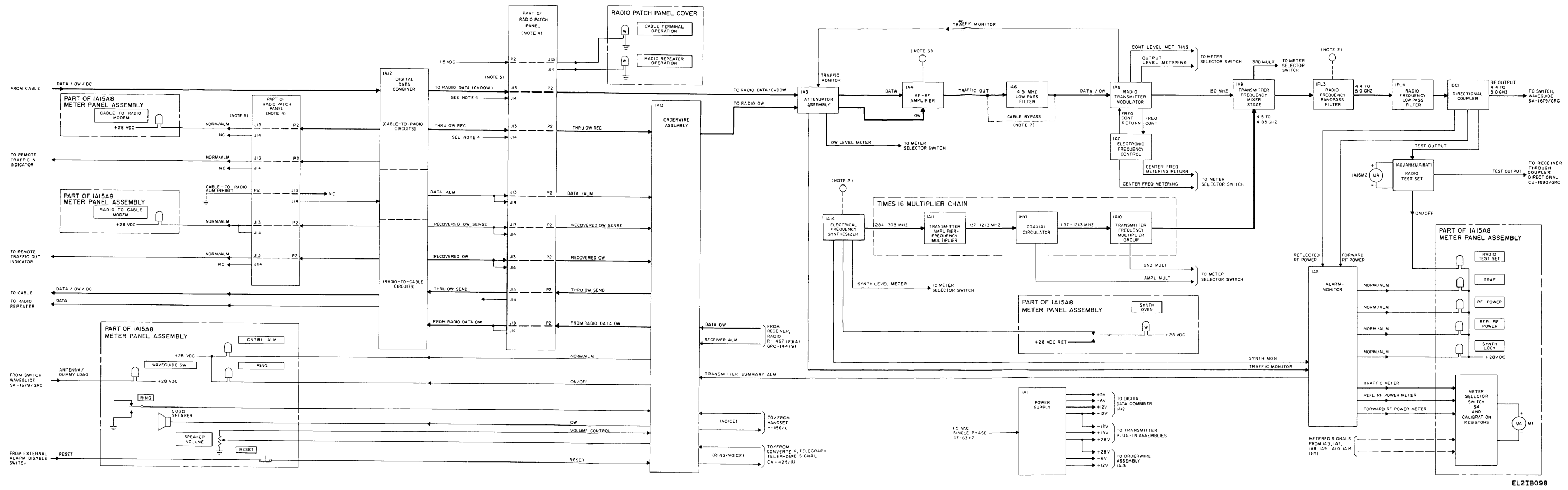


Figure 5-6.1. Transmitter, Radio T-1054 (P)/GRC-144(V) block diagram.  
Change 6 5-13.1

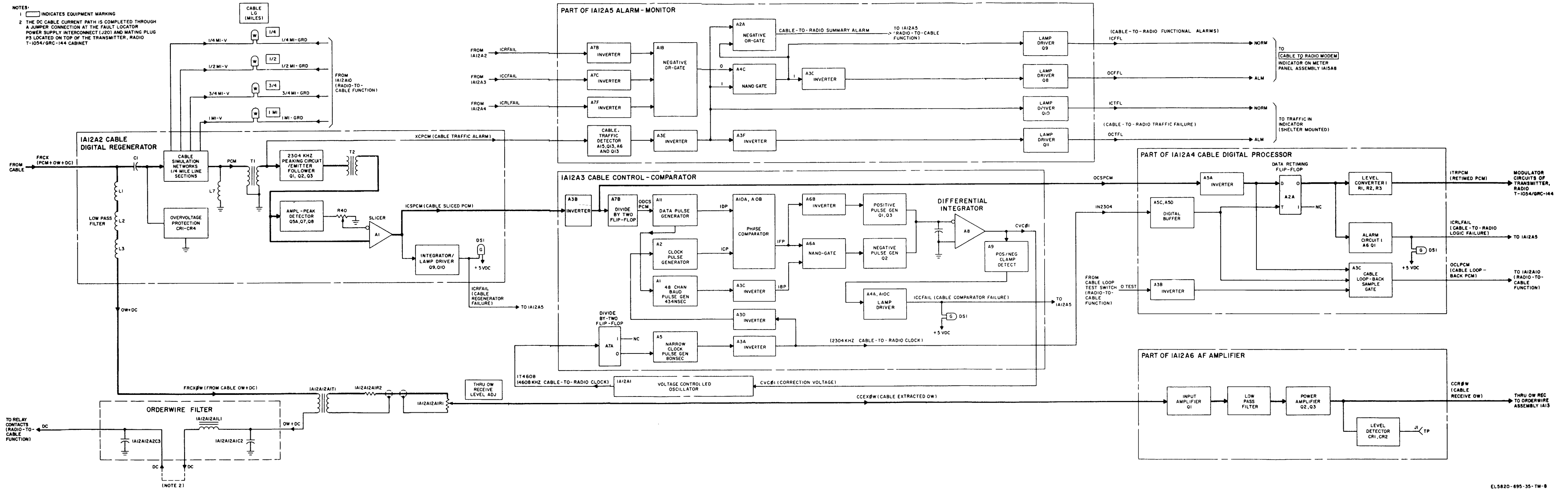


Figure 5-7. Digital data modem 1A12, cable to-radio circuits, functional block diagram, synchronous mode.

Change 1 5-15

NOTES:  
 1 [ ] INDICATES EQUIPMENT MARKING  
 2 THE DC CABLE CURRENT PATH IS COMPLETED THROUGH A JUMPER CONNECTION AT THE FAULT LOCATOR POWER SUPPLY INTERCONNECT (J20) AND MATING PLUG P3 LOCATED ON TOP OF THE TRANSMITTER, RADIO T-1054/SRC-144 CABINET

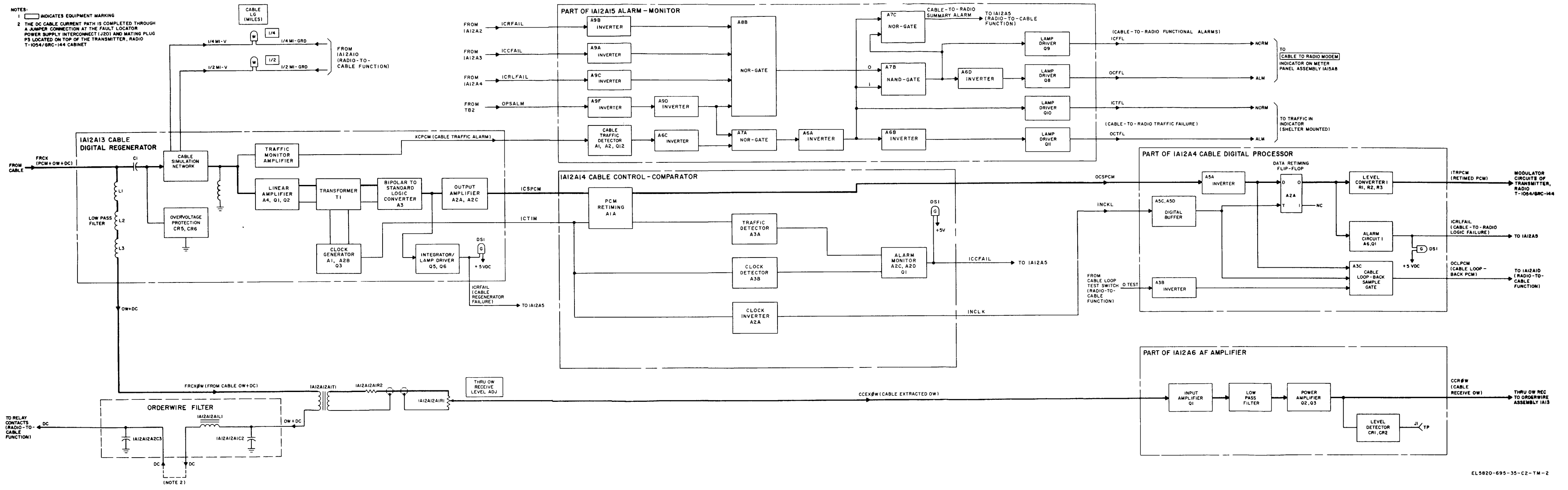


Figure 5-7.1 Digital data modem 1A12, cable to-radio circuits, functional block diagram, asynchronous mode.  
 Change 2 5-16.1





- 1. INDICATES WARNING ON EQUIPMENT
- 2. RELAY IS SHOWN EXHAUSTED
- 3. THE LOGIC OF THIS RADIO ALARM INDICATOR SIGNAL IS SHOWN IN THE RADIO ALARMER WIRE PANEL.

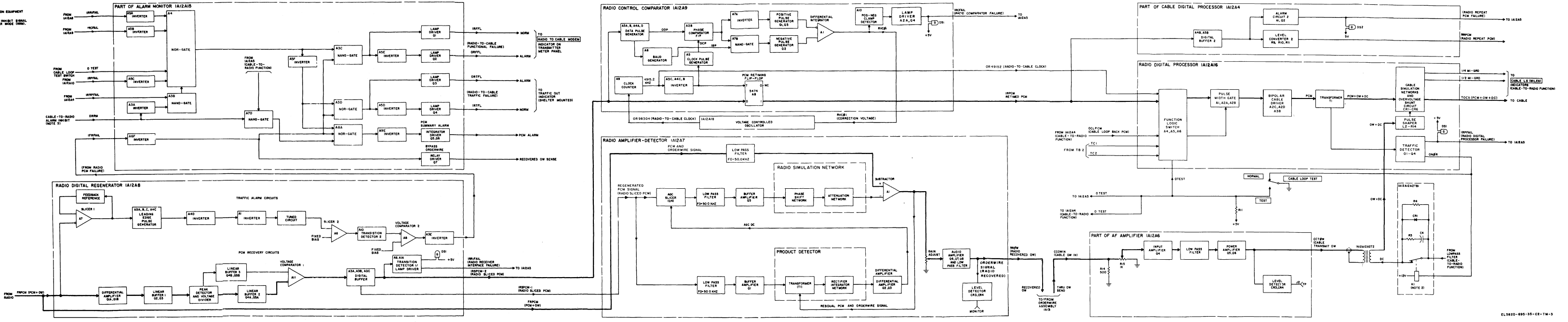


Figure 5-8.1 Digital data modem 1A12, cable to-radio circuits, functional block diagram, asynchronous mode.  
Change 2 5-18.1

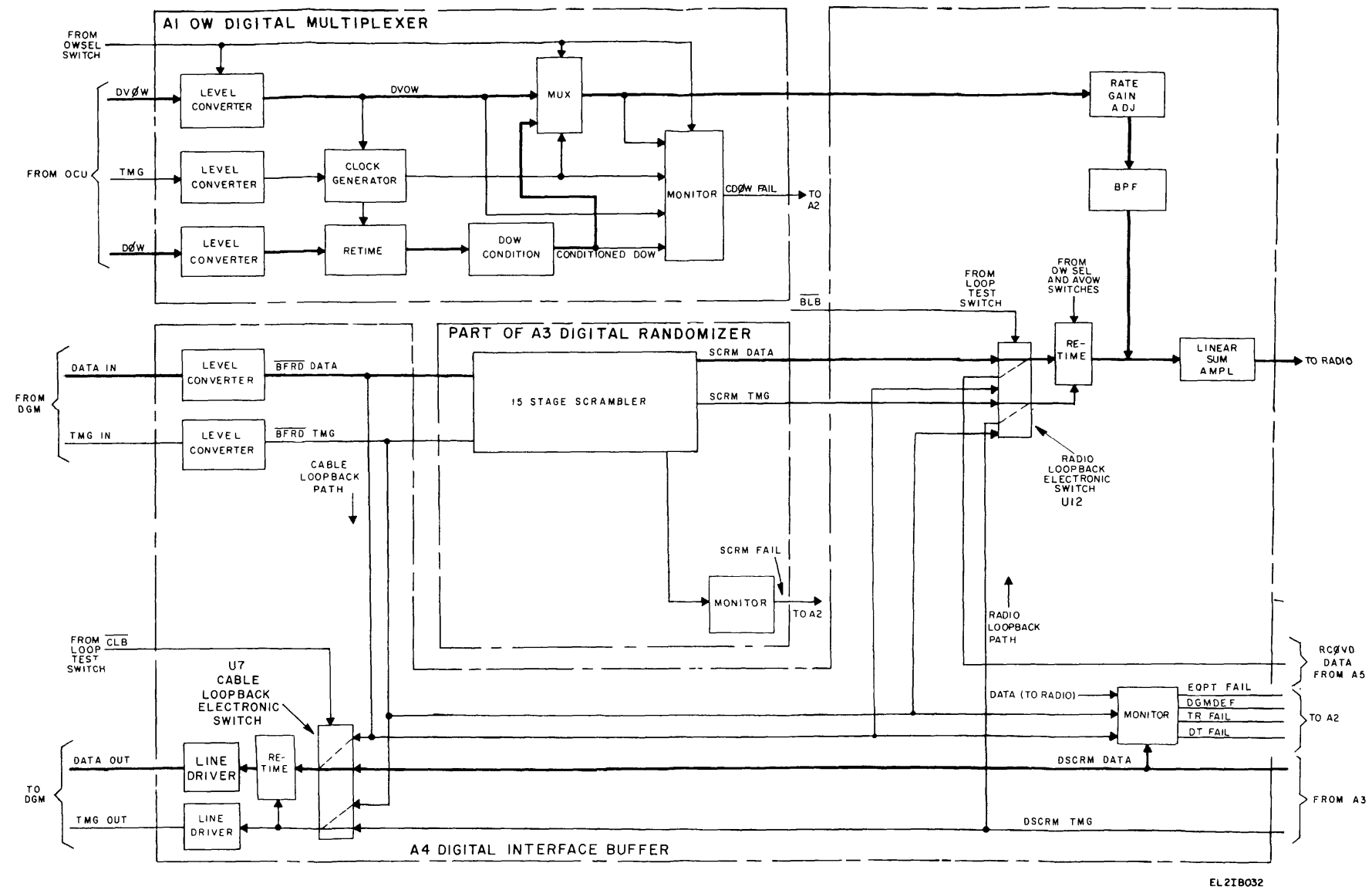
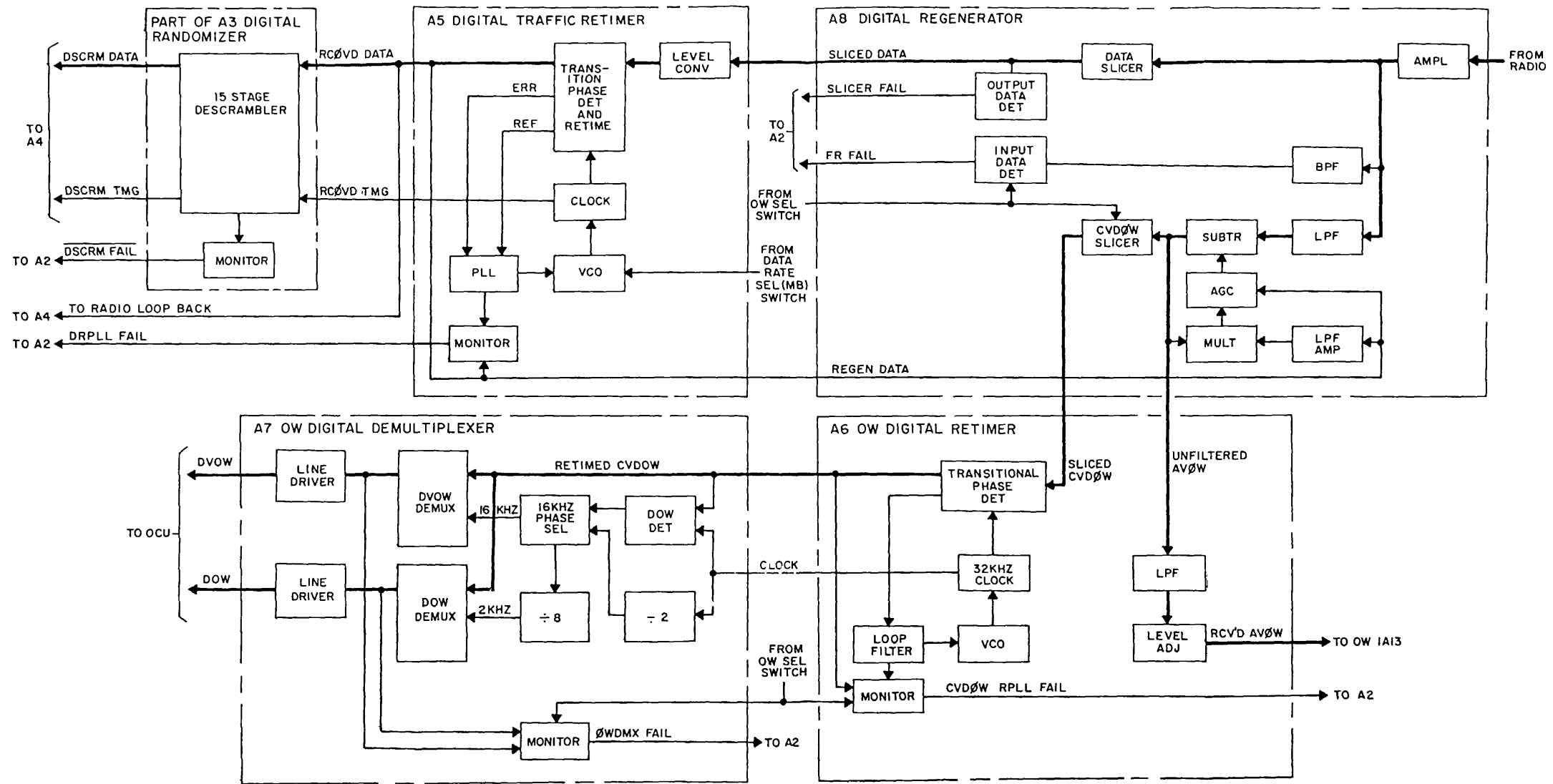


Figure 5-8.2. Digital data combiner 1A12, cable-to-radio circuits, functional block diagram.



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Figure 5-8.3. Digital data combiner 1A12, cable-to-radio circuits, functional block diagram.

Change 6 5-18.5

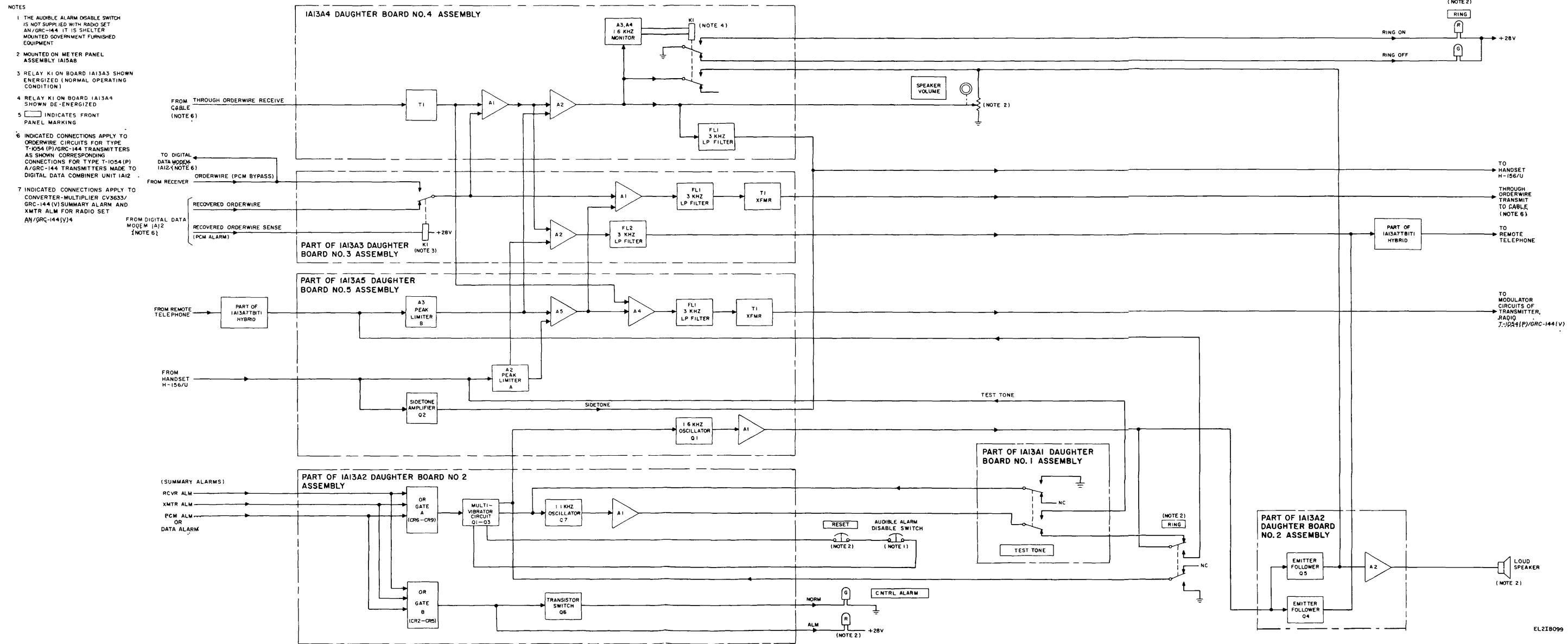


Figure 5-9. Orderwire assembly 1A13, signal distribution circuits block diagram.

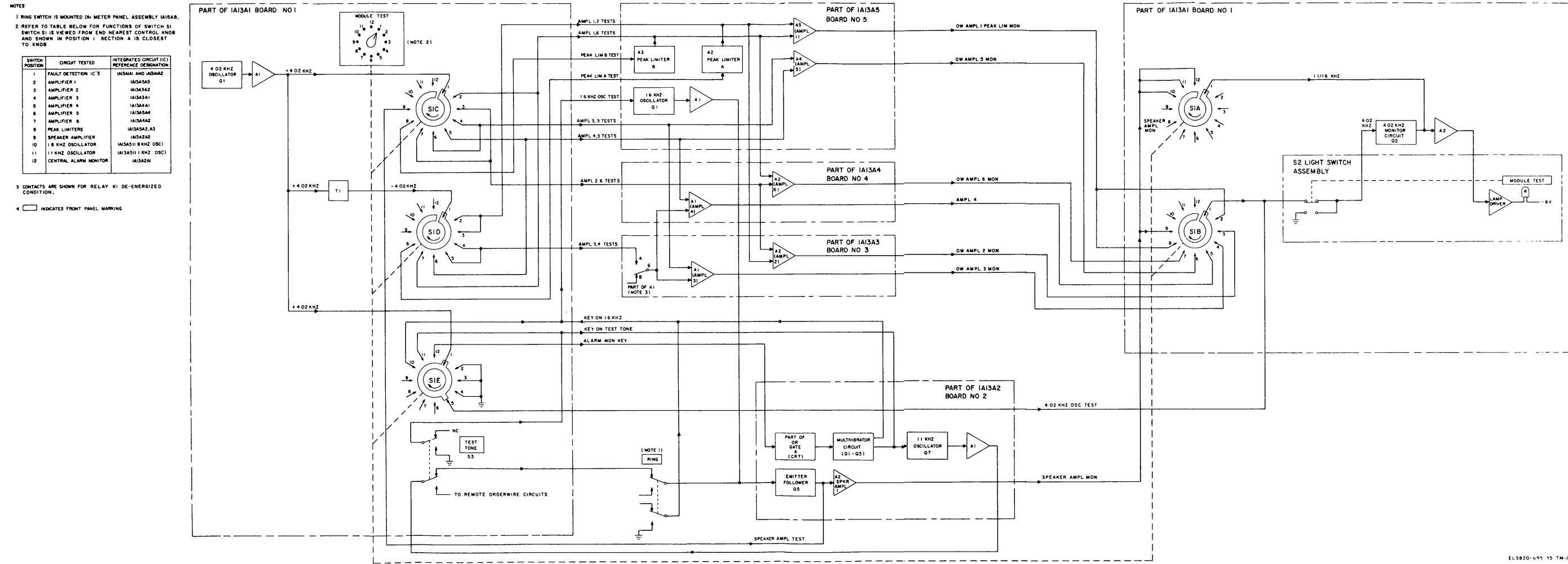


Figure 5-10. Orderwire assembly 1A13 fault detection circuits, block diagram.

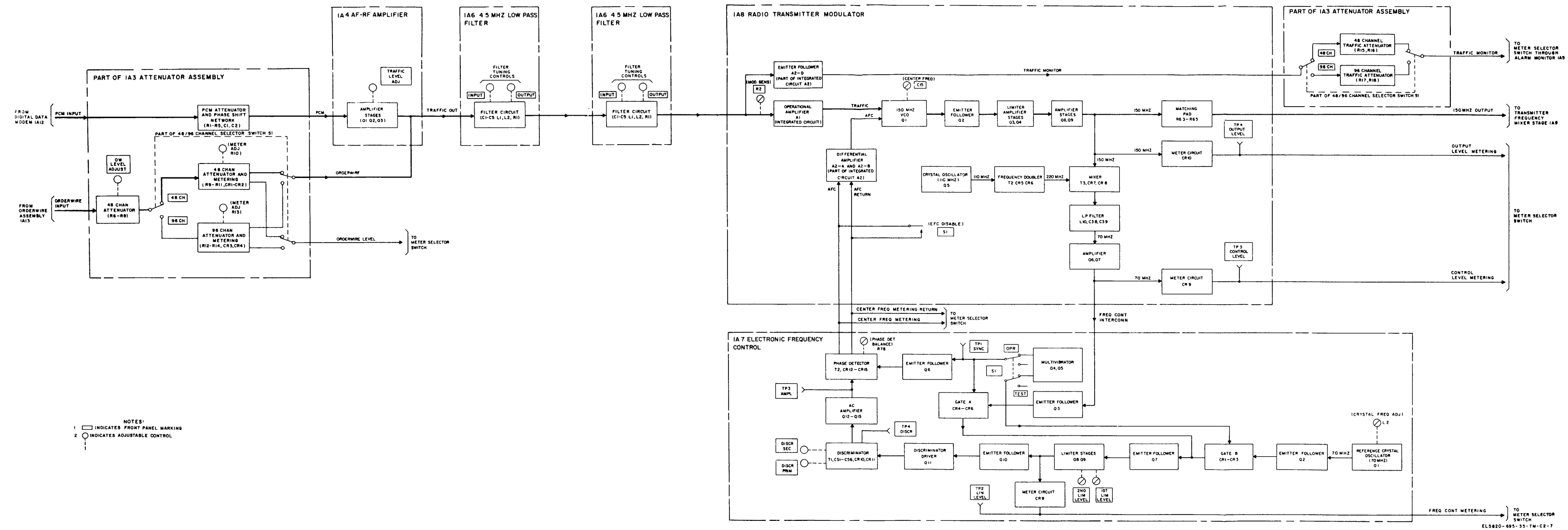


Figure 5-11. Transmitter, Radio T-1054/GRC-144 modular circuits, functional block diagram.

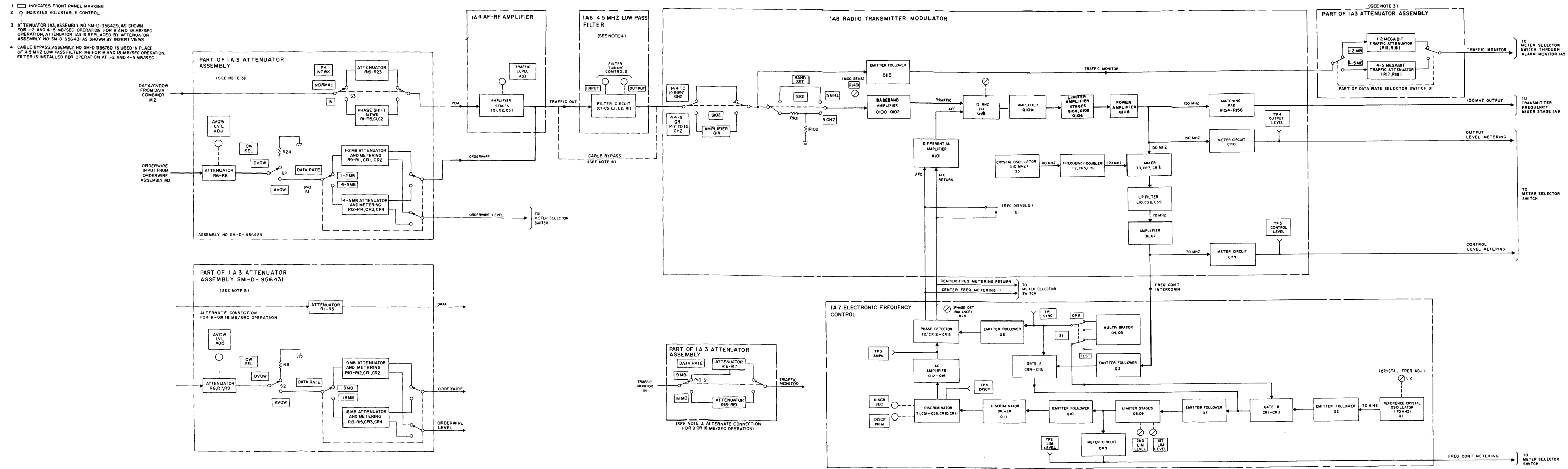
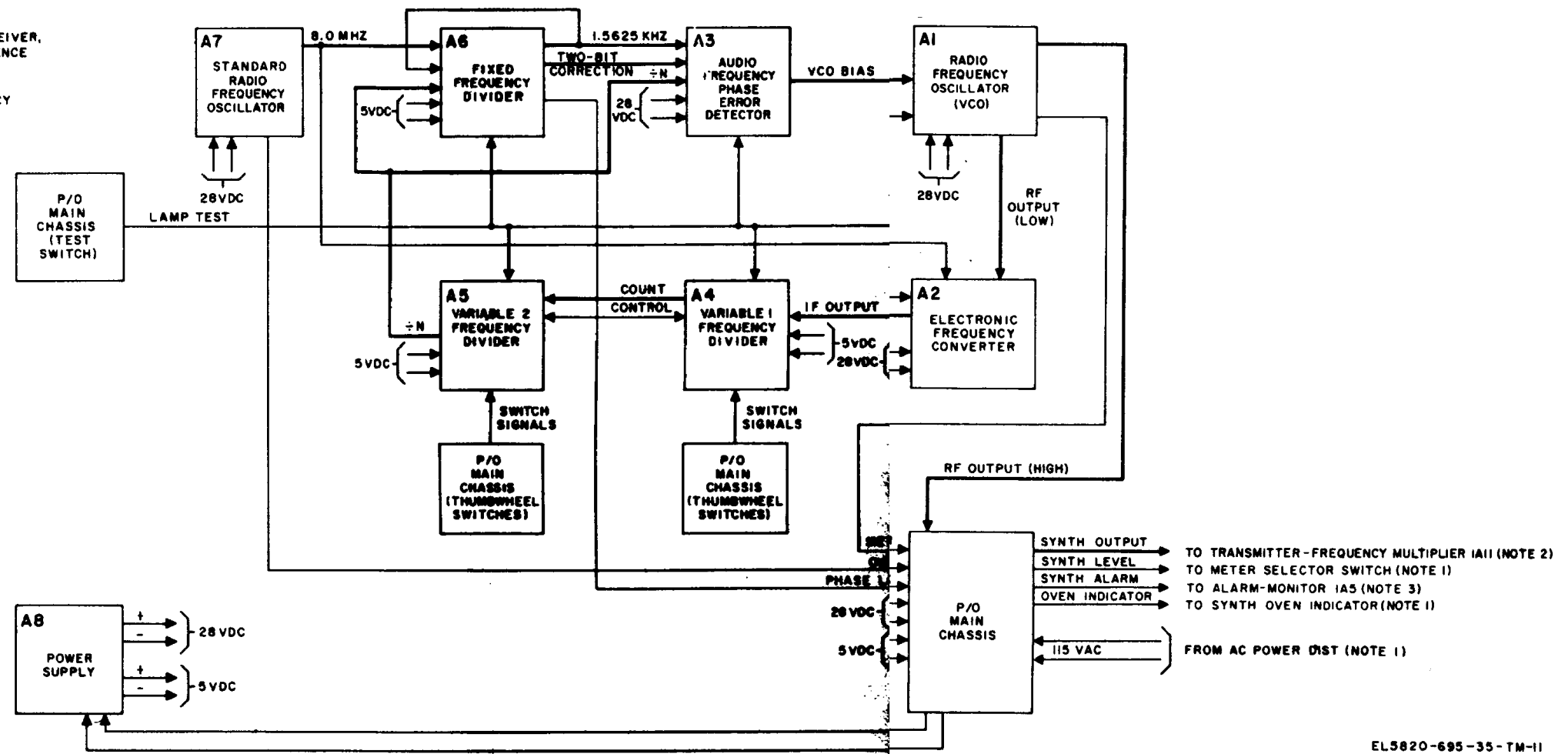


Figure 5-11.1. Transmitter, Radio T-1054 (P) A/GRC-144 (V) modular circuits functional block diagram.

NOTES:

1. THE ELECTRICAL FREQUENCY SYNTHESIZER IS USED IN TRANSMITTER, RADIO T-1054/GRC-144 (1A14) AND RECEIVER, RADIO R-1467/GRC-144 (2A14). FOR COMPLETE REFERENCE DESIGNATIONS, PREFIX WITH 1A14 OR 2A14.
2. THE SYNTH OUTPUT IS SENT TO AMPLIFIER-FREQUENCY MULTIPLIER 2A10 IN RECEIVER, RADIO R-1467/GRC-144.
3. THE SYNTH ALARM IS SENT TO ALARM-MONITOR 2A12 IN RECEIVER, RADIO R-1467/GRC-144.



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Figure 5-12. Electrical frequency synthesizer 1A14/2A14, overall block diagram.



NOTE  
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN  
FOR COMPLETE DESIGNATION PREFIX WITH MAIN  
(T-1054/GRC-144) OR ZA14 (R-1467/GRC-144).

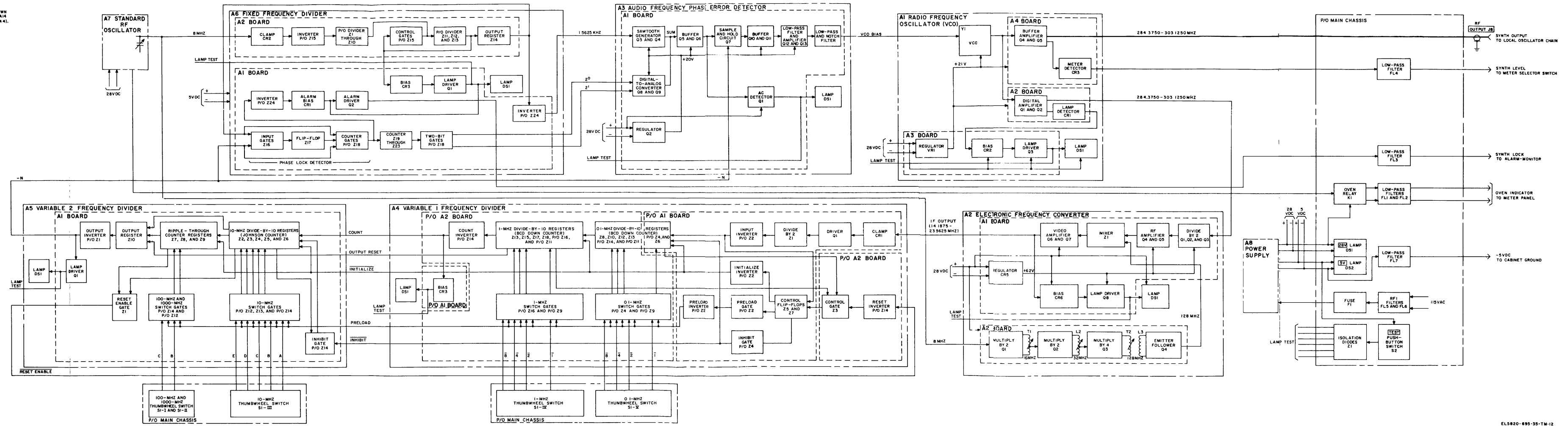
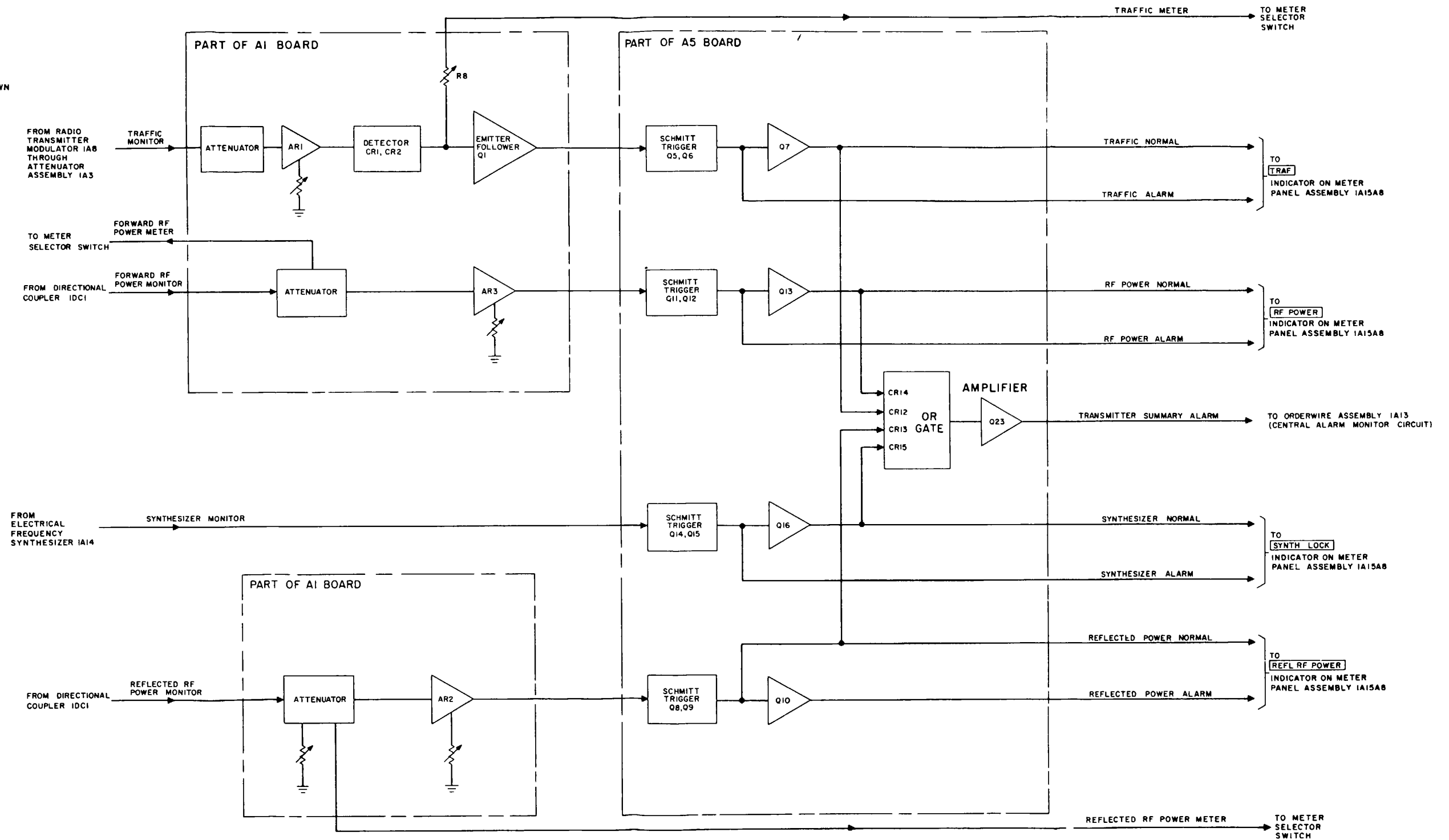


Figure 5-13. Electrical frequency synthesizer 1A14/2A14, functional block diagram.

- NOTES:  
 1 [ ] INDICATES FRONT PANEL MARKING  
 2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATIONS PREFIX WITH 1A5(T-1054/GRC-144), OR 2A12(R-1467/GRC-144)



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Figure 5-14. Alarm monitor 1A5, block diagram.

UNIT 1, TRANSMITTER, RADIO T-1054/GRC-144

- UNLESS OTHERWISE SPECIFIED ALL RESISTANCE VALUES ARE IN OHMS
- REFERENCE DESIGNATIONS OF ASSEMBLIES WHICH ARE NOT PHYSICALLY SHOWN ON DIAGRAM ARE PLATE ASSEMBLY
- UNLESS OTHERWISE SPECIFIED, ALL WIRE SHALL BE STRANDED, TEFLON INSULATED, SIZES AS FOLLOWS  
NO. 16 AWG - FOR 15V AC POWER  
NO. 20 AWG - FOR LOW VOLTAGE AC AND DC AND GROUND  
NO. 22 AWG - FOR ALL OTHER WIRING
- CONTACT ARRANGEMENTS FOR VARIOUS CONNECTORS ARE SHOWN IN TABLE 1 PINS A1, A2, A3 ARE FOR COAX CONTACTS.
- THE SYMBOL  $\times$  P DENOTES TWISTED PAIR
- SWITCH IA15A14 IS VIEWED FROM END OPPOSITE CONTROL KNOB SECTION A IS CLOSEST TO KNOB
- CONTROL, INDICATOR AND SWITCH OUTLINES SHOWING TERMINAL LOCATION ARE PROVIDED BELOW ALL VIEWS ARE FROM WIRING SIDE

TABLE 1 CONNECTOR PIN ARRANGEMENTS (MATING SIDE VIEW)

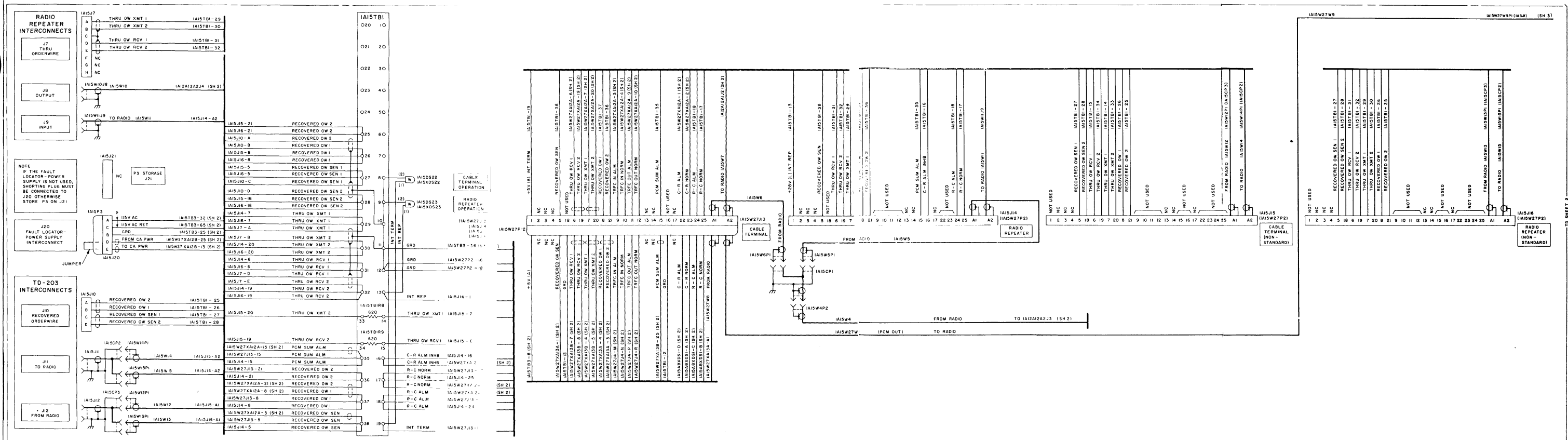
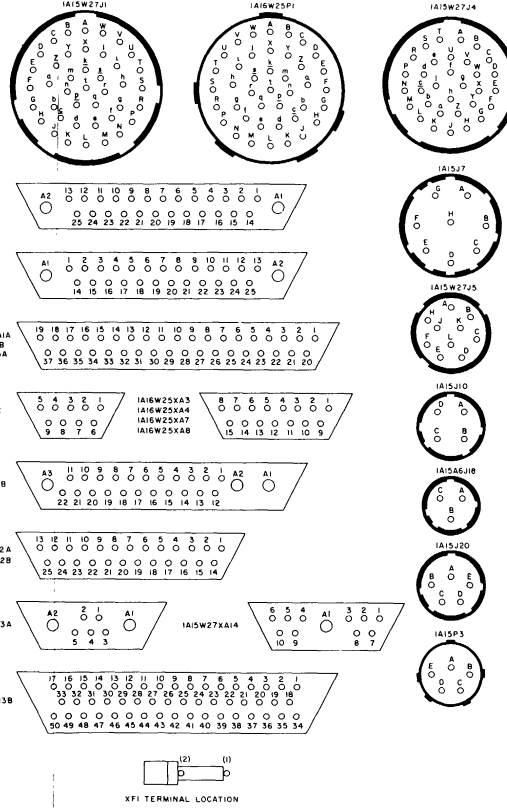


Figure 5-15 (1). Transmitter, Radio T-1054/GRC-144, interconnecting diagram (part 1 of 3).

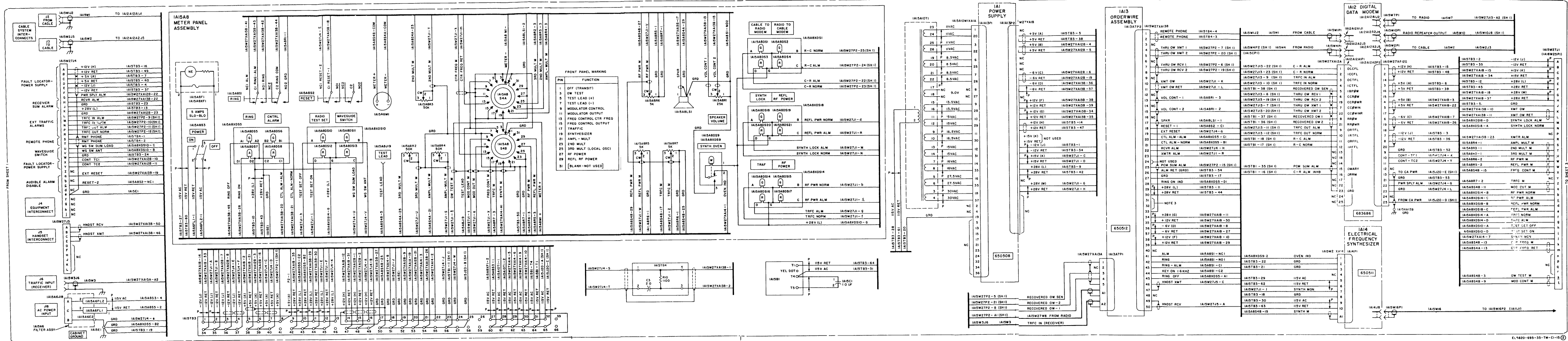


Figure 5-15 (2). Transmitter, Radio T-1054/GRC-144, interconnecting diagram (part 2 of 3)

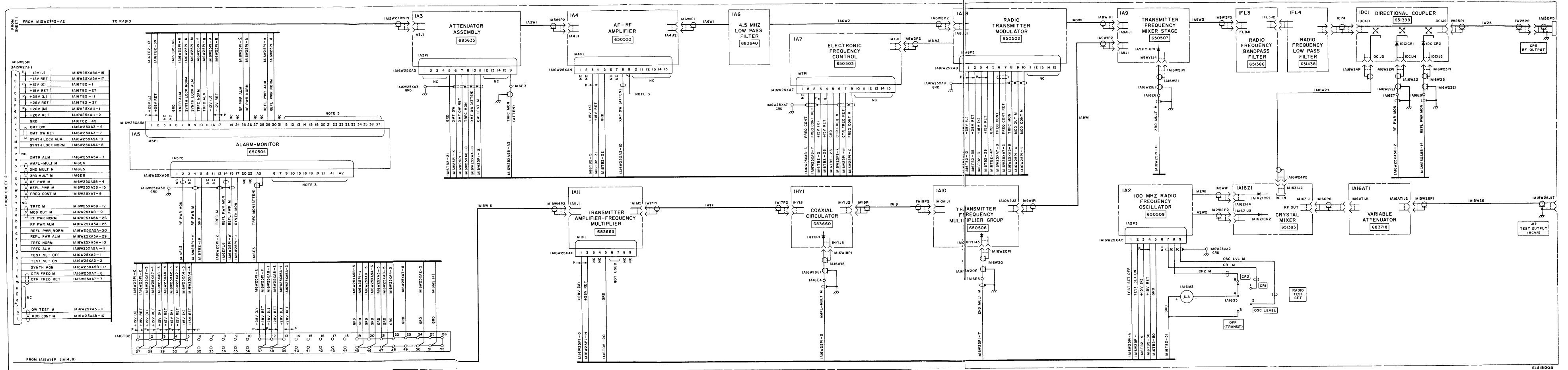


Figure 5-15 (3). Transmitter, Radio T-1054/GRC-144, interconnecting diagram (part 3 of 3).

UNIT 1, TRANSMITTER, RADIO T-1054(PA/GRC-144(V)

- NOTES
- UNLESS OTHERWISE SPECIFIED ALL RESISTANCE VALUES ARE IN OHMS
  - REFERENCE DESIGNATIONS OF ASSEMBLIES WHICH ARE NOT PHYSICALLY SHOWN ON DIAGRAM  
 IA18 - PLATE ASSEMBLY  
 IA18 - CABINET, ELECTRICAL EQUIPMENT  
 IA18W25 - WIRING HARNESS, BRANCHED (PLATE ASSY)  
 IA18A10W1 - WIRING HARNESS, BRANCHED (AC WIRING BETWEEN IA18A10T1 AND IA18A10W1A1)  
 IA18W27 - WIRING HARNESS, BRANCHED (CABINET, MAIN WIRING HARNESS)
  - TERMINALS INDICATED ARE USED FOR INTERNAL MODULE CONNECTIONS. DO NOT CONNECT EXTERNALLY.
  - UNLESS OTHERWISE SPECIFIED, ALL WIRE SHALL BE STRANDED, TEFLON INSULATED, SIZES AS FOLLOWS  
 NO. 18 AWG - FOR 15V AC POWER  
 NO. 20 AWG - FOR LOW VOLTAGE AC AND DC AND GROUND  
 NO. 22 AWG - FOR ALL OTHER WIRING.
  - CONTACT ARRANGEMENTS FOR VARIOUS CONNECTORS ARE SHOWN IN TABLE 1. PINS A1, A2, A3 ARE FOR COAX CONTACTS.
  - THE SYMBOL  $\leftarrow$  P DENOTES TWISTED PAIR
  - SWITCH IA18A54 IS VIEWED FROM END OPPOSITE CONTROL KNOB SECTION A IS CLOSEST TO KNOB
  - CONTROL INDICATOR AND SWITCH OUTLINES SHOWING TERMINAL LOCATION ARE PROVIDED BELOW ALL VIEWS ARE FROM WIRING SIDE
  - [ 3 ] INDICATES CROSS REFERENCE SHEET NUMBER

TABLE 1 CONNECTOR PIN ARRANGEMENTS (MATING SIDE VIEW)

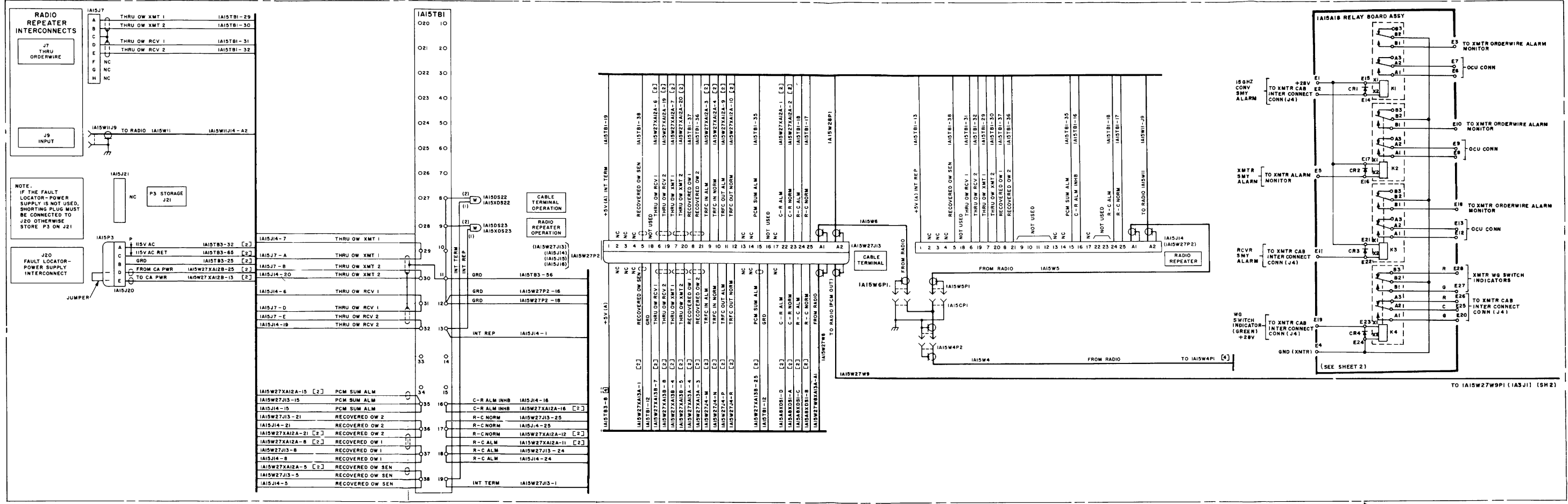
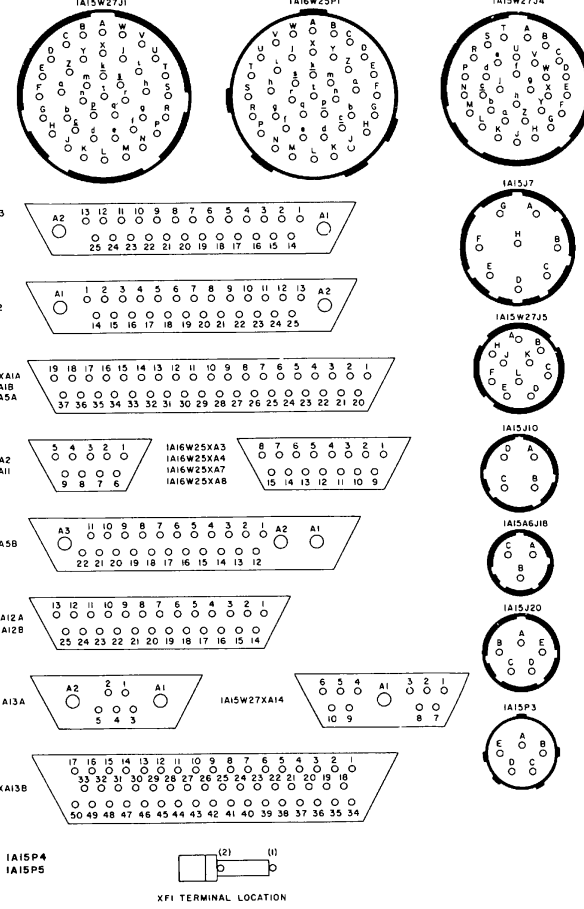


Figure 5-15.1 (1). Transmitter, Radio T-1054 (P) A/GRC-144(V) interconnecting diagram (sheet 1 of 4).

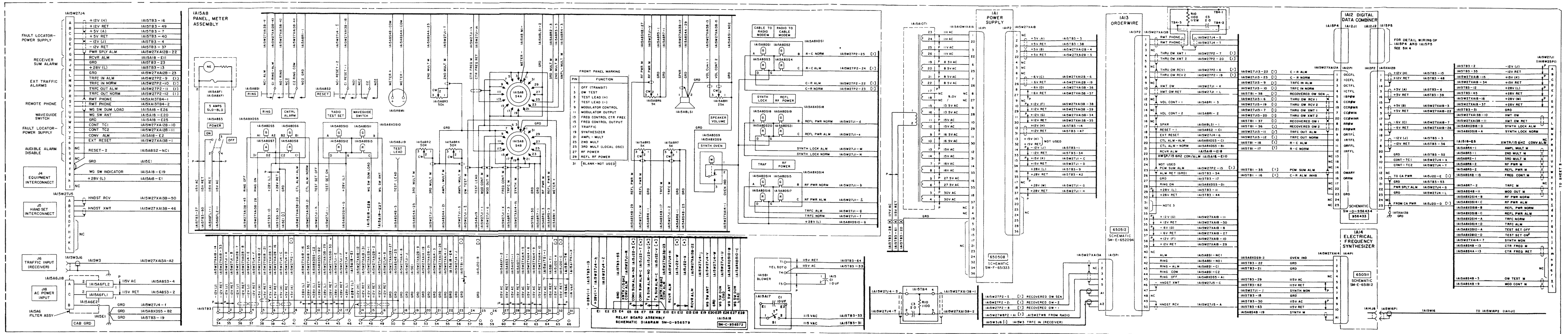


Figure 5-15.1 (2). Transmitter, Radio T-1054 (P) A/GRC-144 (V) interconnecting diagram (sheet 2 of 4).

Change 6 5-35.3

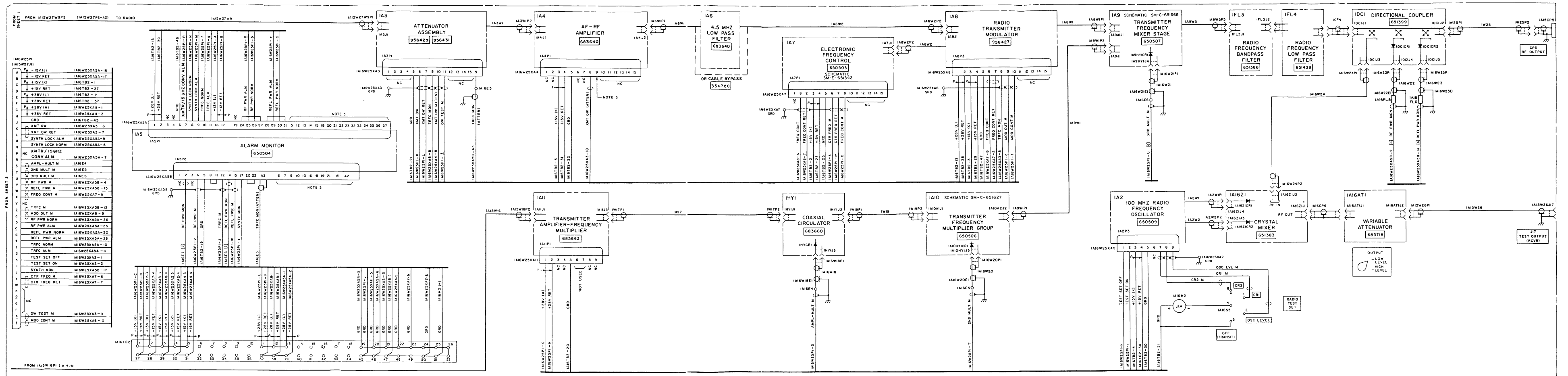


Figure 5-15.1(3). Transmitter, Radio T-1054 (P) A/GRC-144 (V) interconnecting diagram (sheet 3 of 4).

Change 6 5-35.5



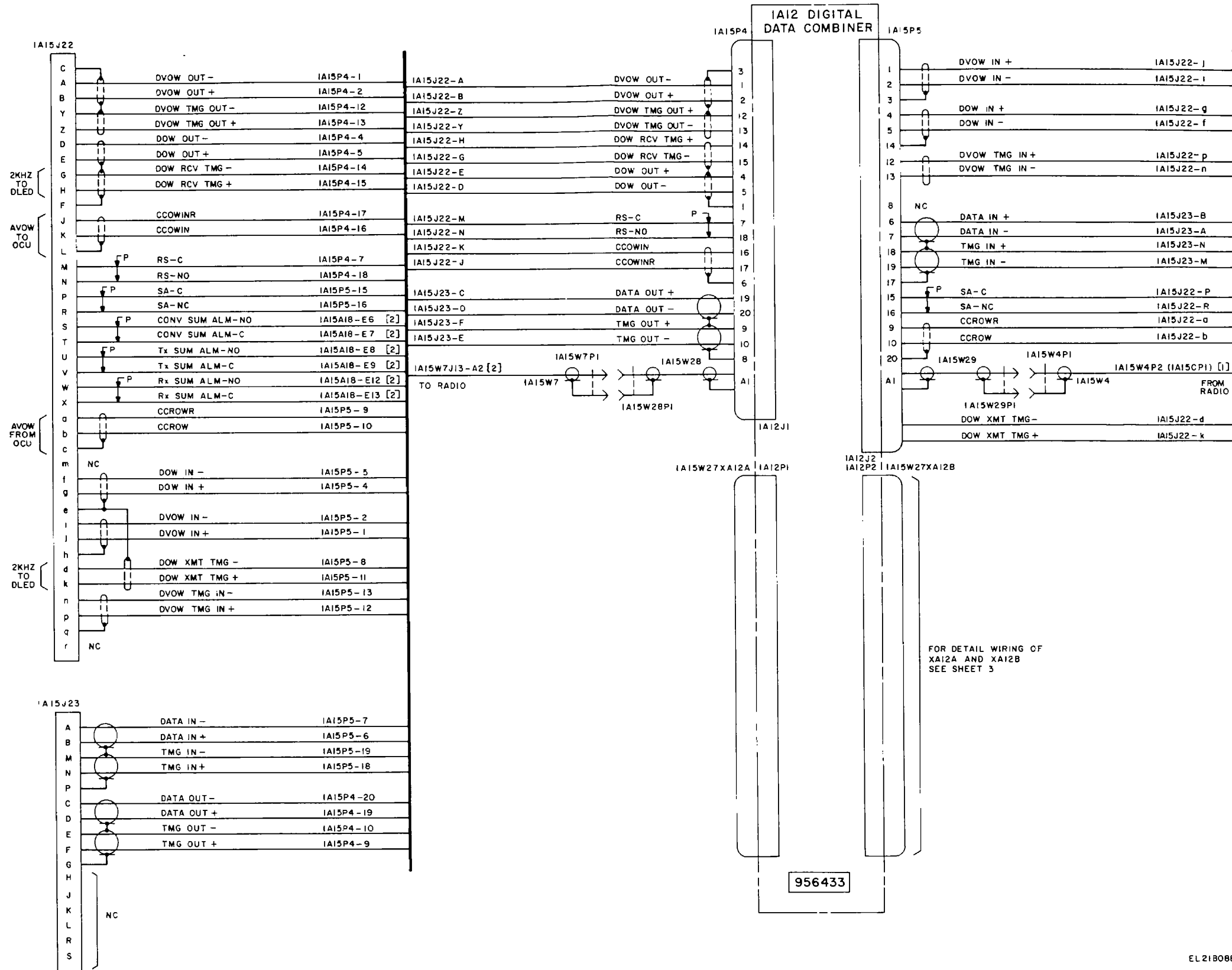
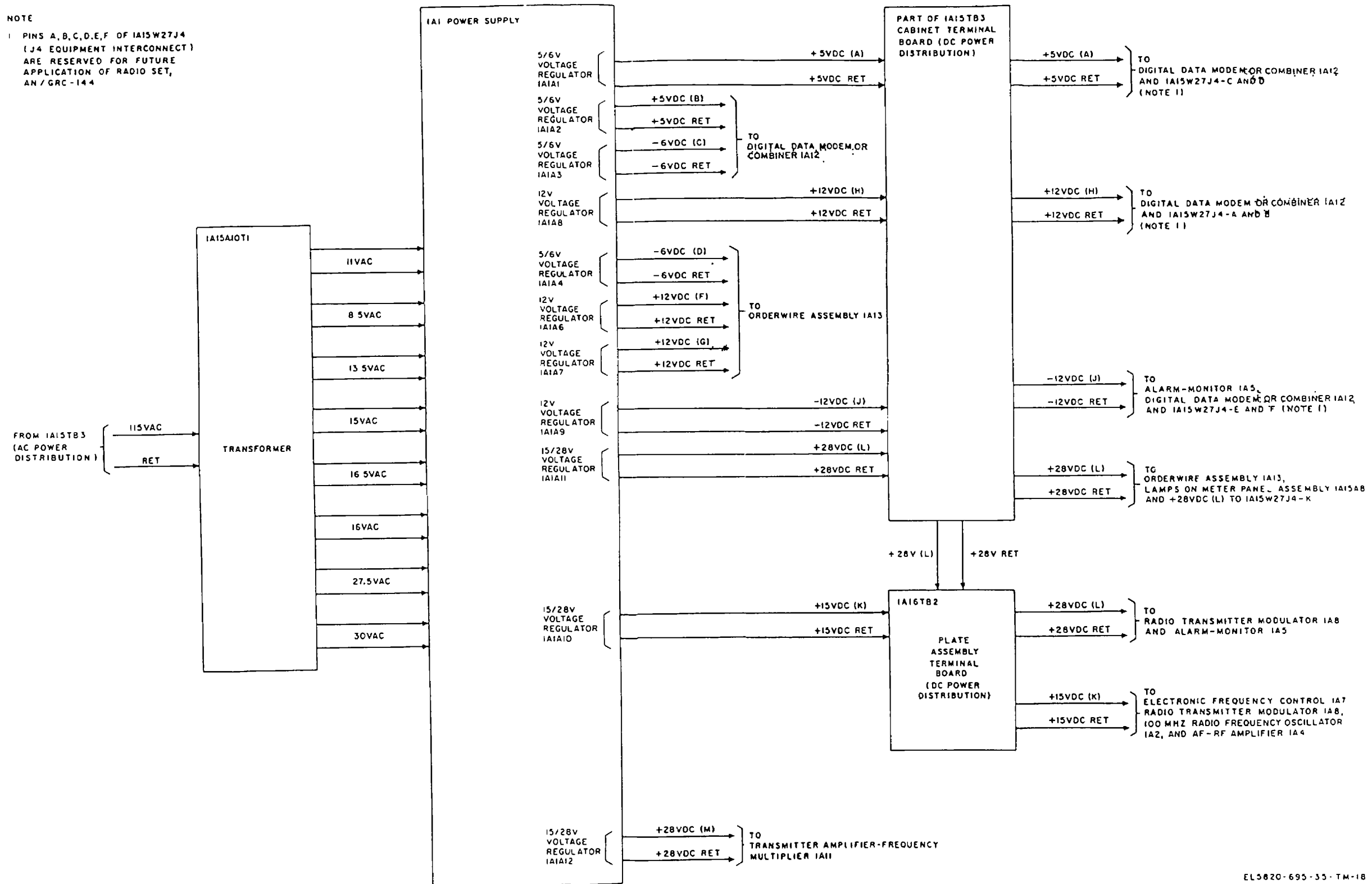


Figure 5-15.1 (4). Transmitter, Radio T-1054 (P) A/GRC-144 (V) interconnecting diagram (Sheet 4 of 4).

NOTE

1 PINS A, B, C, D, E, F OF IA15W27J4 (J4 EQUIPMENT INTERCONNECT) ARE RESERVED FOR FUTURE APPLICATION OF RADIO SET, AN / GRC -144



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Figure 5-16. Transmitter, Radio T-1054 (P) /GRC-144 (V) and T-1054 (P) A/GRC-144 (V) dc power distribution.

- NOTES  
 1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE REFERENCE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION.  
 2. ALL WIRE IS NO. 20 AWG STRANDED, TEFLON INSULATED, EXCEPT FOR WIRES ON J1 THRU J12 AND XDS1 THRU XDS12 WHICH IS NO. 24 AWG.  
 3. CONNECTORS ON A1 THRU A12 ARE ETCHED CONTACTS ON PRINTED WIRING BOARD.  
 4. UNLESS OTHERWISE SPECIFIED RESISTANCE VALUES ARE IN OHMS.

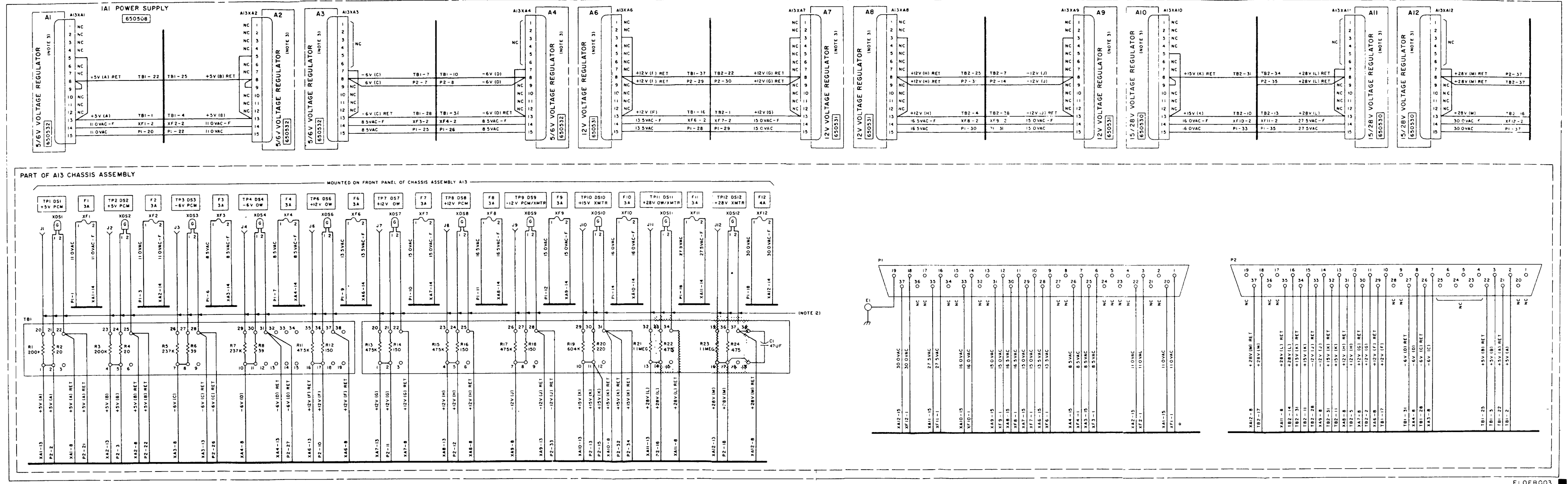




Figure 5-17. Power supply 1A1, interconnecting diagram.

NOTES

- 1  INDICATES FRONT PANEL MARKING
- 2 CONTROLS ON 2FL4, 2FL5, 2FL6, AND 2A14 ARE SET TO THE DESIRED OPERATING FREQUENCY IN THE 4.4 TO 5.0 GHZ RANGE
- 3 CONTROL ON 2A11 IS SET TO THE DESIRED OUTPUT SIGNAL LEVEL
- 4  INDICATES ADJUSTABLE CONTROL

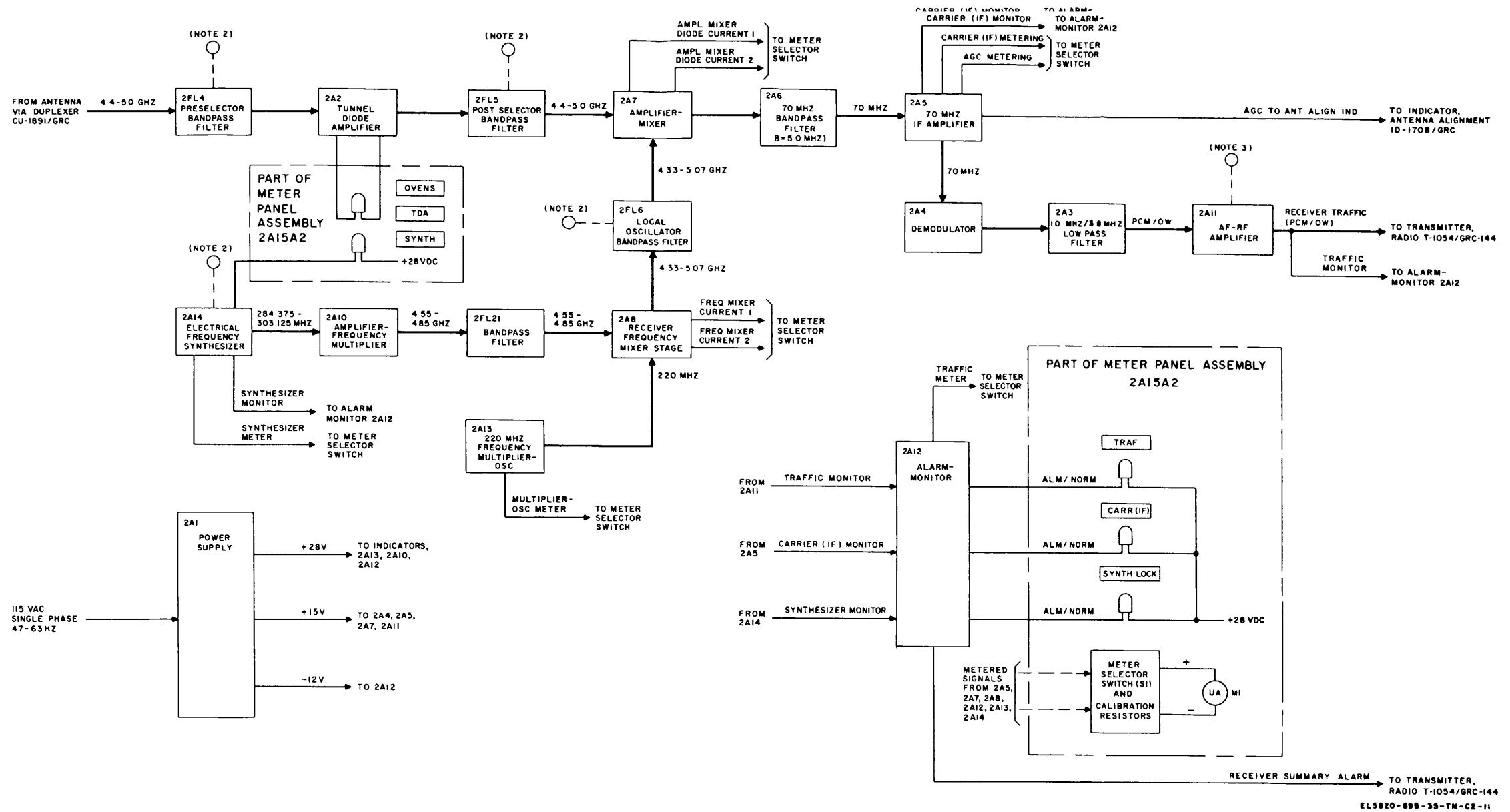


Figure 5-18. Receiver, Radio R-1467/GRC-144, overall block diagram.

NOTES

- 1 [ ] INDICATES FRONT PANEL MARKING
- 2 CONTROLS ON 2FL4, 2FL5, 2FL6 AND 2A14 ARE SET TO THE DESIRED OPERATING FREQUENCY IN THE 4.4 TO 5.0 GHZ RANGE
- 3 CONTROL ON 2A11 IS SET TO THE DESIRED OUTPUT SIGNAL LEVEL
- 4 [ ] INDICATES ADJUSTABLE CONTROL
- 5 LOW PASS FILTER USED IN POSITION 2A3 DEPENDS UPON DATA RATE AS FOLLOWS

DATA RATE (MB/S)	USE FILTER
1-2	1.0 MHZ
4-5	3.0 MHZ
9	5.3 MHZ
18	13.0 MHZ

- 6 BANDPASS AND DATA RATE DETERMINE FILTER TO BE USED IN POSITION 2A6 AS NOTED BELOW.

FILTER PART NUMBER	BANDPASS (MHZ)	DATA RATE MB/S
680047	5.0	1-5
956417	10.6	9
956462	-	18

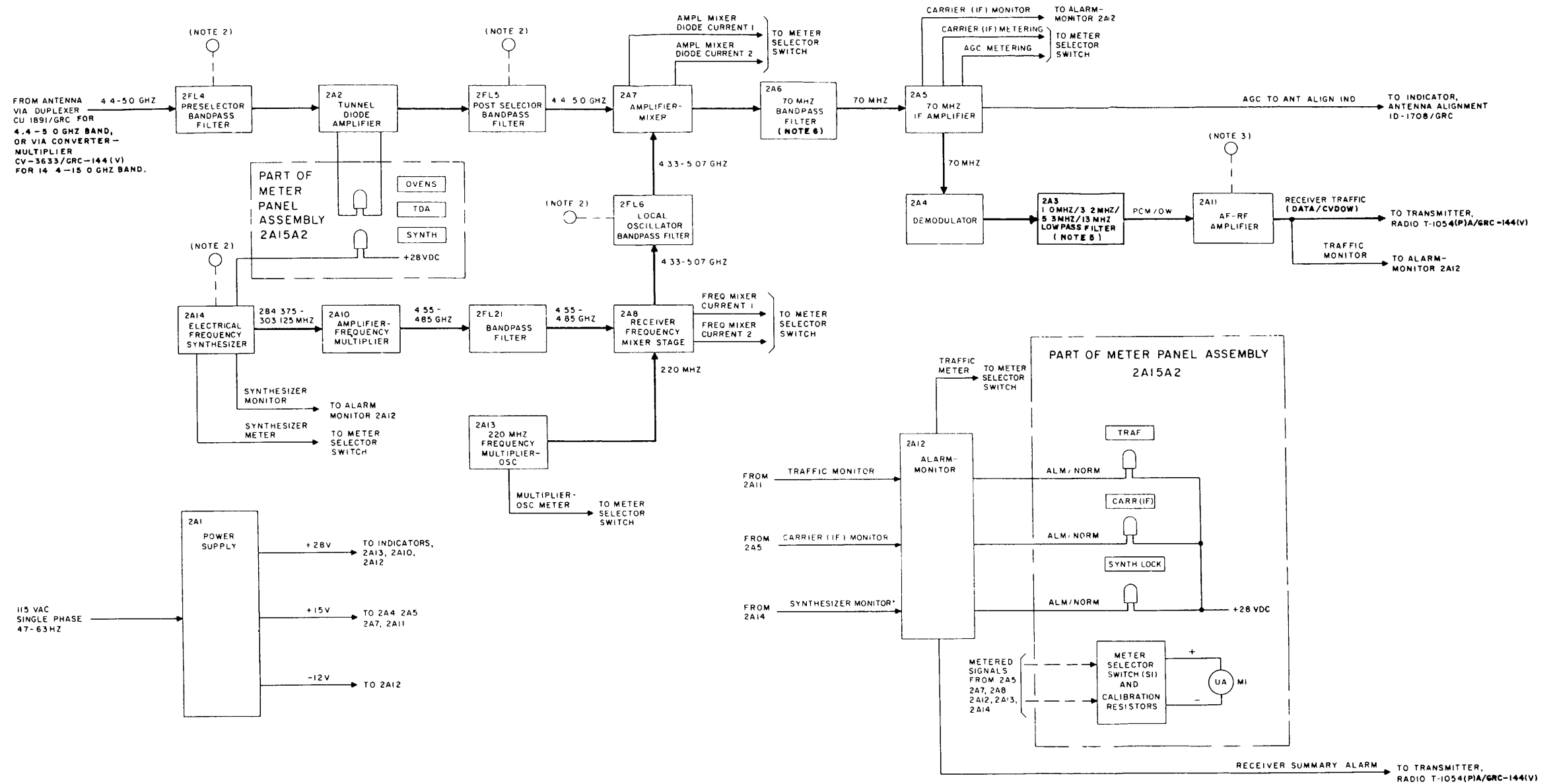


Figure 5-18.1. Receiver, Radio R-1467 (P) A/GRC-144 (V) overall block diagram.

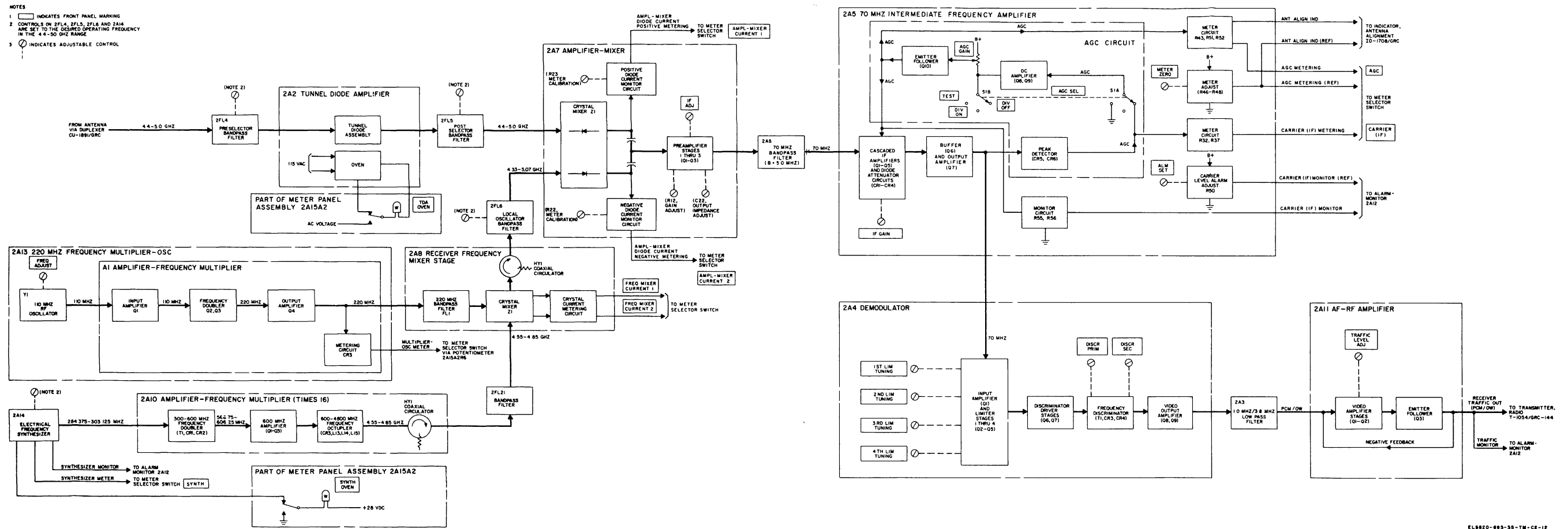


Figure 5-19. Receiver, Radio R-1467/GRC-144, functional block diagram.  
Change 1 5-43

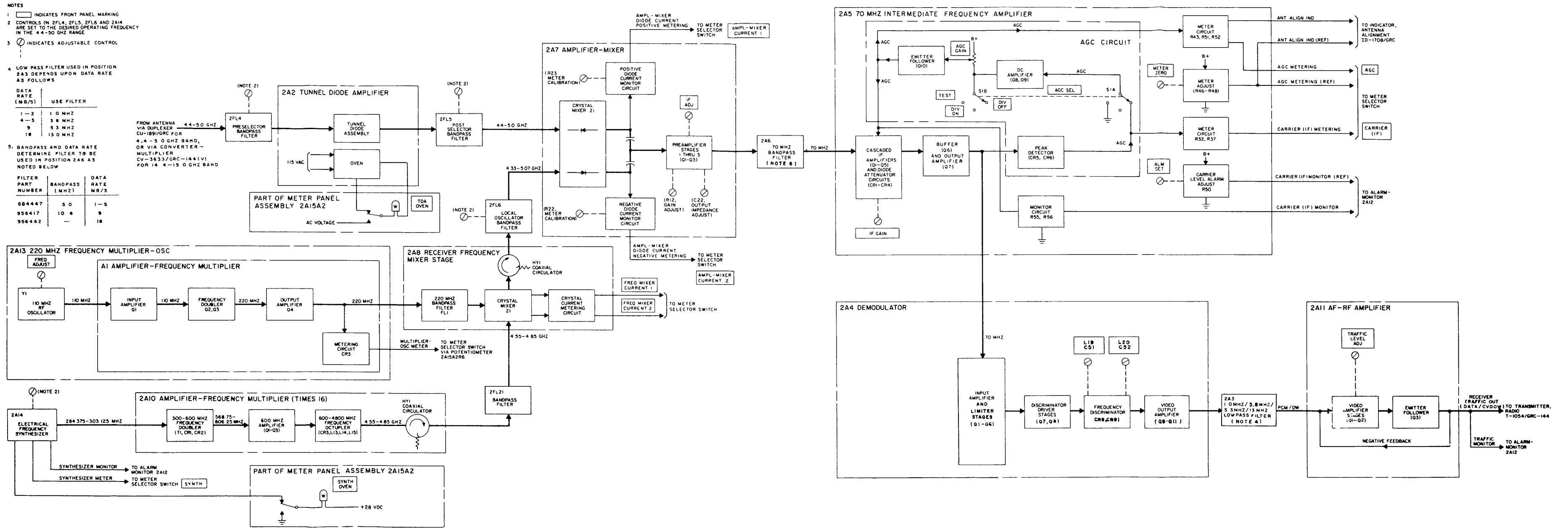


Figure 5-19.1. Receiver, Radio R-1467(P)/GRC-144(V), functional block diagram.

NOTES

- 1  INDICATES FRONT PANEL MARKING
- 2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN PREFIX REFERENCE DESIGNATIONS WITH 2A12

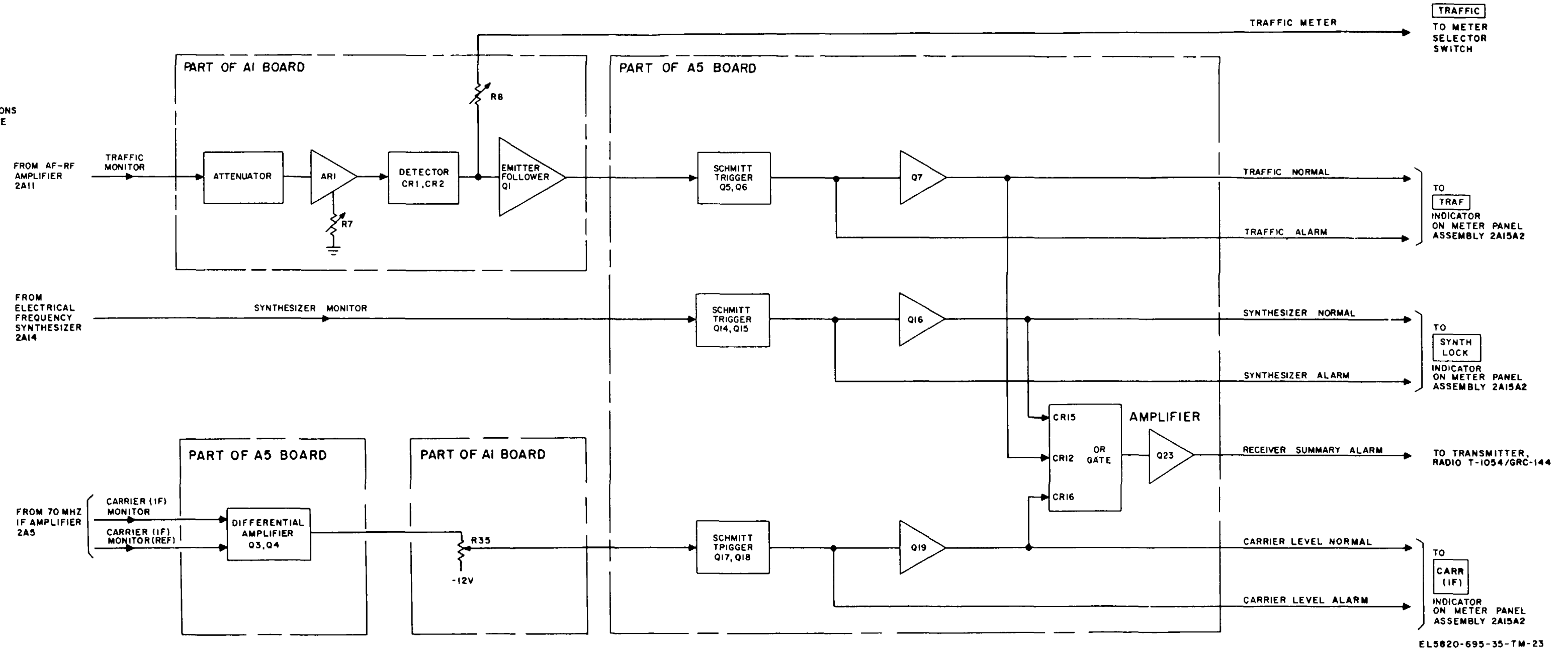


Figure 5-20. Alarm monitor 2A12, block diagram.



UNIT 2  
RECEIVER, RADIO R-1467/GRC-144

- NOTES
- UNLESS OTHERWISE SPECIFIED RESISTANCE VALUES ARE IN OHMS
  - CIRCUIT REFERENCES NOT SHOWN ARE CURRENT ELECTRICAL EQUIPMENT (SEE RECEIVER)
  - TERMINALS INDICATED ARE USED FOR INTERMEDIATE CONNECTIONS DO NOT CONNECT EXTERNALLY
  - UNLESS OTHERWISE SPECIFIED ALL WIRE SHALL BE STRANDED TELEFON MULTIPLE SIZE AS FOLLOWS: NO. 16 AND FOR 115V AC POWER NO. 18 AND FOR LOW VOLTAGE AC AND DC AND GROUND NO. 22 AND FOR ALL OTHER WIRING NO. 22 AND FOR ALL OTHER WIRING
  - CONTACT ARRANGEMENTS FOR VARIOUS CONNECTORS ARE SHOWN ON TABLE 1
  - INDICATES MARKING ON EQUIPMENT
  - THE SYMBOL  $\ominus$  DENOTES TWISTED PAIR
  - SWITCH ZAI5A23 IS VIBRATED FROM END OPPOSITE CONTROL WIND MOTOR A IS CLOSEST TO WIND
  - CONTROL INDICATOR AND SWITCH OUTLINE DRAWING TERMINAL LOCATIONS ARE PROVIDED BELOW ALL VIEWS FROM WIND SIDE

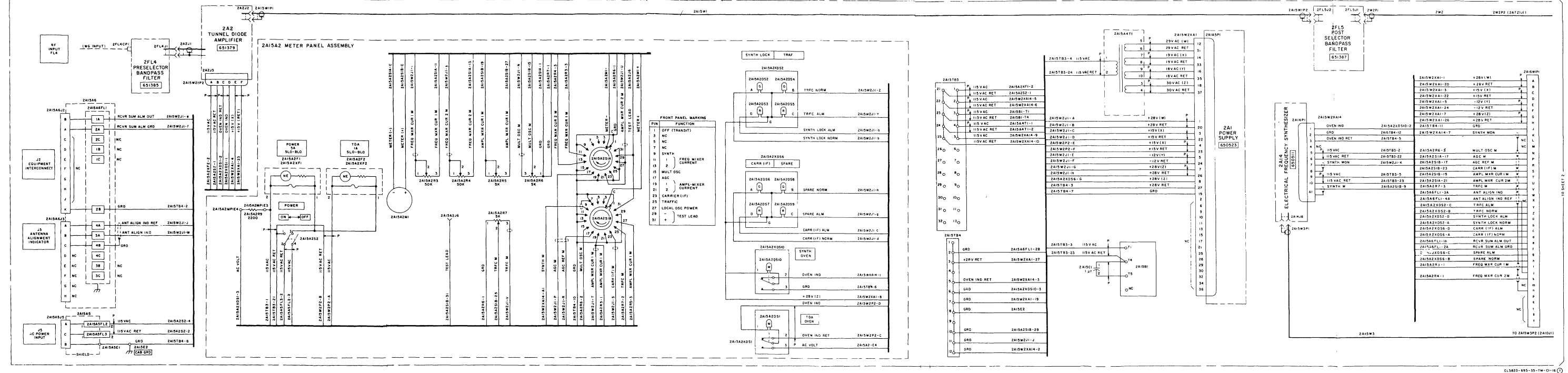
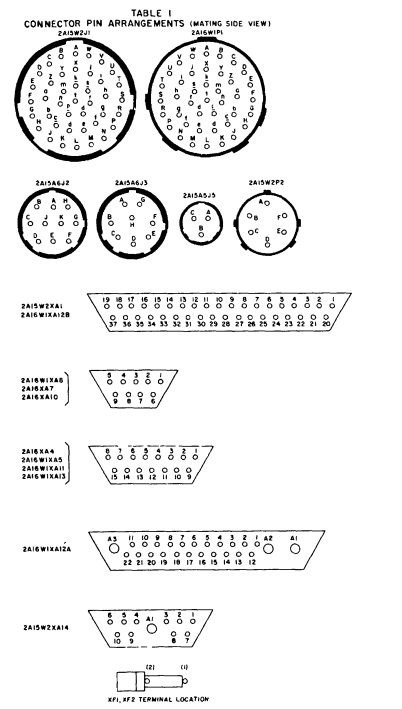


Figure 5-21 (1). Receiver, Radio R-1467/GRC-144, interconnecting diagram (part 1 of 2)

Change 1 5-47

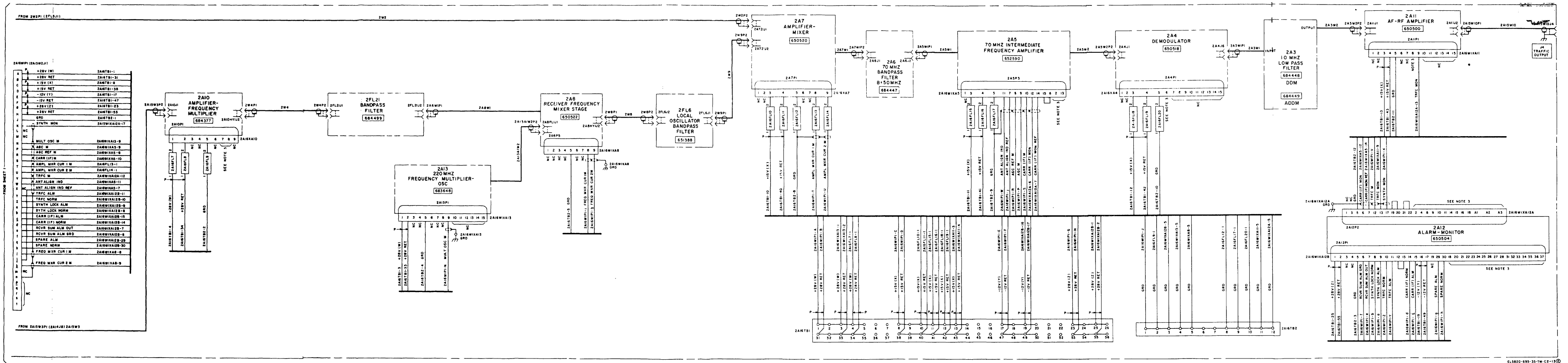


Figure 5-21 (2).Receiver, Radio R-1467/GRC-144, interconnecting diagram (part 2 of 2).

UNIT 2  
RECEIVER, RADIO R-1467(P)A/GRC-144(V)

NOTES

1 RECEIVER, RADIO R-1467/GRC-144 AND R-1467(P)A/GRC-144(V) INTERCONNECTION DIAGRAMS (FIG 5-21) ARE IDENTICAL EXCEPT AS INDICATED WITHIN DASH AREAS

2 LOW PASS FILTER USED IN POSITION 2A3 DEPENDS UPON DATA RATE AS FOLLOWS

DATA RATE (MB/S)	USE FILTER	FILTER PART NUMBER
1-2	10 MHz	684448
4-5	3.8 MHz	684449
9	5.3 MHz	956419
18	13.0 MHz	956421

3 BANDPASS AND DATA RATE DETERMINE FILTER TO BE USED IN POSITION 2A6 AS NOTE BELOW

FILTER PART NUMBER	BANDPASS (MHZ)	DATA RATE MB/S
684447	5.0	1-5
956417	10.6	9
956462	-	18

4 RECEIVER, RADIO R-1467(P)A/GRC-144(V) UP-GRADED MODULES ARE AS FOLLOWS

MODULE	PART NUMBER
DEMODULATOR	956415
IF AMPLIFIER	956423
AMPL - MIXER	956425

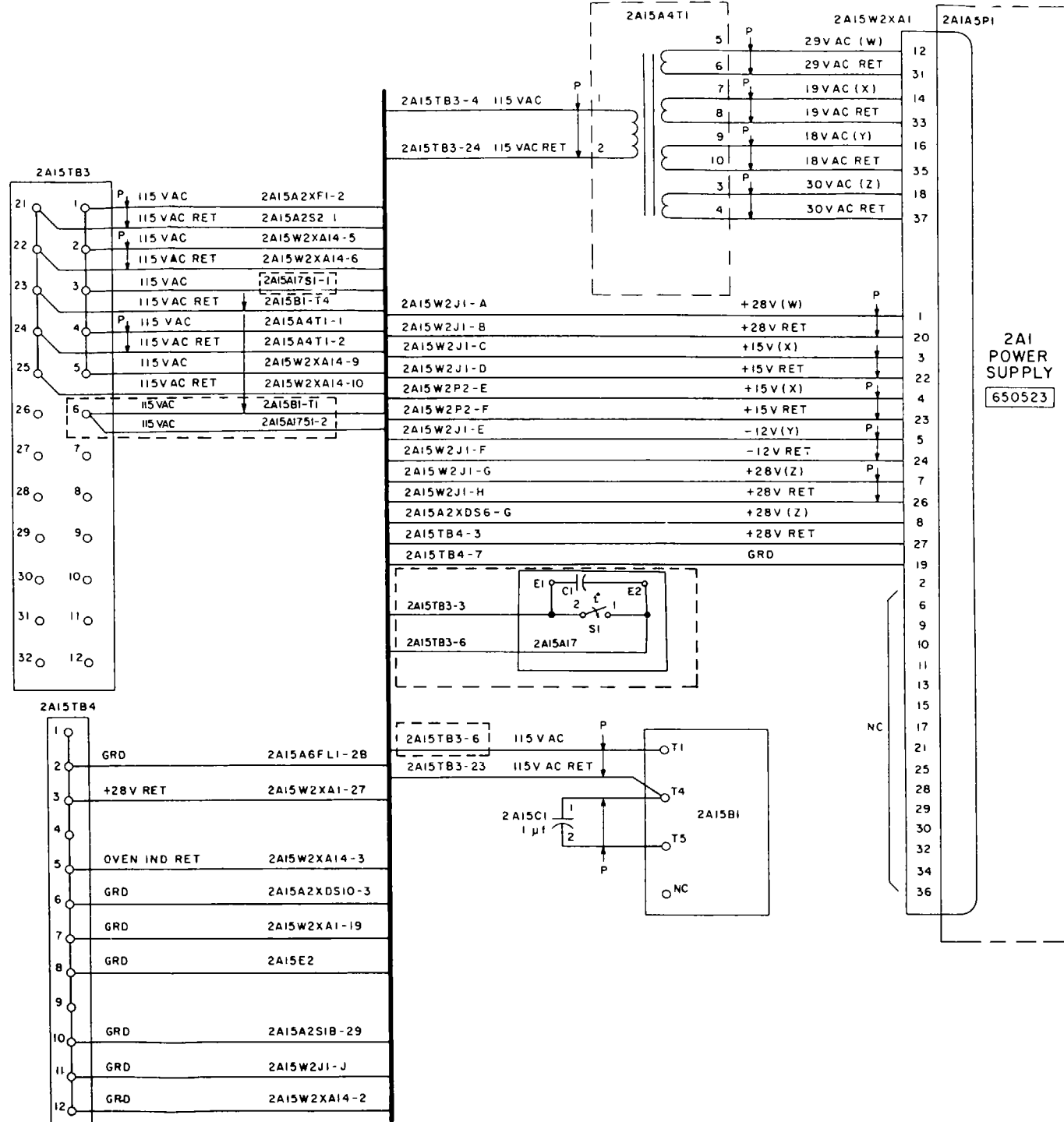


Figure 5-21.1.Receiver, Radio R-1467 (P) A/GRC-144 (V), interconnecting diagram.  
Change 6 5-49.1

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- NOTES
- 1 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION. PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION
  - 2 ALL WIRE IS NO 20 AWG STRANDED WIRE, TEFLON INSULATED EXCEPT FOR WIRES ON J1 TO J4 AND XDS1 TO XDS4 WHICH IS NO 24 AWG
  - 3 CONNECTORS ON A1 THRU A4 ARE ETCHED CONTACTS ON PRINTED WIRING BOARD
  - 4 UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS
  - 5   INDICATES MARKING ON EQUIPMENT

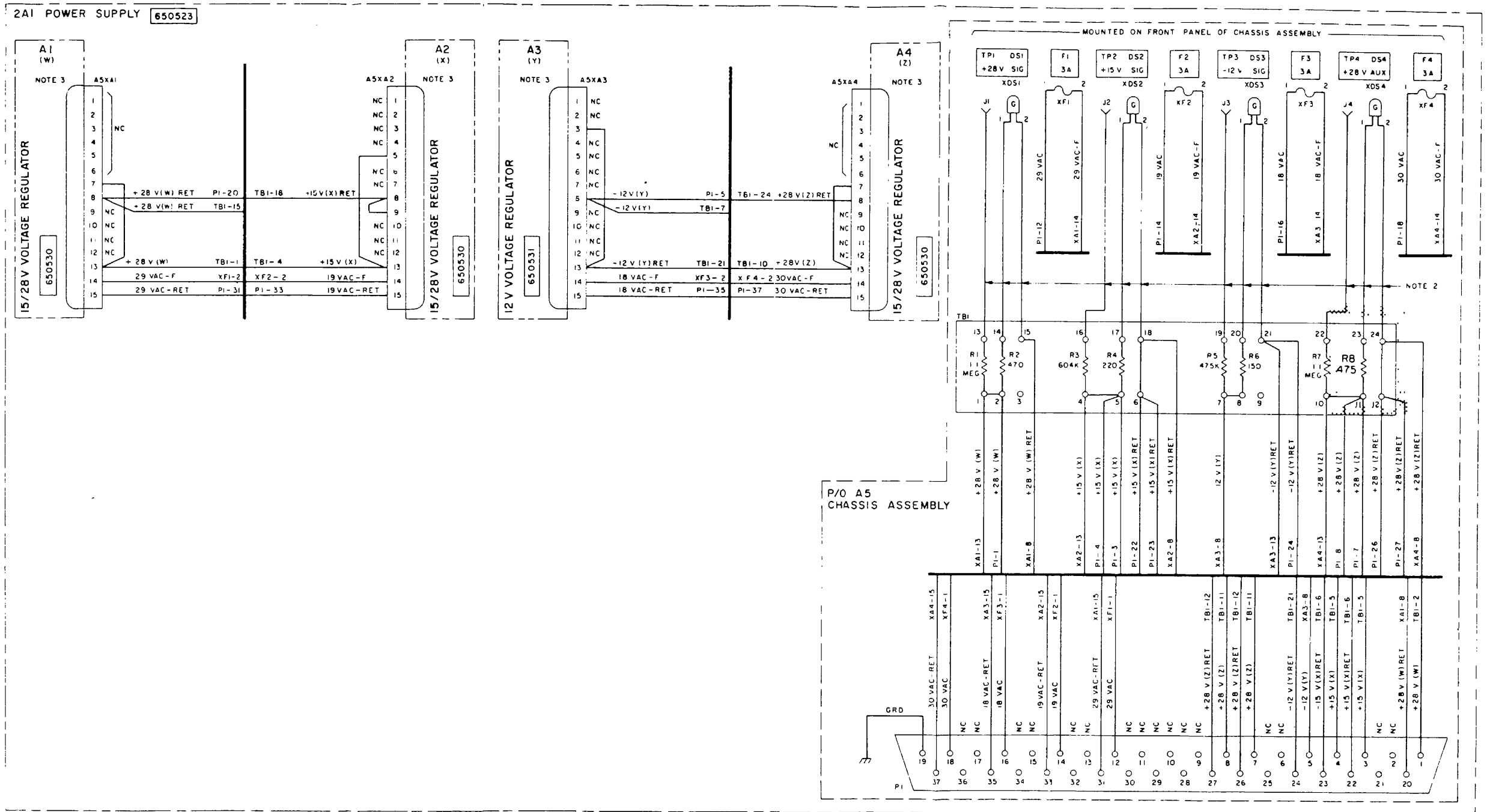


Figure 5-22. Power supply 2A1, interconnecting diagram

- NOTES
- 1 UNLESS OTHERWISE SPECIFIED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS, INDUCTANCES ARE IN MICROHENRIES
  - 2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, PREFIX REFERENCE DESIGNATIONS WITH 1A2
  - 3    INDICATES MARKING ON EQUIPMENT
  - 4 CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM-B-653389

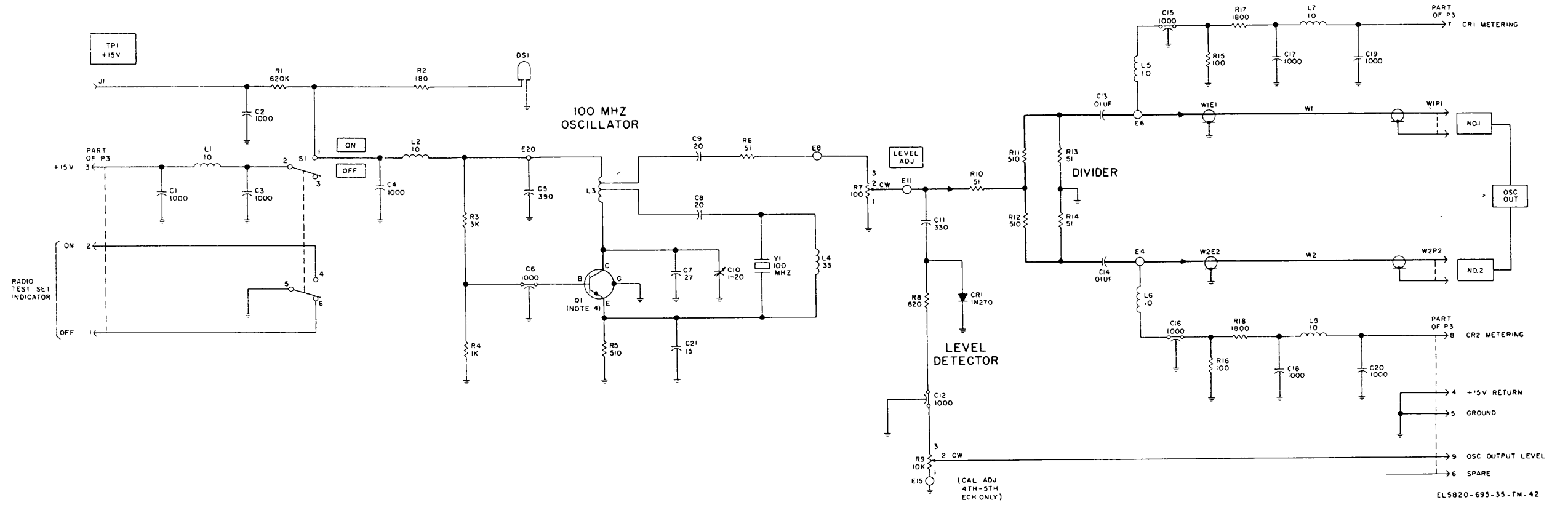
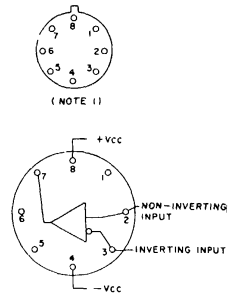


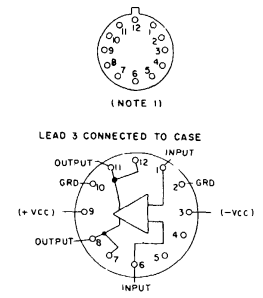
Figure 5-23. 100 MHz radio frequency oscillator 1A2, schematic diagram.

NOTES  
 1 DENOTES PIN LOCATION AS VIEWED FROM BOTTOM (PIN SIDE) OF INTEGRATED CIRCUIT  
 2 DENOTES PIN LOCATION AS VIEWED FROM TOP (OPPOSITE PIN SIDE) OF INTEGRATED CIRCUIT

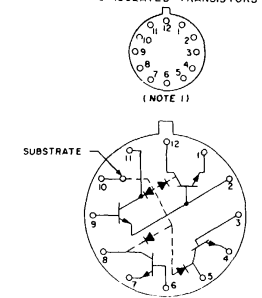
U5B771031X OR LM710  
 HIGH SPEED DIFFERENTIAL  
 COMPARATOR



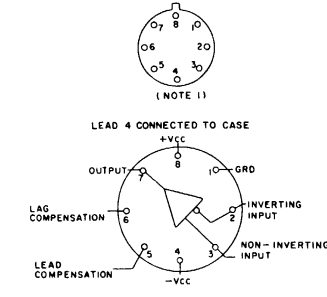
CA3001  
 DIFFERENTIAL AMPLIFIER



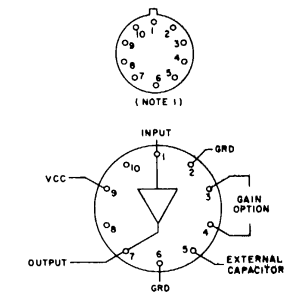
80286  
 LINEAR ARRAY-  
 DARLINGTON PAIR  
 AND  
 TWO ISOLATED TRANSISTORS



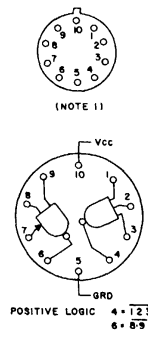
U5B770231X  
 OPERATIONAL AMPLIFIER



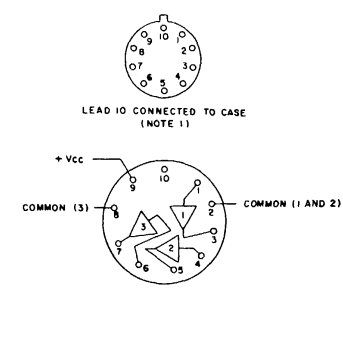
MC1553G  
 LINEAR AMPLIFIER



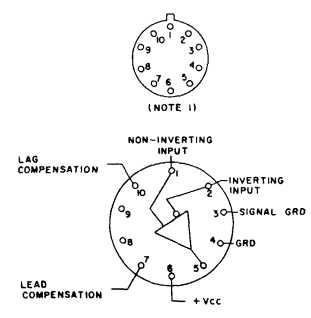
MC944G



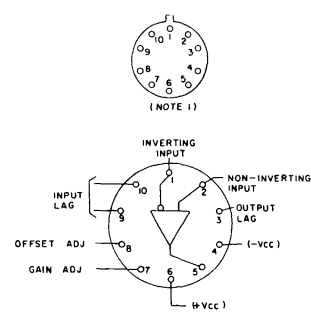
CA3035  
 3-IN-1 WIDEBAND  
 AMPLIFIER ARRAY



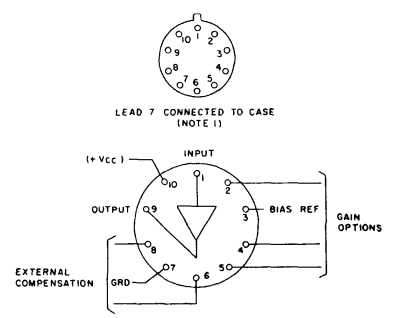
MC1531G  
 OPERATIONAL AMPLIFIER



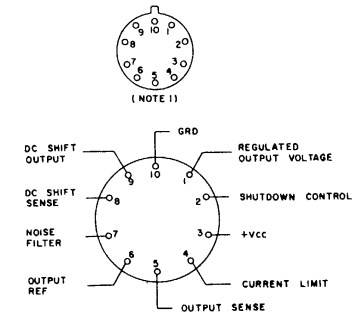
MC1533G  
 OPERATIONAL AMPLIFIER



MC1554G  
 ONE WATT  
 POWER AMPLIFIER



MC1560G  
 VOLTAGE REGULATOR



MD2905  
 DUAL PNP

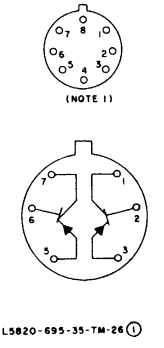


Figure 5-24. (1). Radio Set AN/GRC-144 integrated circuits, schematic diagrams (part 1 of 5).

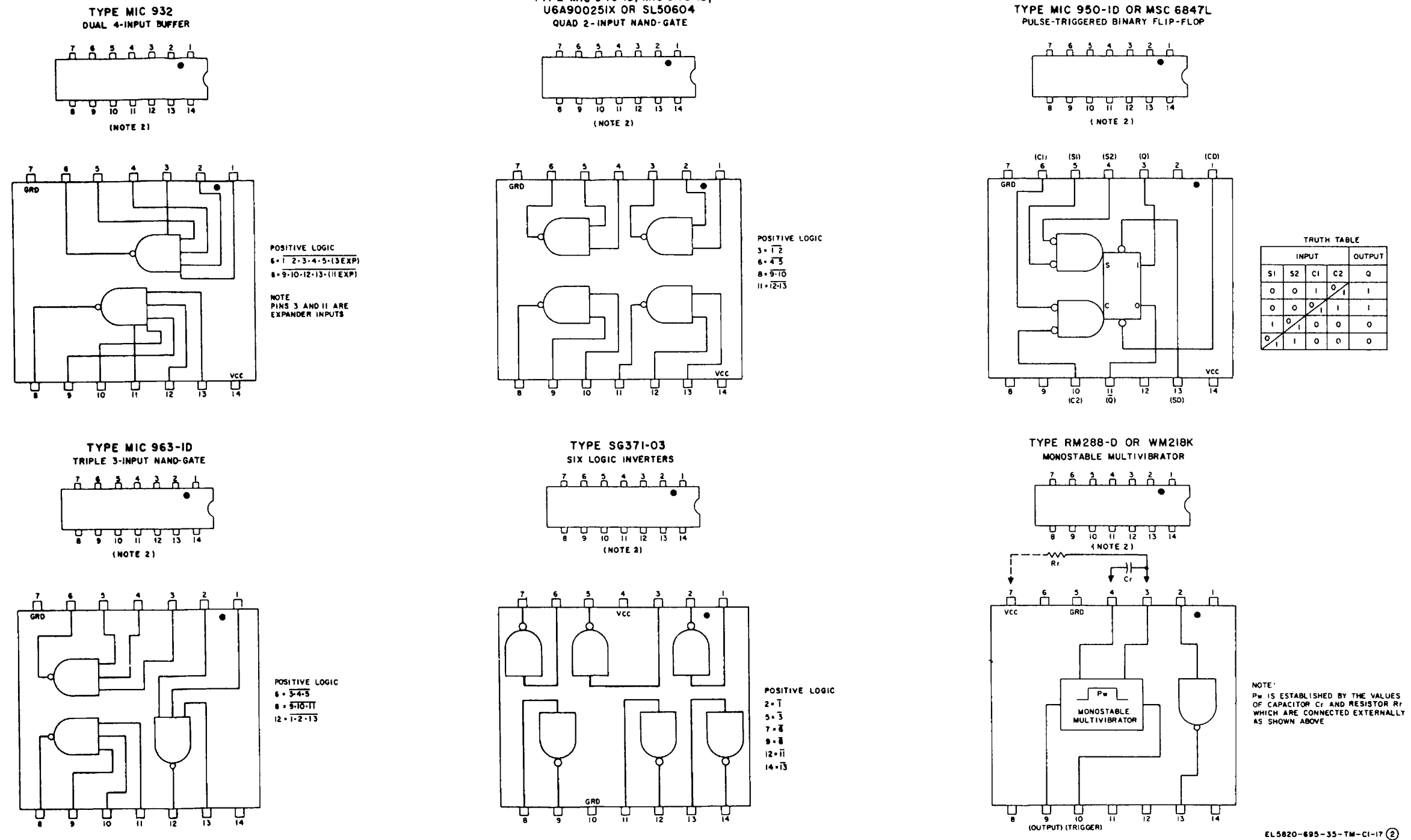


Figure 5-24. (2). Radio Set AN/GRC-144 intergrated circuits, schematic diagrams (part 2 of 5).

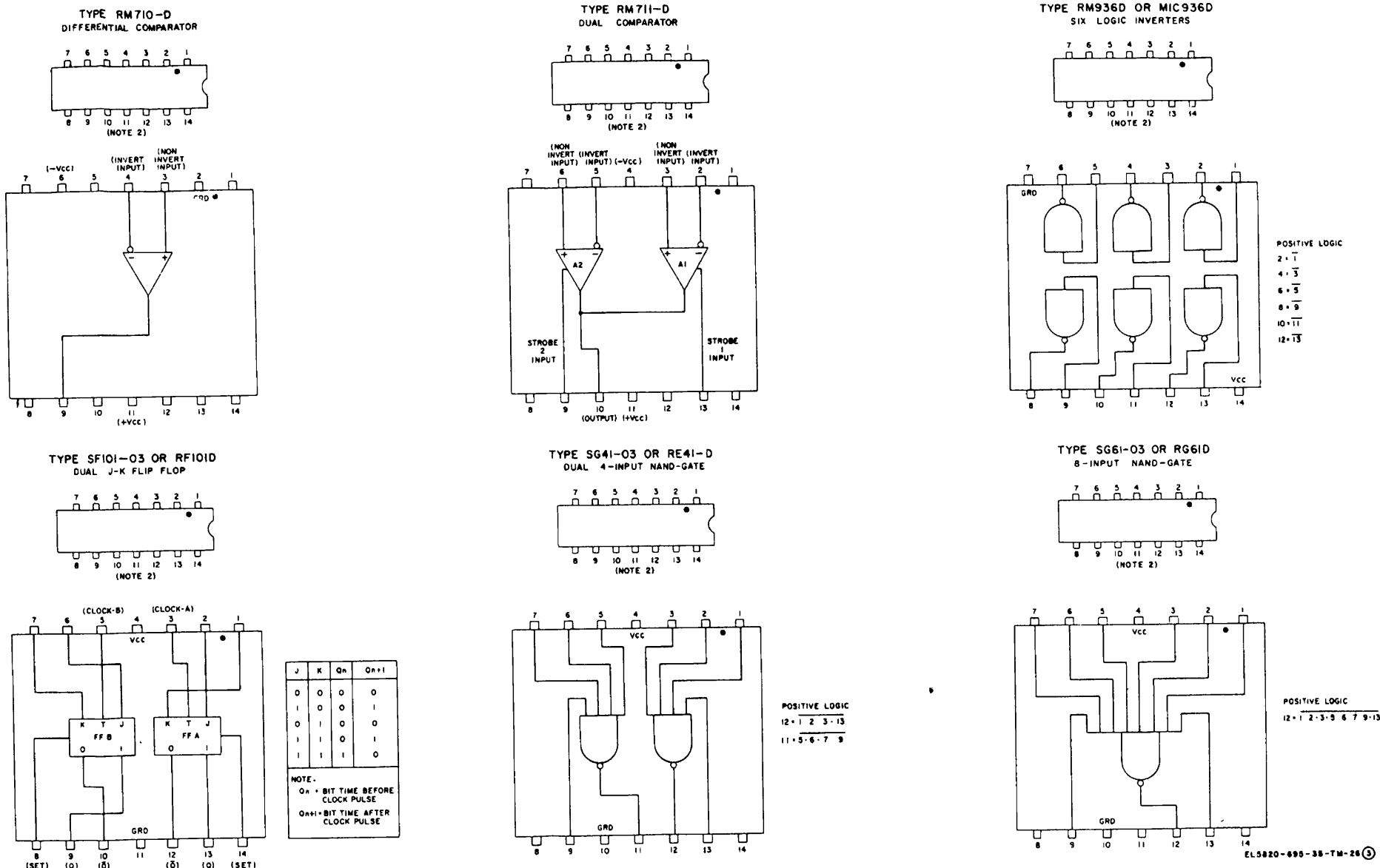
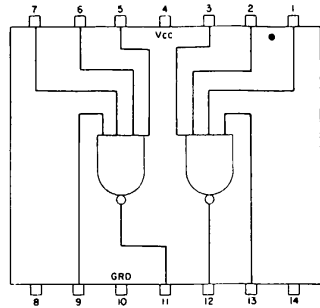
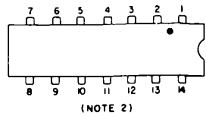


Figure 5-24. (3). Radio Set AN/GRC -144 integrated circuits, schematic diagrams (part 3 of 5)

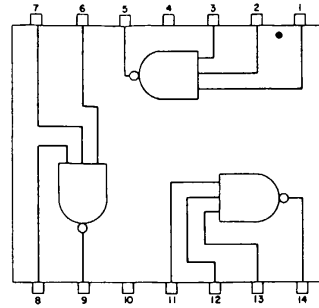
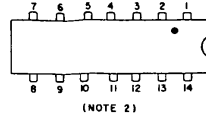


TYPE SG130-03 OR RG130D  
DUAL 4-INPUT NAND-GATE



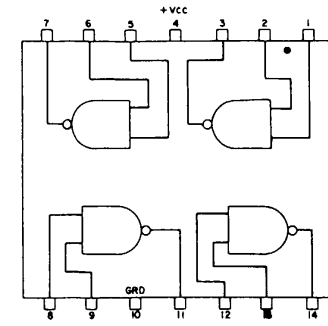
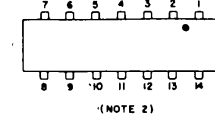
POSITIVE LOGIC  
12 = 1-2-3-13  
11 = 5-6-7-9

TYPE SG191-03 OR RG191D  
TRIPLE 3-INPUT NAND-GATE



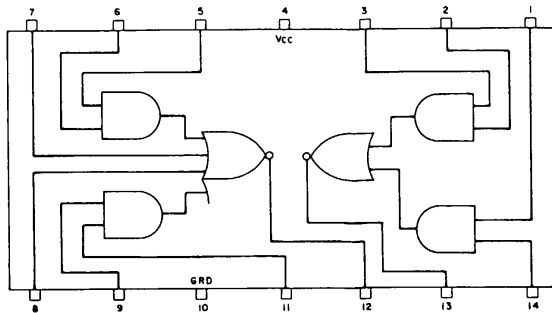
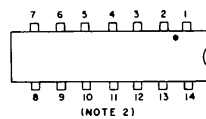
POSITIVE LOGIC  
5 = 1-2-3  
9 = 6-7-8  
14 = 11-12-13

TYPE SG221-03, SG141-03 OR RG141D  
QUAD 2-INPUT NAND-GATE



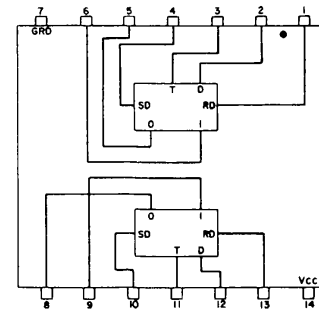
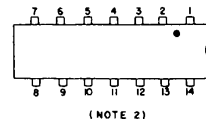
POSITIVE LOGIC  
3 = 1-2  
7 = 5-6  
10 = 8-9  
14 = 12-13

TYPE SG71-03 OR RG71D



POSITIVE LOGIC  
12 = 5-6 + 9-11 + 7-8  
13 = 2-3 + 1-4

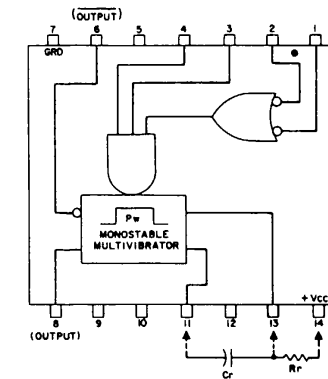
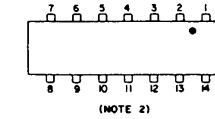
TYPE SN5474J  
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP



D	Q <sub>n</sub>	Q <sub>n+1</sub>
0	0	0
1	0	1
0	1	0
1	1	1

NOTE  
Q<sub>n</sub> = BIT TIME BEFORE CLOCK PULSE  
Q<sub>n+1</sub> = BIT TIME AFTER CLOCK PULSE

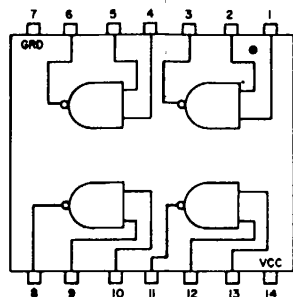
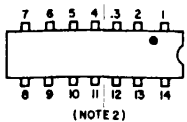
TYPE UGA96015IX OR MIC-9601-ID  
RETRIGGERABLE MONOSTABLE MULTIVIBRATOR



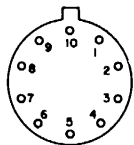
NOTE  
P<sub>w</sub> IS ESTABLISHED BY THE VALUES OF CAPACITOR C<sub>r</sub> AND RESISTOR R<sub>r</sub> WHICH ARE CONNECTED EXTERNALLY AS SHOWN

Figure 5-24. (4). Radio Set AN/GRC-144 integrated circuits, schematic diagrams (part 4 of 5)

**SN5403J - 00**  
QUAD 2-INPUT NAND-GATE

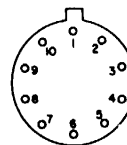


**MC1711G**  
DUAL DIFFERENTIAL COMPARATOR



(NOTE 1)

**MC1552G**  
LINEAR AMPLIFIER



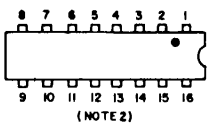
(NOTE 1)

**GT 733T**  
LINEAR DIFFERENTIAL AMPLIFIER



(NOTE 1)

**M38510/O1203CEB**  
DUAL MONOSTABLE MULTIVIBRATOR



(NOTE 2)

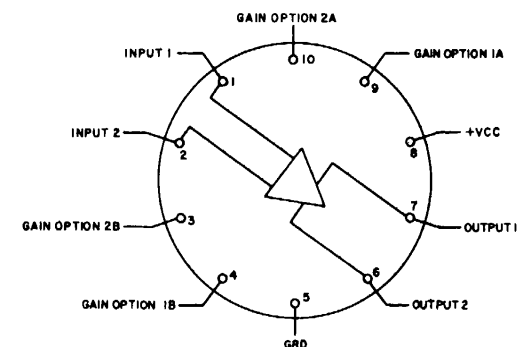
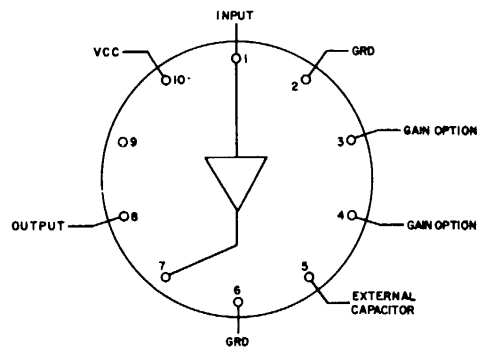
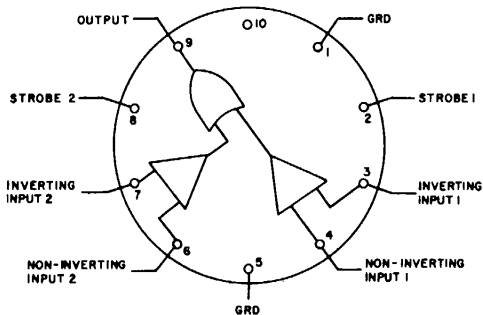
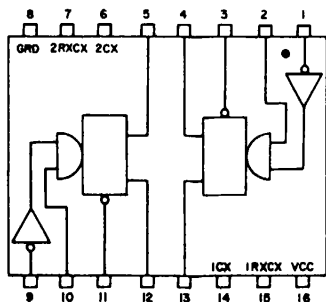


Figure 5-24. (5). Radio Set AN/GRC -144 integrated circuits, schematic diagrams (part 5 of 5)

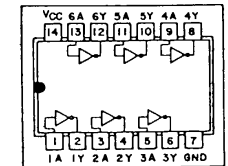
Change 1 5-62.1

Radio Set AN/GRC-144(V)3 and (V)4 integrated circuits

REF DES	DEVICE	PART NUMBER	FIG 5-24.1 (SHEET)	REF DES	DEVICE	PART NUMBER	FIG 5-24.1 (SHEET)	REF DES	DEVICE	PART NUMBER	FIG 5-24.1 (SHEET)
<b>Multiplexer, Digital OW 1A12A1</b>				<b>Digital Interface Buffer 1A12A4</b>				<b>Digital Traffic Retimer (Continued)</b>			
U4, U10	SN55107	M38510/10401BCB	2	U1	S08	M38510/08003BCB	1	U19	AM686	SM-B-956445	5
U6, U13	54LS00	M38510/30001BCB	1	U2, U9	54LS123	M38510/31401BEB	2	U20	54LS123	M38510/31401BEB	2
U9	34LS74	M38510/30102BCB	1	U3	S140	M38510/08101BCB	1	<b>Retimer, Digital, Orderwire 1A12A6</b>			
U11	54LS86	M38510/30502BCB	1	U4	55107AN	M38510/10401BCB	2	U2	LS86	M38510/30502BCB	1
U8, U12	54LS123	M38510/31401BEB	2	U5	LS00	M38510/30001BCB	1	U3	LS12	M38510/30006BCB	1
U2, U3	54LS161	M38510/31504BEB	3	U6	S04	M38510/07003BCB	1	U5, U6	LS74	M38510/30102BCB	1
U5	54LS175	M38510/30107BEB	2	U7	54LS158	M38510/30904BEB	2	U8	LS123	M38510/31401BEB	2
U7	54S04	M38510/07003BCB	1	U8	S02	M38510/07301BCB	1	U9	04	M38510/00105BCB	1
U1	MC12561	SM-B-956437-1	4	U10	55109AN	SM-B-956443	4	U7, U10	747	M38510/10102BCB	1
<b>Combiner, Alarm-Status 1A12A2</b>				U11	S74	M38510/07101BCB	1	U1	XR2207	SM-B-956513	5
U2, U10	54S00	M38510/07001BCB	1	U13	5426	M38510/00805BCB	1	U4	LM1081	M38510/10104BCB	2
U4	54S02	M38510/07301BCB	1	U14	LH0033G/883B	SM-B-956477	See Fig 5-38.6	<b>Demultiplexer, Digital Orderwire 1A12A7</b>			
U6, U11	54S04	M38510/07003BCB	1	U15	S07	M38510/00803BCB	1	U1, U2, U10	LS175	M38510/30107BEB	2
U3, U5, U8	54S10	M38510/07005BCB	1	U12	LS352	SM-B-956583	6	U3	LS191	M38510/31509BEB	3
U7, U12	ULN2003A	SM-B-956476	5	<b>Digital Traffic Retimer 1A12A5</b>				U4	LS04	M38510/30003BCB	1
U1	893-1-R10K	M8340102K1002GB	5	U1	DG182A	SM-B-956446	5	U5	LS86	M38510/30502BCB	1
U9	598-1-R2 7K	M8340102K2701GB	5	U2	5406	M38510/00801BCB	1	U6	LS00	M38510/30001BCB	1
<b>Digital Randomizer 1A12A3</b>				U3	AM686	SM-B-956445	5	U7	LS74	M38510/30102BCB	1
U1, U3, U7, U10	54LS164	M38510/30605BCB	6	U4	LM108L	M38510/10104BCB	2	U8, U9	SN55109A	SM-B-956443	4
U2, U4, U6, U8	54S74	M38510/07101BCB	6	U5	54S163	SM-B-956581	3	U11	LS123	M38510/31401BEB	2
U5, U9	54LS123	M38510/30401BEB	2	U6	54LS15	M38510/31002BCB	2	U12	LS10	M38510/30005BCB	1
U11, U15	54S86F	M38510/30605BCB	6	U7	54LS20	M38510/30007BCB	2	U13	S04	M38510/07003BCB	1
U12, U13	54S140	M38510/08101BCB	6	U8	1K Resistor Network	M8340102K1001GB	5	<b>Regenerator Digital 1A12A8</b>			
U14	54LS00	M38510/30001BCB	1	U9	LM211	SM-B-956444	4	U1, U4, U7	747	M38510/10102BCB	1
				U10	54LS04	M38510/30003BCB	1	U2	LM118D	M38510/10107BGA	2
				U11	54LS00	M38510/30001BCB	1	U3	LM2111	SM-B-956444	4
				U12	54LS74	M38510/07101BCB	1	U5	4213VM/MIL	SM-B-956496	4
				U13	54S86	M38510/07501BCB	1	U6	MDG001	JAN TX 2N5854	5
				U14	54S51	M38510/07401BCB	1	U8	0G	M38510/00801BCB	1
				U15	54LS74	M38510/07101BCB	1	U9	LH0032	SM-B-956502	5
				U16	54S03	M38510/07002BCB	1	U10	AM686	SM-B-956445	5
				U17	54S140	M38510/08101BCB	1	U11	LS02	M38510/30301BCB	1
				U18	MC12561	SM-B-956437	4	U12	LS123	M38510/31401BEB	2

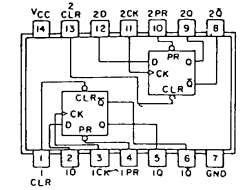
TYPE M38510/00105BCB, /00801BCB, /07003BCB, /30003BCB OR M38510/30004BCB

HEX INVERTER GATES



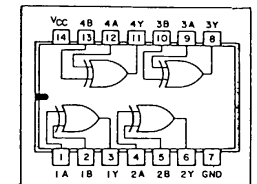
POSITIVE LOGIC  $Y = \bar{A}$

TYPE M38510/07101BCB OR/ 30102BCB DUAL D-TYPE FLIP-FLOP WITH PRESET AND CLEAR



D	
PRESET C	
L	
L	
H	
H	
H	

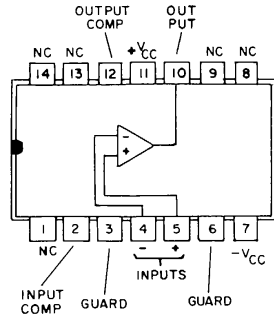
TYPE M 38510/07501BCB/ 30502BCB QUADRUPLE 2-INPUT EXCLUSIVE OR GATES



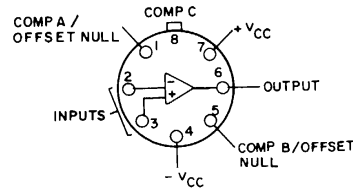
POSITIVE LOGIC  $Y = A \oplus B = \bar{A}B + A\bar{B}$

Figure 5-24.1 (1). Radio Set AN/GRC-144 (V) 3 and (V) 4 integrated circuits, (Sheet 1 of 6)

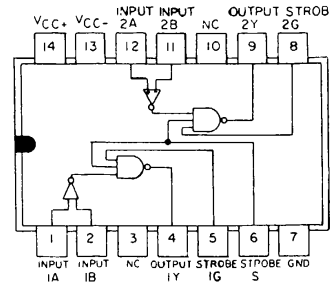
**M38510/10104BCB**  
OPERATIONAL AMPLIFIER, EXTERNALLY COMPENSATED



**M38510/10107BGA**  
OPERATIONAL AMPLIFIER, HIGH-SPEED



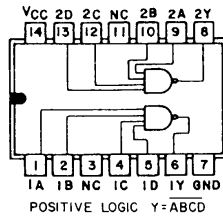
**M38510/10401BCB**  
DUAL LINE RECEIVER



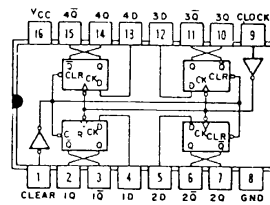
TRUTH TABLE

DIFFERENTIAL INPUTS A-B	STROBES		OUTPUT Y
	G	S	
$V_{ID} \geq 25 \text{ mV}$	L or H	L or H	H
$-25 \text{ mV} < V_{ID} < 25 \text{ mV}$	L or H	L	H
	L	L or H	H
$V_{ID} \leq -25 \text{ mV}$	H	H	INDETERMINATE
	L or H	L	H
	L	L or H	H
	H	H	L

**M38510/30007BCB**  
DUAL 4-INPUT POSITIVE NAND GATES



**M38510/30107BEB**  
QUADRUPLE D-TYPE FLIP-FLOPS  
WITH COMMON CLEAR AND COMMON CLOCK

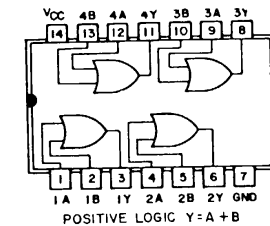


FUNCTION TABLE  
(EACH FLIP-FLOP)

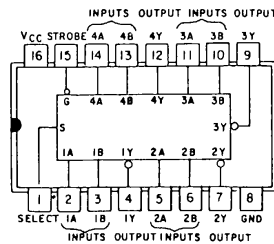
INPUTS		OUTPUTS	
CLEAR	CLOCK D	Q	$\bar{Q}$
L	X	X	L
H	X	H	H
H	↑	L	L
H	L	X	$Q_0$

(NOTE 2)

**M38510/30501BCB**  
QUADRUPLE 2-INPUT OR GATES



**M38510/30904BEB**  
QUADRUPLE 2-INPUT DATA SELECTOR/MULTIPLEXERS  
WITH ENABLE AND INVERTED DATA OUTPUTS

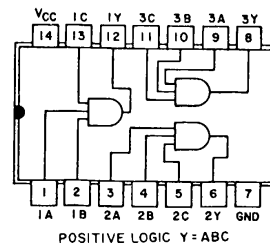


INPUTS		OUTPUT Y	
STROBE	SELECT	A B	TYPE 03 TYPE 04
H	X	X X	L H
L	L	L X	L H
L	L	H X	H L
L	H	X L	L H
L	H	X H	H L

H = high level, L = low level, X = irrelevant

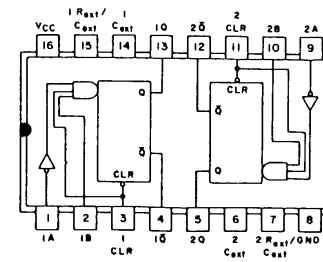
(NOTE 2)

**M38510/31002BCB**  
TRIPLE 3-INPUT POSITIVE AND GATES  
WITH OPEN COLLECTOR OUTPUTS



POSITIVE LOGIC Y = ABC

**M38510/31401BEB**  
DUAL MONOSTABLE MULTIVIBRATOR RETRIGGERABLE, WITH CLEAR

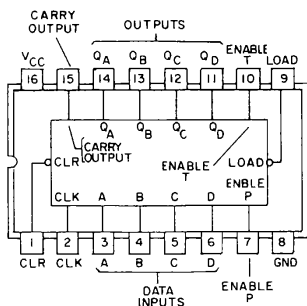


INPUTS		OUTPUTS	
CLEAR	A B	Q	$\bar{Q}$
L	X X	L	H
X	H X	L	H
X	X L	L	H
H	L ↑	↘	↗
H	↑ H	↘	↗
↑	L H	↘	↗

EL2IB094

Figure 5-24.1 (2). Radio Set AN/GRC -144 (V) 3 and (V) 4 integrated circuits, (Sheet 2 of 6)

**M38510/ 315048EB**  
 SYNCHRONOUS 4-BIT BINARY COUNTER WITH DIRECT CLEAR  
**SM-B-956581**  
**M38510/ 315128EB**  
 SYNCHRONOUS 4-BIT BINARY COUNTER WITH SYNCHRONOUS CLEAR  
 (DIRECT CLEAR)



Inputs at time $t_n$										Outputs at time $t_{n+1}$				
Clock	Enable P	Enable T	Load	A	B	C	D	Clear	$Q_A$	$Q_B$	$Q_C$	$Q_D$	Carry output	
X	X	X	X	X	X	X	X	L	L	L	L	L	L	

(SYNCHRONOUS CLEAR)

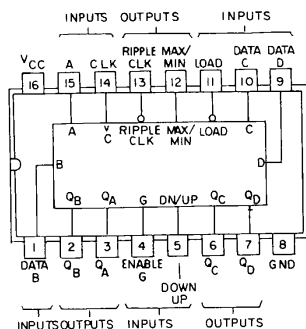
Inputs at time $t_n$										Outputs at time $t_{n+1}$				
Clock	Enable P	Enable T	Load	A	B	C	D	Clear	$Q_A$	$Q_B$	$Q_C$	$Q_D$	Carry output	
CP	L	X	H	X	X	X	X	H	NC	NC	NC	NC	NC	
CP	X	L	H	X	X	X	X	H	NC	NC	NC	NC	L	
CP	H	H	H	X	X	X	X	H	Previous count plus 1 (note 1)				H if count = 15 L if count < 15	
CP	X	H	L	X	X	X	X	H	A	B	C	D	H if count = 15 L if count < 15	
CP	X	L	L	X	X	X	X	H	A	B	C	D	L	
CP	X	X	X	X	X	X	X	L	L	L	L	L	L	

UP COUNT SEQUENCE TABLE

$Q_A$ (LSB)	$Q_B$	$Q_C$	$Q_D$ (MSB)
L	L	L	L
H	L	L	L
L	H	L	L
H	H	L	L
L	L	H	L
H	L	H	L
L	H	H	L
H	H	H	L
L	L	L	H
H	L	L	H
L	H	L	H
H	H	L	H
L	L	H	H
H	L	H	H
L	H	H	H
H	H	H	H

- NOTES  
 1 See up count sequence table  
 2  $L = V_{IL}$  for inputs,  $V_{OL}$  for outputs  
 3  $H = V_{IH}$  for inputs,  $V_{OH}$  for outputs  
 4  $X = V_{IH}$  or  $V_{IL}$   
 5 CP = Clock pulse  
 6 NC = No change

**M38510/ 315098EB**  
 SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTER



Mode select table

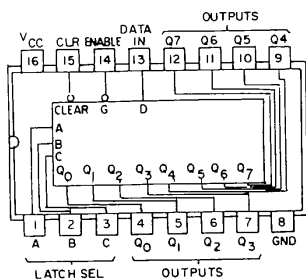
Inputs				Mode
Load	Enable G	U/D	CLK	
H	L	L	⌋	Count up
H	L	H	⌋	Count down
L	X	X	X	Preset (Asyn)
H	H	X	X	No change (Hold)

Ripple carry truth table

Inputs			RC output
Enable G	Max/Min	CLK	
L	H	⌋	⌋
H	X	X	H
X	L	X	H

- L = Low voltage level  
 H = High voltage level  
 X = Don't care  
 ⌋ = Low-to-high clock transition  
 ⌋ = Negative going clock pulse

**SM-B-956435**  
 EIGHT BIT ADDRESSABLE LATCH



LATCH SELECTION TABLE

SELECTED INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

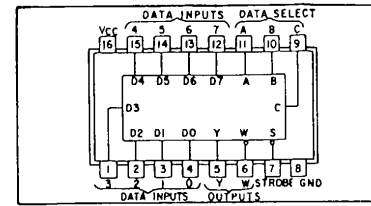
TRUTH TABLE

INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
CLEAR	$\bar{G}$			
H	L	D	$Q_{IO}$	ADDRESSABLE LATCH
H	H	$Q_{IO}$	$Q_{IO}$	MEMORY
L	L	D	L	8-LINE DEMULTIPLEXER
L	H	L	L	CLEAR

D = THE LEVEL AT THE DATA INPUT  
 $Q_{IO}$  = THE LEVEL OF  $Q_i$  (I=0,1, 7, AS APPROPRIATE) BEFORE THE INDICATED STEADY-STATE INPUT CONDITIONS WERE ESTABLISHED

Figure 5-24.1 (3). Radio Set AN/GRC-144 (V)3 and (V) 4 integrated circuits, (Sheet 3 of 6)

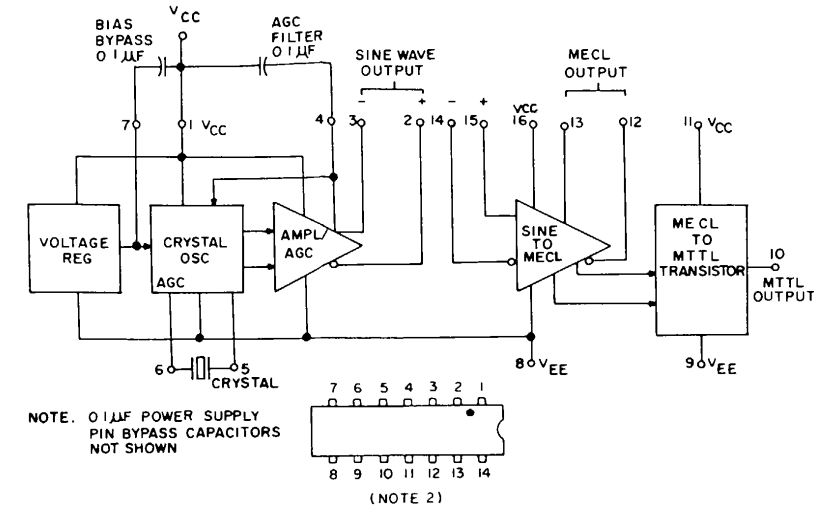
**TYPE SM-B-956436**  
EIGHT-INPUT DATA SELECTOR/MULTIPLEXER  
3-STATE OUTPUTS WITH ENABLE



SELECT		STROBE	DATA					OUTPUTS					
C	B		D0	D1	D2	D3	D4	D5	D6	D7	Y	W	Z
X	X	X	H	X	X	X	X	X	X	X	L	H	Z
L	L	L	L	X	X	X	X	X	X	X	L	H	L
L	L	L	L	H	X	X	X	X	X	X	H	L	L
L	L	L	L	X	L	X	X	X	X	X	L	H	L
L	L	L	L	X	H	X	X	X	X	X	H	L	L
L	L	L	L	X	X	L	X	X	X	X	L	H	L
L	L	L	L	X	X	H	X	X	X	X	H	L	L
L	L	L	L	X	X	X	L	X	X	X	L	H	L
L	L	L	L	X	X	X	H	X	X	X	H	L	L
L	L	L	L	X	X	X	X	L	X	X	L	H	L
L	L	L	L	X	X	X	X	H	X	X	H	L	L
L	L	L	L	X	X	X	X	X	L	X	L	H	L
L	L	L	L	X	X	X	X	X	H	X	H	L	L
L	L	L	L	X	X	X	X	X	X	H	L	H	L
L	L	L	L	X	X	X	X	X	X	H	L	H	L

H = high logic level, L = low logic level, Z = high impedance, X = irrelevant

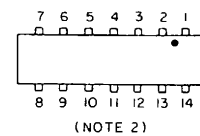
**TYPE SM-B-956437**  
PHASE-LOCKED LOOP COMPONENTS,  
CRYSTAL OSCILLATOR



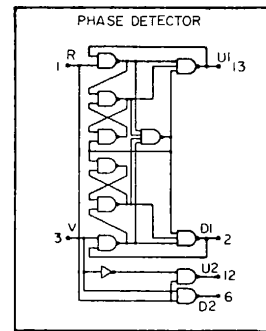
NOTE: 0.1µF POWER SUPPLY PIN BYPASS CAPACITORS NOT SHOWN

(NOTE 2)

**TYPE SM-B-956438**  
DIGITAL PHASE-FREQUENCY DETECTOR



(NOTE 2)

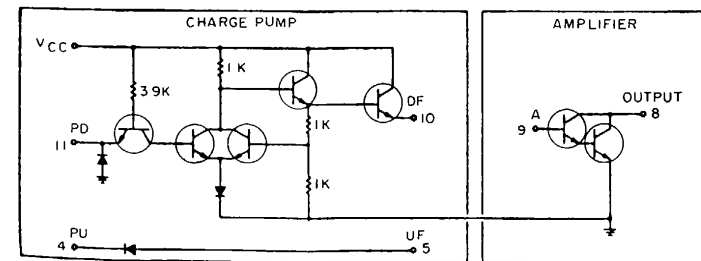
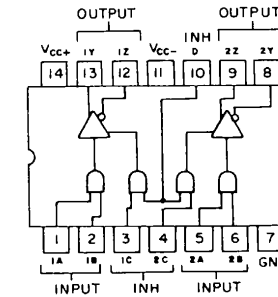


**TYPE SM-B-956443**  
DIGITAL DUAL LINE DRIVER

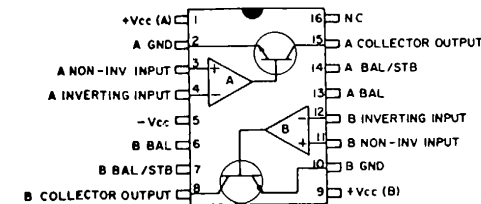
TRUTH TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
L or H	L or H	L	L or H	H	H
L or H	L or H	L or H	L	H	H
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

LOW OUTPUT REPRESENTS THE ON STATE  
HIGH OUTPUT REPRESENTS THE OFF STATE

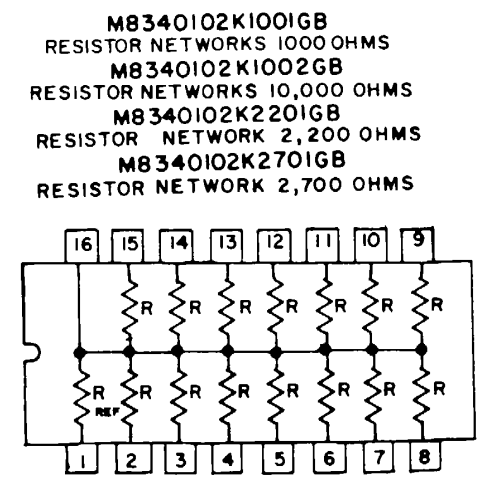
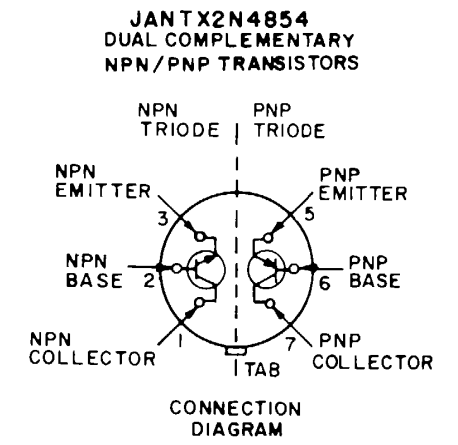
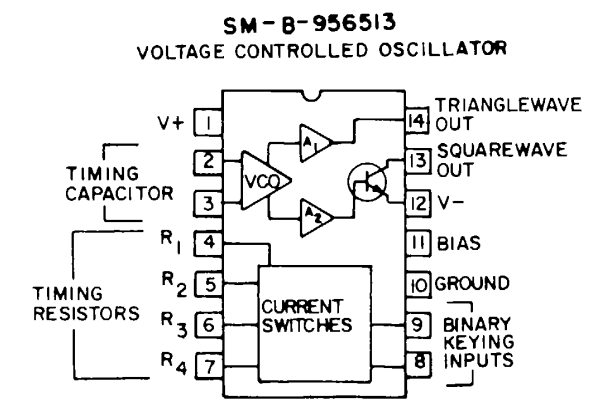
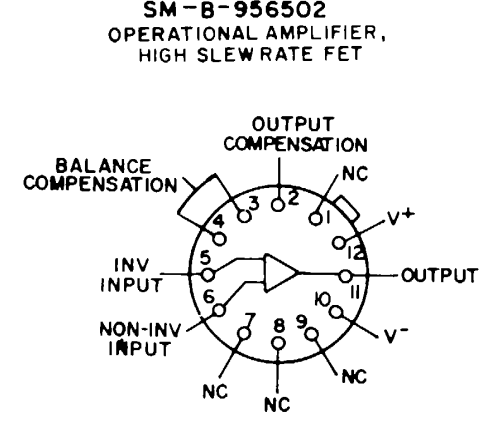
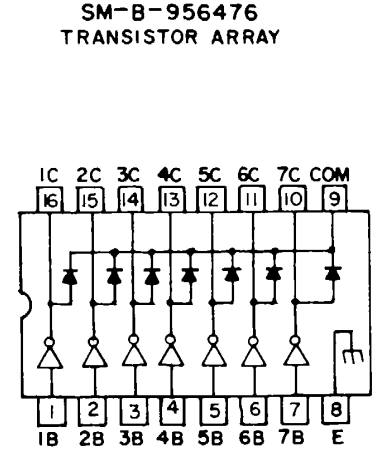
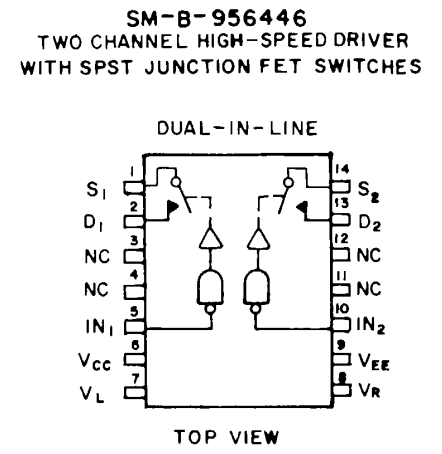
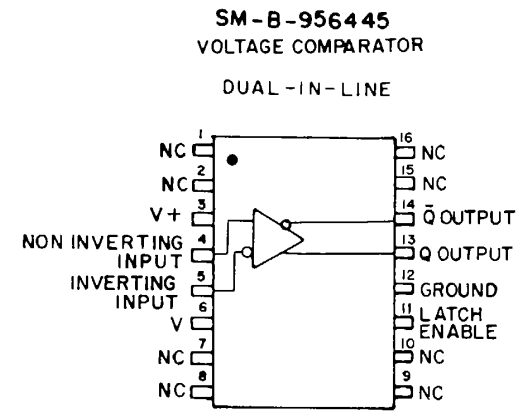


**TYPE SM-B-956444**  
DUAL PRECISION VOLTAGE COMPARATORS



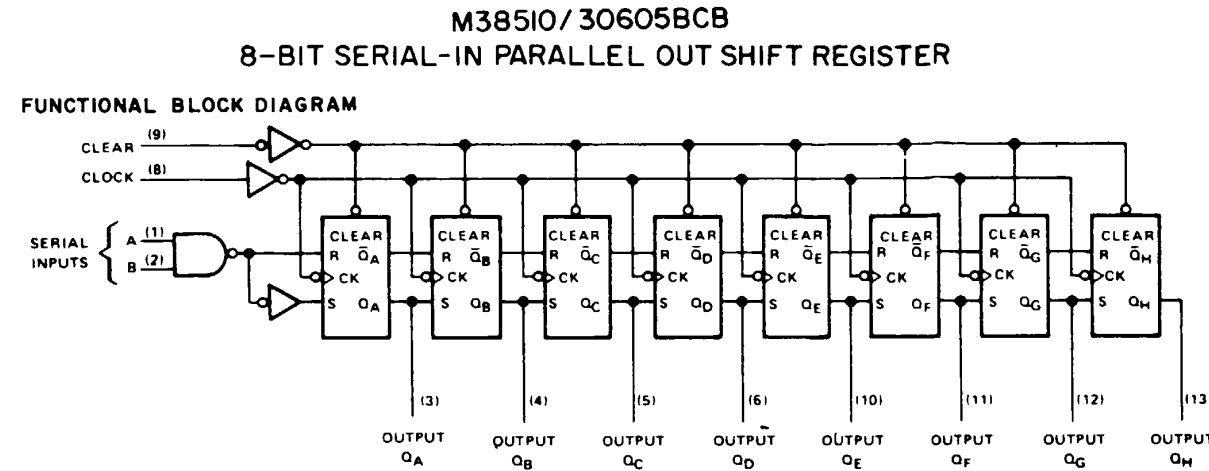
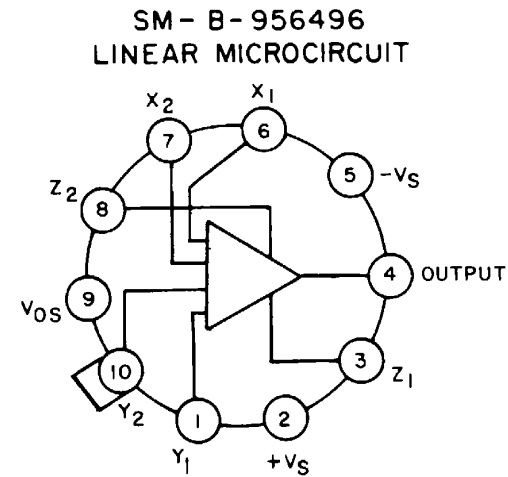
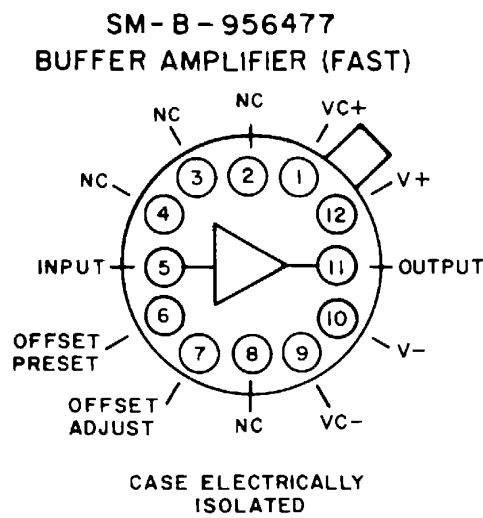
EL2IB096

Figure 5-24.1(4). Radio Set AN/GRC-144(V)3 and (V)4 integrated circuits (sheet 4 of 6)  
Change 6 5-62.9

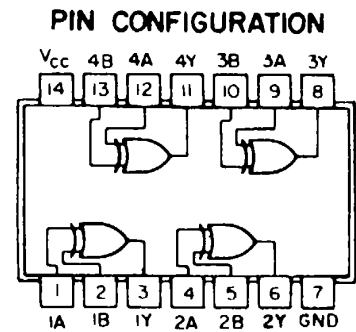


EL2IB097

Figure 5-24.1(5) Radio Set AN/GRC-144(V)3 and (V)4 intergrated circuits (sheet 5 of 6).  
Change 6 5-62.11



**M38510/30605BCB**  
QUAD 2-INPUT EXCLUSIVE OR GATE

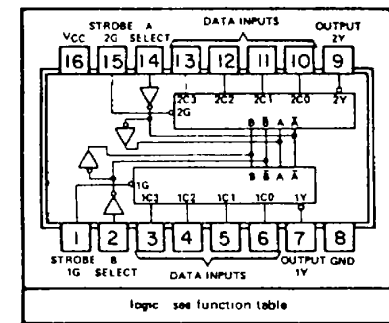


TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

L = LOW voltage level  
H = HIGH voltage level

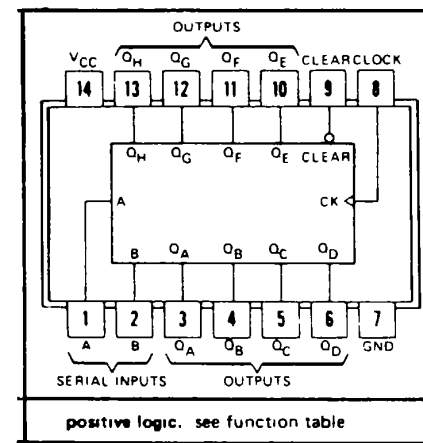
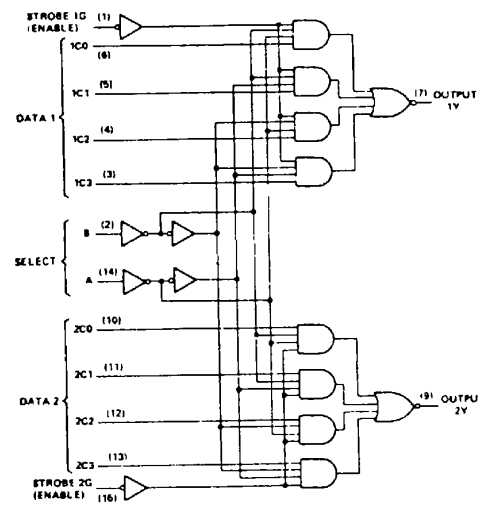
**SM-B-956435**  
DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections  
H = high level L = low level X = irrelevant

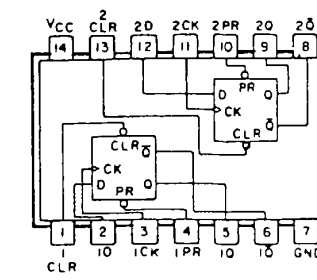


**M38510/07101BCB**  
DUAL 0-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

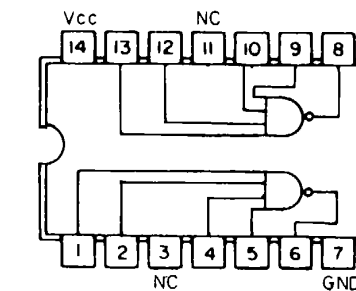
FUNCTION TABLE

INPUTS			OUTPUTS	
PRESET	CLEAR	CLOCK	Q	Q̄
L	H	X	X	H L
H	L	X	X	L H
L	L	X	X	H* H*
H	H	↑	L	H L
H	H	↑	H	L H
H	H	L	X	Q0 Q̄0

\* THIS CONFIGURATION IS NONSTABLE, THAT IS, IT WILL NOT PERSIST WHEN PRESET AND CLEAR INPUTS RETURN TO THEIR INACTIVE (HIGH) LEVEL.



**M38510/08101BCB**  
DUAL 4-INPUT NAND LINE DRIVER



Positive logic Y = ABCD  
NC - No internal connection

EL21B147

Figure 5-24.1(6) Radio Set AN/GRC-144(V)3 and (V)4 integrated circuits (sheet 6 of 6).  
Change 6 5-62-13



- NOTES
- UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS CAPACITANCES ARE IN MICROFARADS INDUCTANCES ARE IN MICROHENRIES.
  - PARTIAL REFERENCE DESIGNATIONS ARE SHOWN PREFIX REFERENCE DESIGNATIONS WITH 1A7.
  - TERMINALS 1 THROUGH 11, 16, 17 AND 24 THROUGH 39 ARE MOUNTED ON THE PRINTED WIRING BOARD TERMINALS 12 THROUGH 15 AND 18 THROUGH 23 ARE PADS ON THE PRINTED WIRING BOARD.
  - INDICATES MARKING ON EQUIPMENT.
  - CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING.

REFERENCE DESIGNATION	SPECIFICATION DRAWING
Q1, Q3, Q7, Q11	SM-B-653437-1
Q6, Q14, Q15	SM-B-653417
Q8, Q9, Q10	SM-B-653437-2
Q2, Q12, Q13	SM-B-653389

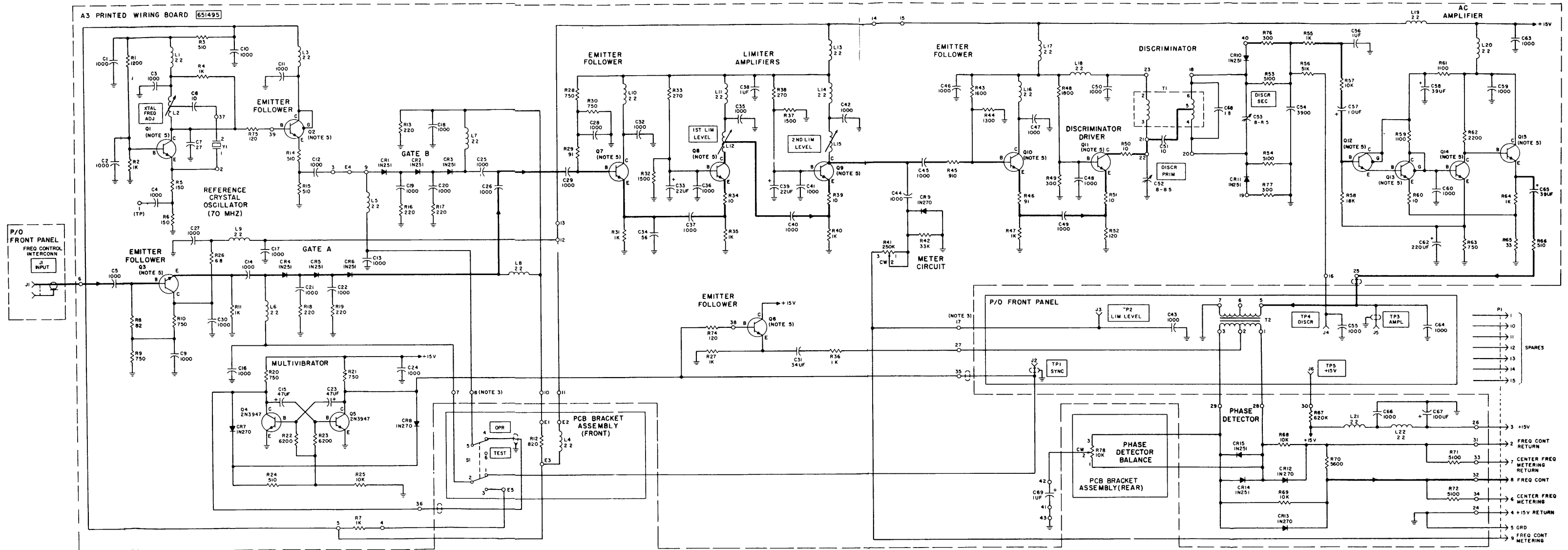


Figure 5-25. Electronic frequency control 1A7, schematic diagram.  
Change 1 5-63

- NOTES  
 1 UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS CAPACITANCES ARE IN PICOFARADS INDUCTANCES ARE IN MICROHENRIES.  
 2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX REFERENCE DESIGNATIONS WITH 1A8  
 3 INDICATES MARKING ON EQUIPMENT  
 4 THE TYPE DESIGNATOR FOR A1 IS USB770231X; FOR A2, 80286  
 5 LEGEND  
  
  
 6 CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING

DESCRIPTION	REFERENCE DESIGNATION	SPECIFICATION DRAWING
TRANSISTOR	Q1, Q2, Q3, Q5, Q6, Q7	SM-B-653389
TRANSISTOR	Q8, Q9	SM-B-651335-2
TRANSISTOR	Q4, Q8	SM-B-650721
DIODE	CR1, CR2	SM-B-653076
SUPPRESSOR	L17	SM-B-651350
OPERATIONAL AMPLIFIER	A1	SM-B-650746
LINEAR AMPLIFIER	A2	SM-B-653078
COIL, RF	L19	SM-B-651363

7 IN SOME COMPONENTS RESISTOR R78 IS ADDED AND SWITCH S1 IS SPOT AS SHOW IN PARTIAL SCHEMATIC BELOW.

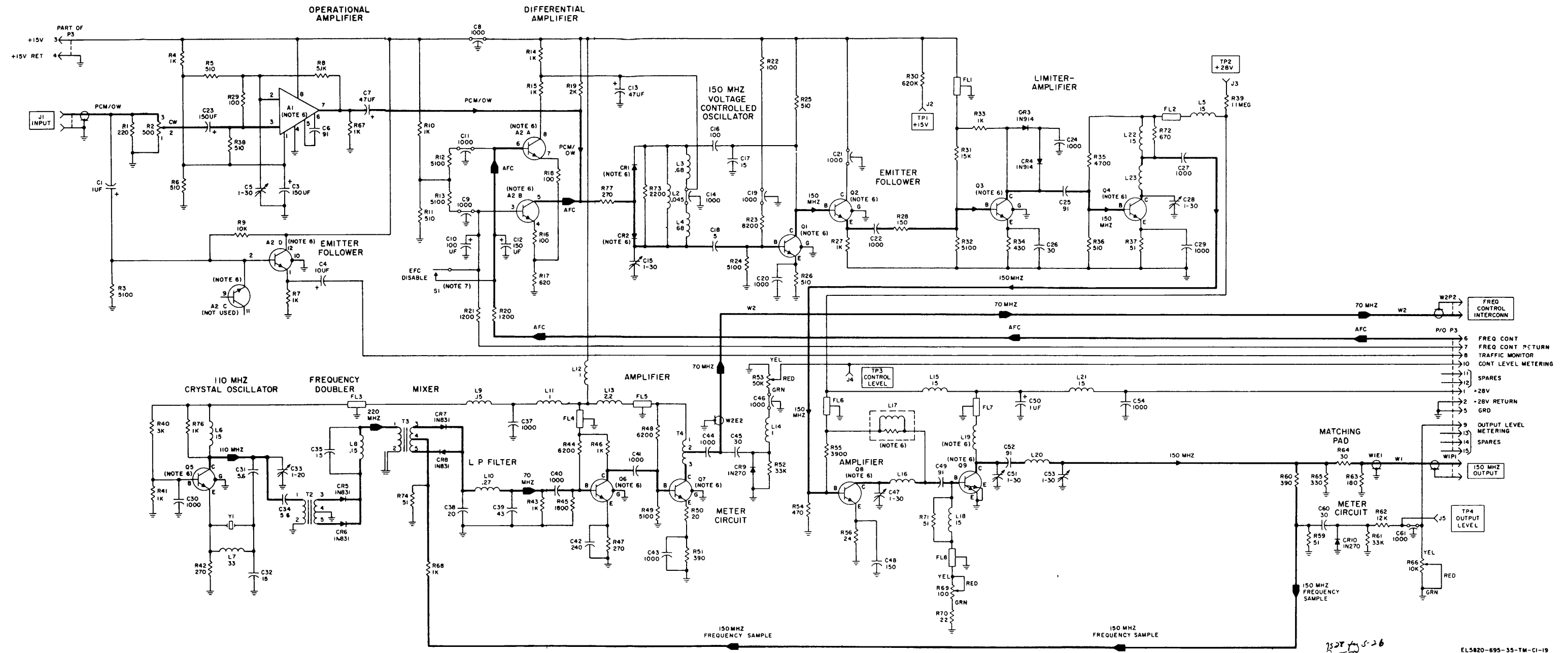
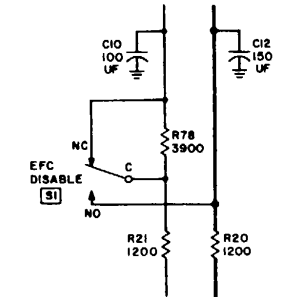


Figure 5-26. Radio transmitter, modulator 1A8, schematic diagram.  
 Change 1 5-65

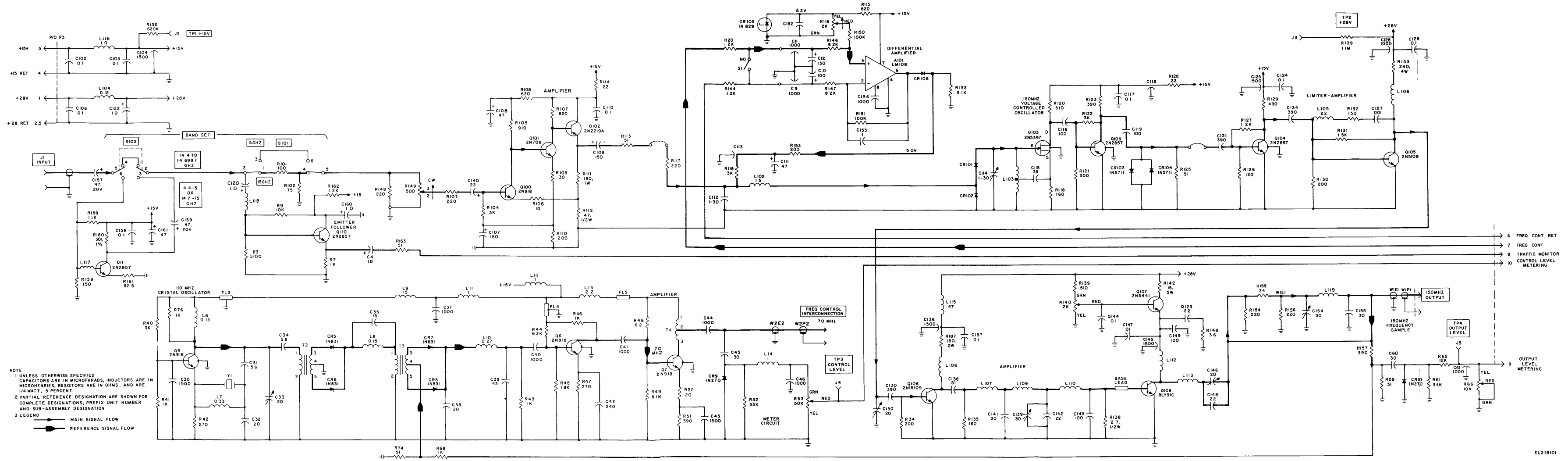


Figure 5-26.1. Modulator, radio transmitter 1A8 (956427), schematic diagram.  
 Change 6 5-65.1

EL218101

NOTES  
1 UNLESS OTHERWISE SPECIFIED, ALL RESISTOR VALUES ARE IN OHMS, ALL CAPACITOR VALUES ARE IN PICOFARADS  
2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH IAH  
3 J4 IS THE INITIAL ALIGNMENT TEST POINT.

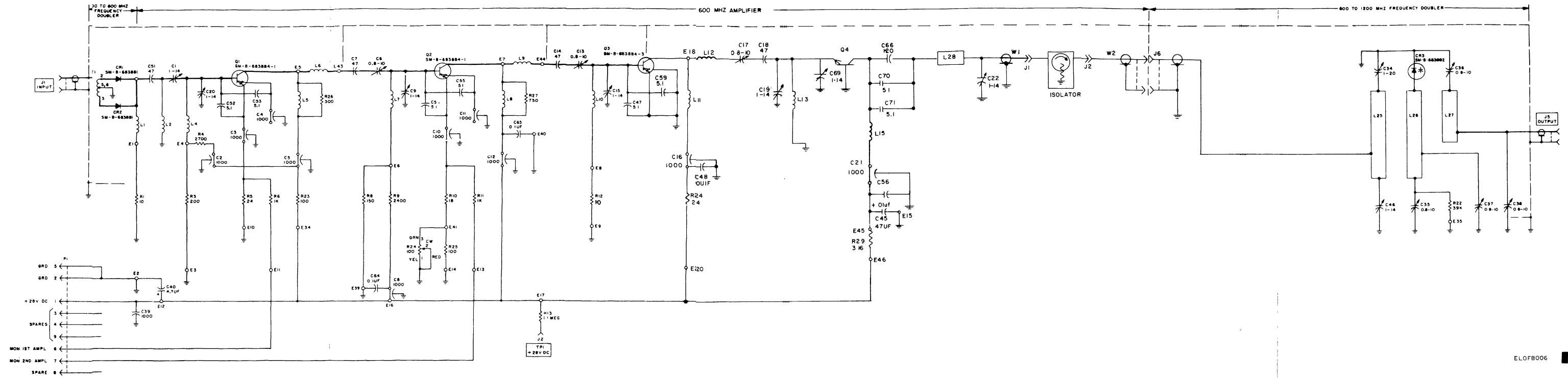


Figure 5-27. Transmitter amplifier-frequency multiplier 1A11, schematic diagram.  
Change 5 5-67

ELOFB006

- NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION.
  2. PLUS-IN MODULES AT THRU ARE PREFIXED WITH DESIGNATION 1A12 ONLY.
  3. CONTACTS ON AT THRU ARE ETCHED CONTACTS ON PRINTED WIRING BOARD.
  4. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES IN MICROFARADS.
  5. IN CIRCUIT NUMERICS: P = LETTER "P" O = NUMBER ZERO
  6. UNLESS OTHERWISE SPECIFIED ALL WIRES ARE STRANDED, TEFLOM INSULATED, SIZE AS FOLLOWS: NO. 10-40 - FOR VOLTAGE, GROUND AND TWISTED PAIR (PI) SIGNAL LEADS. NO. 22 AWG - FOR ALL OTHER WIRES INCLUDING SHIELDED TWISTED PAIRS.
  7. AT XAS ALL SHIELD GROUND LEADS ARE RUN AS SEPARATE WIRES.
  8. THE FOLLOWING PARTS ARE NOT PHYSICALLY SHOWN IN THIS DIAGRAM: 1A1210W - WIRING HARNESS, BRANCHED 1A1210W - WIRING HARNESS, BRANCHED 1A1210W - WIRING HARNESS, BRANCHED.

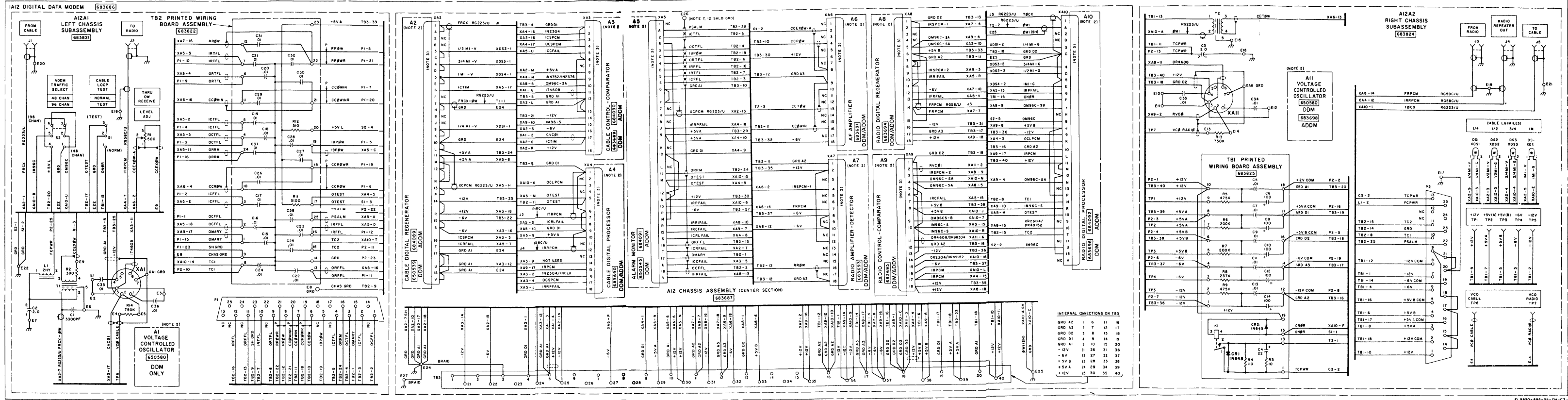
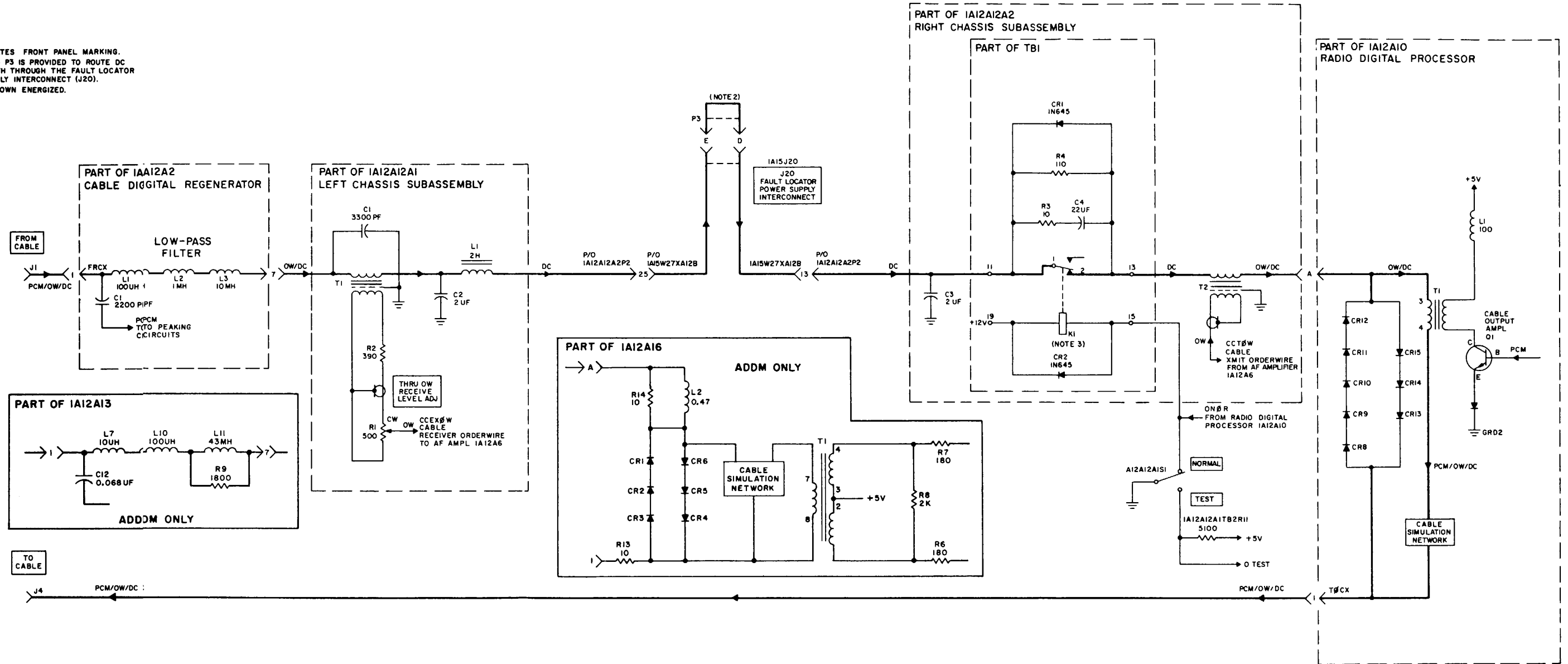


Figure 5-28. Digital data modem 1A12, interconnecting diagram.  
Change 1 5-69

- NOTES:  
 1.   INDICATES FRONT PANEL MARKING.  
 2. JUMPER PLUG P3 IS PROVIDED TO ROUTE DC CURRENT PATH THROUGH THE FAULT LOCATOR POWER SUPPLY INTERCONNECT (J20).  
 3. RELAY K1 SHOWN ENERGIZED.



EL5820-695-35-C2-TM-4

Figure 5-29. Dc path through digital data modem 1A12, SIMPLIFIED SCHEMATIC.

Change 2 5-71

- NOTES  
 1. UNLESS OTHERWISE SPECIFIED:  
 RESISTANCES ARE IN OHMS  
 CAPACITANCES ARE IN MICROFARADS  
 INDUCTANCES ARE IN MICROHENRIES  
 2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.  
 PREFIX REFERENCE DESIGNATIONS WITH 1A12A2.  
 3. ALL TERMINALS PREFIXED WITH E ARE TEST POINTS.  
 4. REFER TO TABLE FOR STRAPPING CONFIGURATIONS.  
 5. INTEGRATED CIRCUIT A1 IS A SPECIALLY  
 SELECTED USB71031X PER ITTDCO DROWING SM-B-685816.

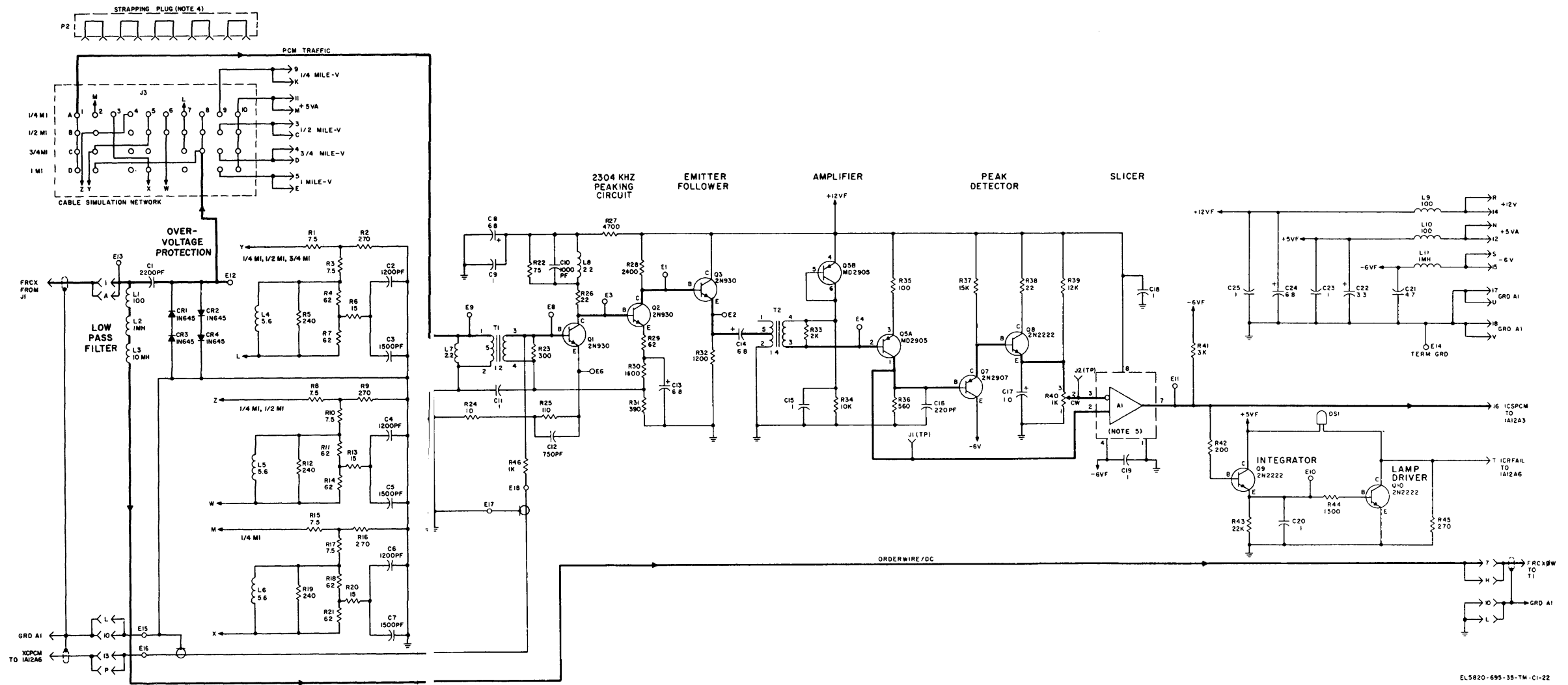


Figure 5-30. Cable digital regenerator 1A12A2, schematic diagram, synchronous mode.

Change 1 5-73

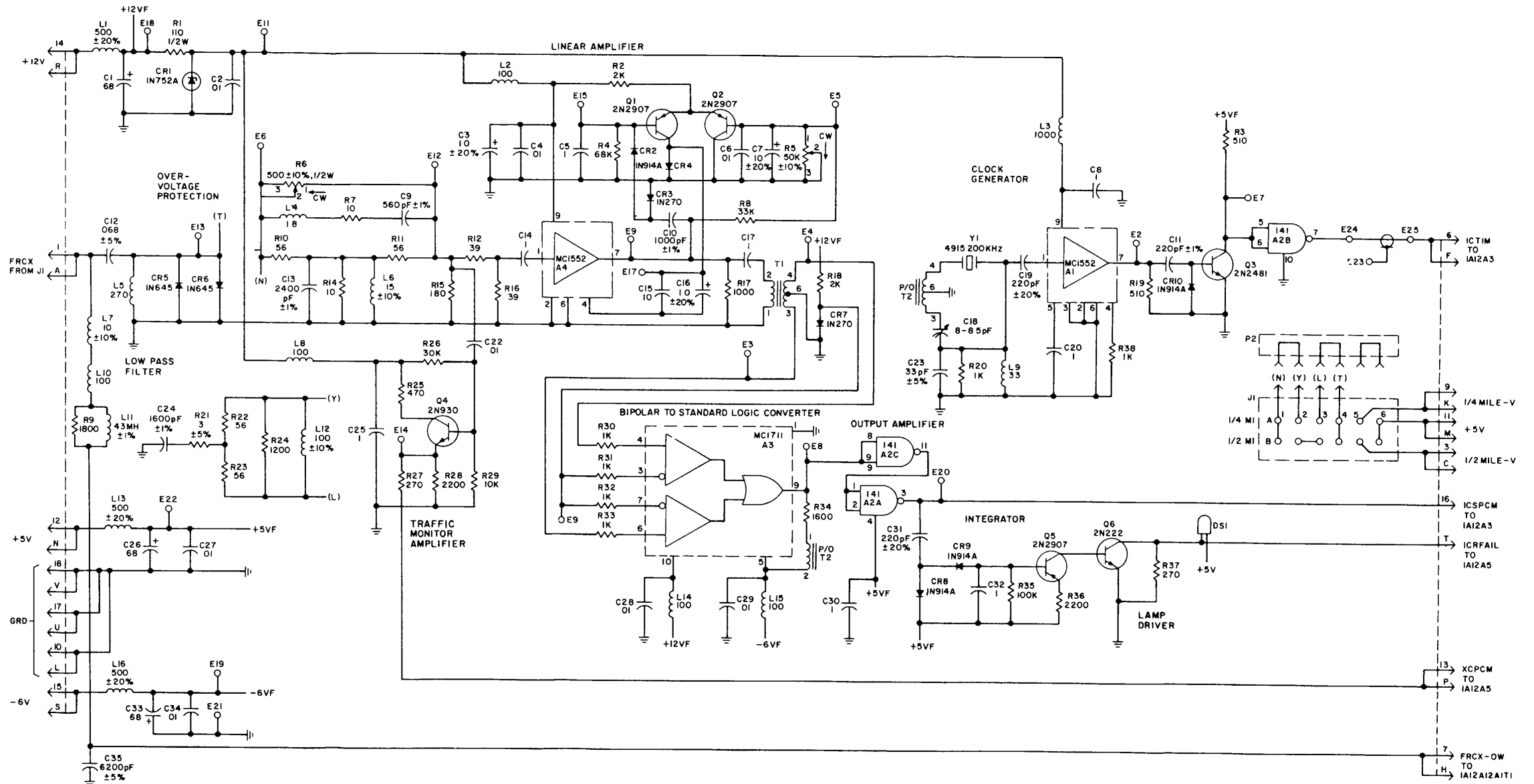
- NOTES:  
 1. UNLESS OTHERWISE SPECIFIED:  
 ALL RESISTORS ARE IN OHMS, 1/4 W ± 2%  
 ALL CAPACITORS ARE IN MICROFARADS, ± 10%  
 ALL INDUCTORS ARE IN MICROHENRIES, ± 5%

2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH IA12A13  
 3. POSITION OF ADAPTER FURNISHED WITH EQUIPMENT DETERMINES LENGTH OF CABLE EQUIPMENT WILL OPERATE WITH PER TABLE 1

CABLE LENGTH	CONNECTIONS MADE WHEN P2 IS INSERTED INTO J1
1/4 MILE	A1 TO A2, A3 TO A4, A5 TO A6
1/2 MILE	B1 TO B2, B3 TO B4, B5 TO B6

4. IN THE LOGIC SYMBOL, THE NUMBERS ABOVE THE REFERENCE DESIGNATOR IS PART OF THE TYPE DESIGNATOR  
 5. LETTERS WITHIN PARENTHESIS INDICATE INTERNAL CONNECTIONS ON BOARD  
 6. ALL TERMINALS PREFIXED WITH E (E1, E2, ETC) ARE TEST POINTS  
 7. POWER CONNECTIONS FOR INTEGRATED CIRCUITS ARE SHOWN IN TABLE 2

PWR CONNECTIONS			
POS	+5V	GRD	TYPE
A1	AS SHOWN		MC1552G
A2	4	10	SG 141-03
A3	AS SHOWN		MC1711G
A4	AS SHOWN		MC1552G



EL5820-695-35-TM-5

Figure 5-30.1. Cable digital regenerator 1A12A13 schematic diagram, asynchronous mode.

Change 2 5-74.1



- 1 RESISTANCES ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
- 2 CAPACITANCES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
- 3 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX REFERENCE DESIGNATION WITH 1A12A3 IS USED.
- 4 ALL TERMINALS PREFIXED WITH E (E1, E2, ETC.) ARE TEST POINTS.
- 5 POWER CONNECTIONS FOR INTEGRATED DIGITAL CIRCUITS ARE SHOWN IN THE TABLE.

POS	GRD			TYPE
	A	B	C	
A1	AS SHOWN			UGA9601S1X, MIC-9601-D
A2	4	10		SG141-03, RG 141D
A3	4	10		SG141-03, RG 141D
A4	4	10		SG130-03, RG 130D
A5	AS SHOWN			UGA9601S1X, MIC-9601-D
A6	4	10		SG130-03, RG 130D
A7		10		SF101-03, RF101D
A8	AS SHOWN			MC1531G
A9	AS SHOWN			RM711-D
A10	4	10		SG221-03
A11	4	10		SG141-03, RG141D

5 IN THE LOGIC SYMBOLS, THE NUMBER ABOVE THE REFERENCE DESIGNATOR IS PART OF THE TYPE DESIGNATOR.

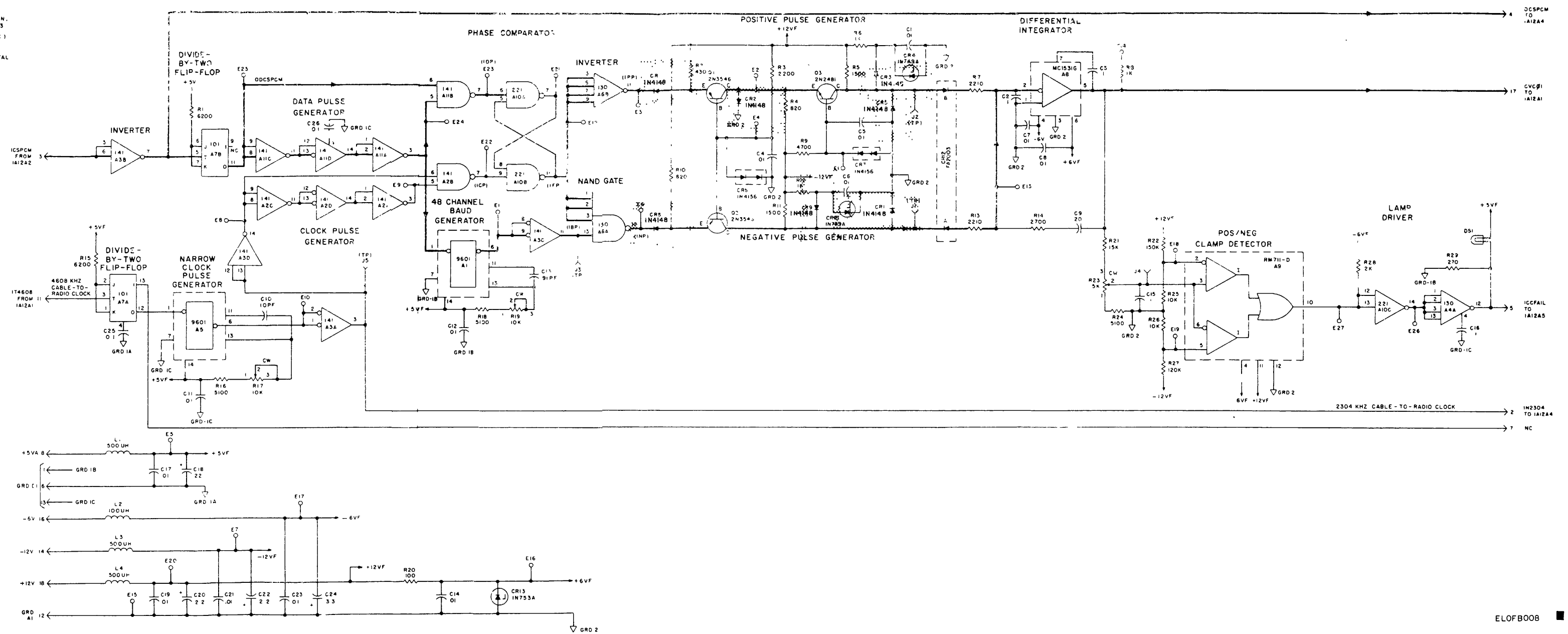
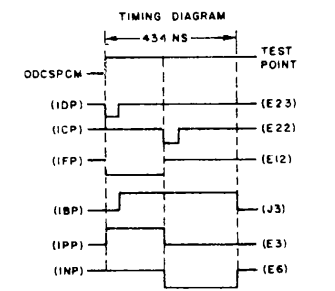
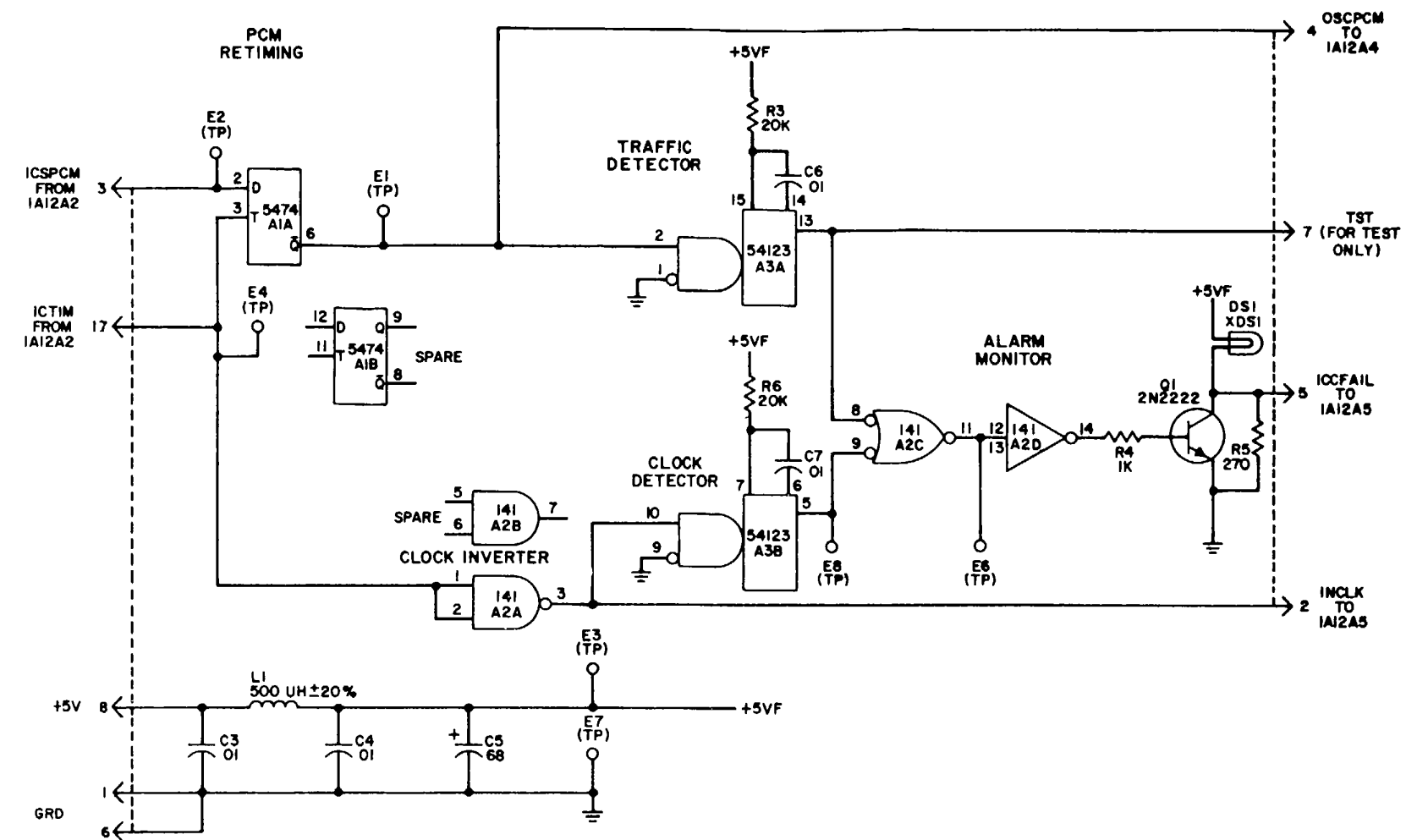


Figure 5-31. Cable control-comparator 1A12A3, schematic diagram, synchronous mode.

Change 5 5-75



NOTES

- 1 UNLESS OTHERWISE SPECIFIED RESISTORS ARE IN OHMS, 1/4 W, ±2%. CAPACITORS ARE IN MICRO-FARADS ±10%.
- 2 PARTIAL REF DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A12A14.
- 3 ALL TERMINALS PREFIXED WITH E (E1, E2, ETC) ARE TEST POINTS.
- 4 IN THE LOGIC SYMBOL, THE NUMBER ABOVE THE REFERENCE DESIGNATOR IS PART OF THE TYPE DESIGNATOR.
- 5 POWER CONNECTIONS FOR INTEGRATED CIRCUITS ARE SHOWN IN TABLE I.

TABLE I

POS	PWR CONNECTIONS		TYPE
	+5V	GRD	
A1	14	7	SN 5474J
A2	4	10	SG 141-03
A3	16	8	M38510/01203 CEB

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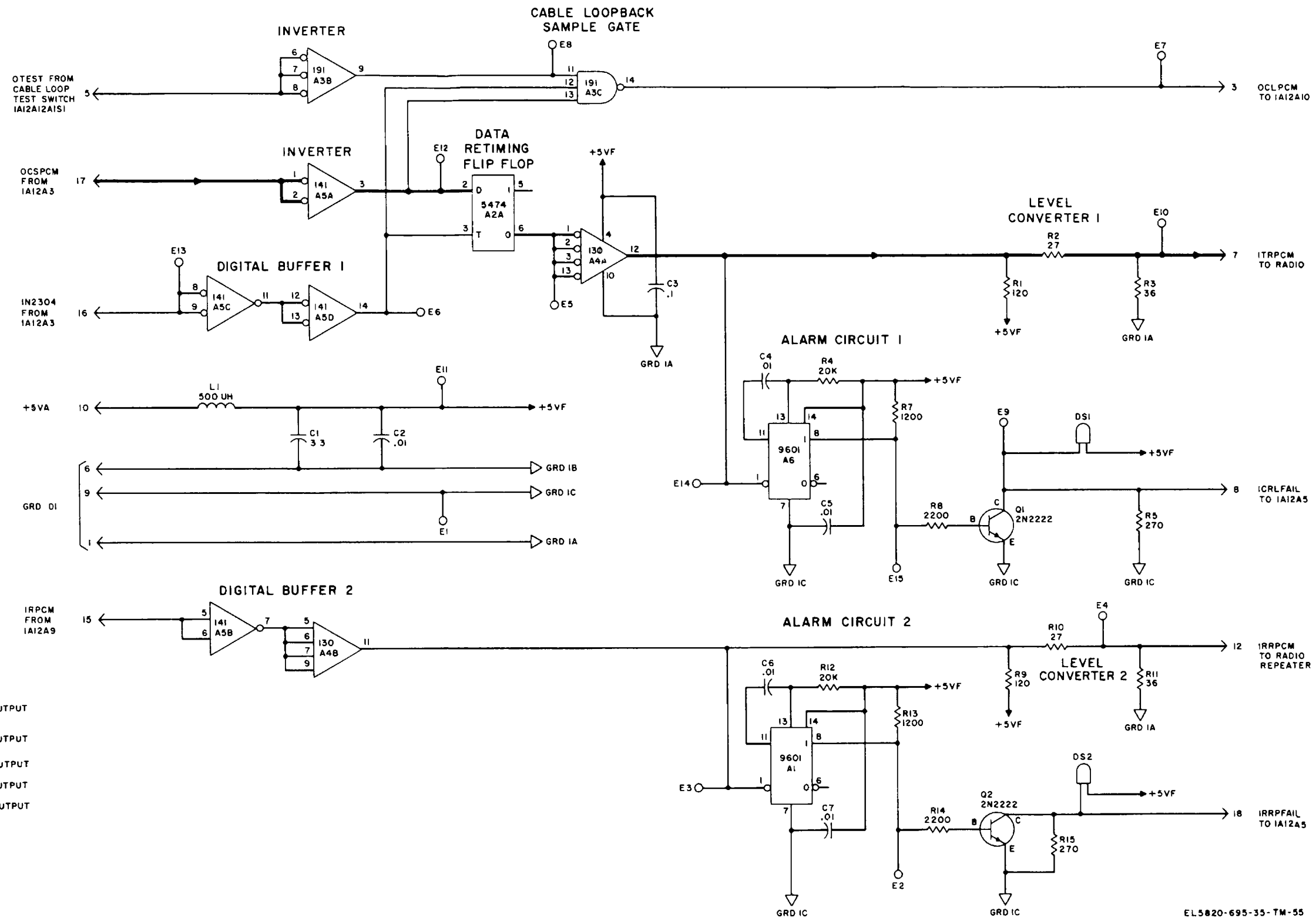
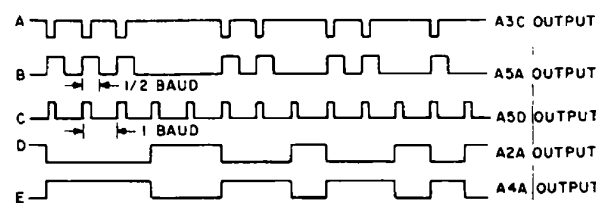
Figure 5-31.1. Cable control comparator 1A12A14, schematic diagram, asynchronous mode.

NOTES

- 1 UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS CAPACITANCES ARE IN MICROFARADS
- 2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN PREFIX REFERENCE DESIGNATIONS WITH 1A12A4
- 3 ALL TERMINALS PREFIXED WITH E (E1, E2, ETC) ARE TEST POINTS
- 4 POWER CONNECTIONS FOR INTEGRATED CIRCUITS ARE SHOWN IN THE TABLE

POWER CONNECTIONS				TYPE	
POS	+5VF	GRD I			
		A	B	C	
A1	AS SHOWN				U8A960151X MIC-9601-1D
A2	14			7	SN5474
A3	4	10			SG191-03
A4	4	10			SG130-03
A5	4			10	SG141-03
A6	AS SHOWN				U8A960151X MIC-9601-1D

- 5 IN THE LOGIC SYMBOL, THE NUMBER ABOVE THE REFERENCE DESIGNATOR IS PART OF TYPE DESIGNATOR



EL5820-695-35-TM-55

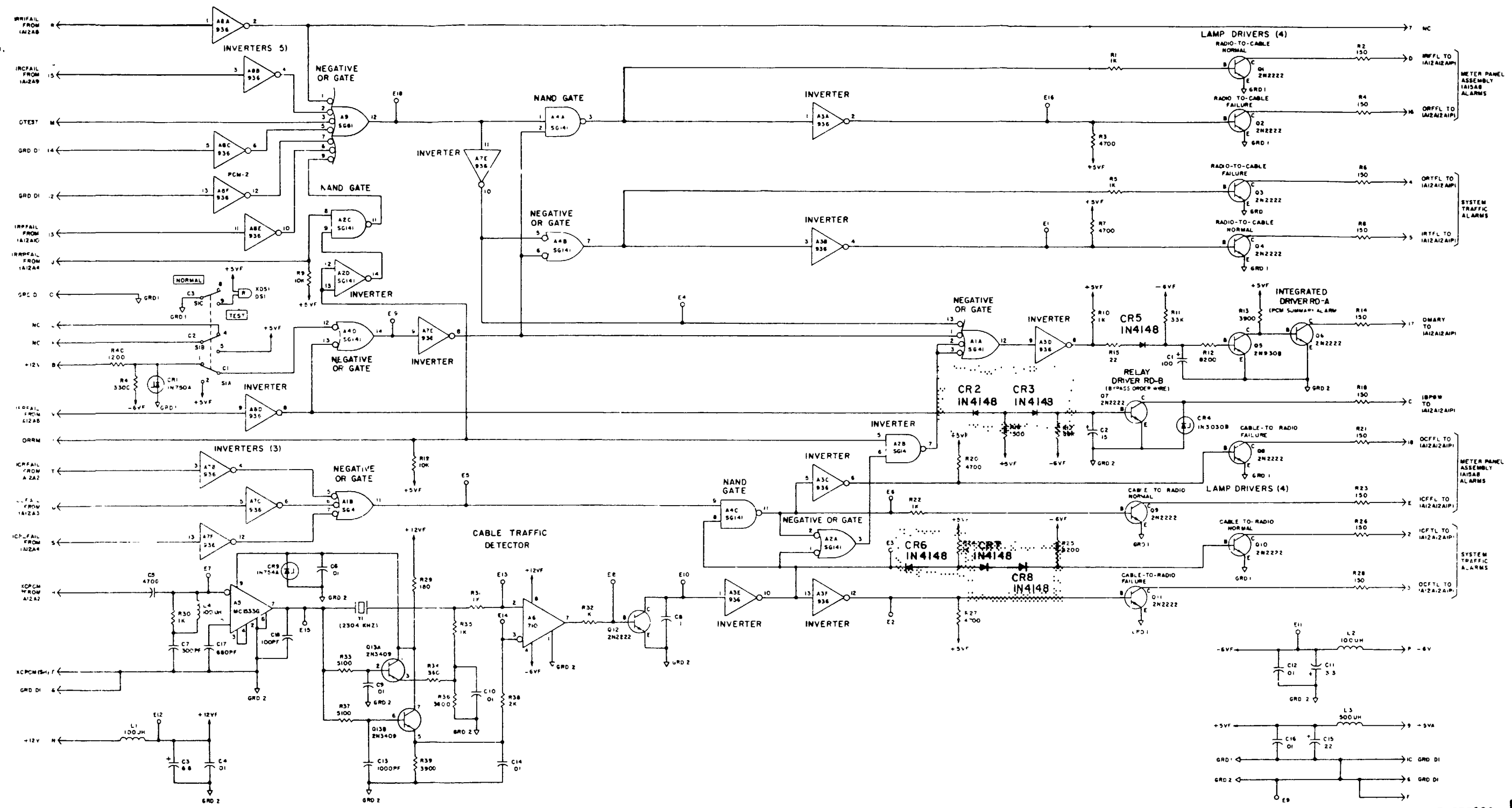
Figure 5-32. Cable digital processor 1A12A4, schematic diagram.

NOTES

- 1 UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS CAPACITANCES ARE IN MICROFARADS
- 2 PARTIAL REFERENCE DENOTATIONS ARE SHOWN. PREFIX REFERENCE DENOTATIONS WITH 1A12A5 ARE TEST POINTS
- 3 ALL TERMINALS PREFIXED WITH E (E1, E2, ETC.) ARE TEST POINTS
- 4 IN THE LOGIC SYMBOL, THE NUMBER BELOW THE REFERENCE DESIGNATOR IS PART OF THE TYPE DESIGNATOR

POWER CONNECTIONS			TYPE
POS	+5VF	GRD 1	
A1	4	10	5641-03
A2	4	10	5641-03
A3	14	7	RM936D
A4	4	10	5641-03
A7	14	7	RM936D
A8	14	7	RM936D
A9	4	10	5641-03
A5	A5 SHOWN		MC5336
A6	A5 SHOWN		US87703X

5 POWER CONNECTIONS FOR EACH INTEGRATED CIRCUIT ARE SHOWN IN THE TABLE ABOVE



EL OF 8009

Figure 5-33. Alarm monitor 1A12A5, schematic diagram, synchronous mode.

- NOTES
- UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS 1/4W±2% CAPACITANCES ARE IN MICROFARADS±20%
  - PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 1A12A15
  - ALL TERMINALS PREFIXED WITH E (E1, E2, ETC) ARE TEST POINTS
  - POWER CONNECTIONS FOR EACH INTEGRATED CIRCUIT ARE SHOWN IN THE TABLE

TABLE

PWR CONNECTIONS			
POS	+5VF	GRD	TYPE
A1	AS SHOWN	SG 733T	
A2	AS SHOWN	US877103IX	
A3	4	10	SG 141-03
A4	4	10	SG 61-03
A5	14	7	RM 936 D
A6	14	7	RM 936 D
A7	4	10	SG 141-03
A8	4	10	SG 41-03
A9	14	7	RM 936 D

- IN THE LOGIC SYMBOL, THE NUMBER BELOW THE REFERENCE DESIGNATOR IS PART OF THE TYPE DESIGNATOR.

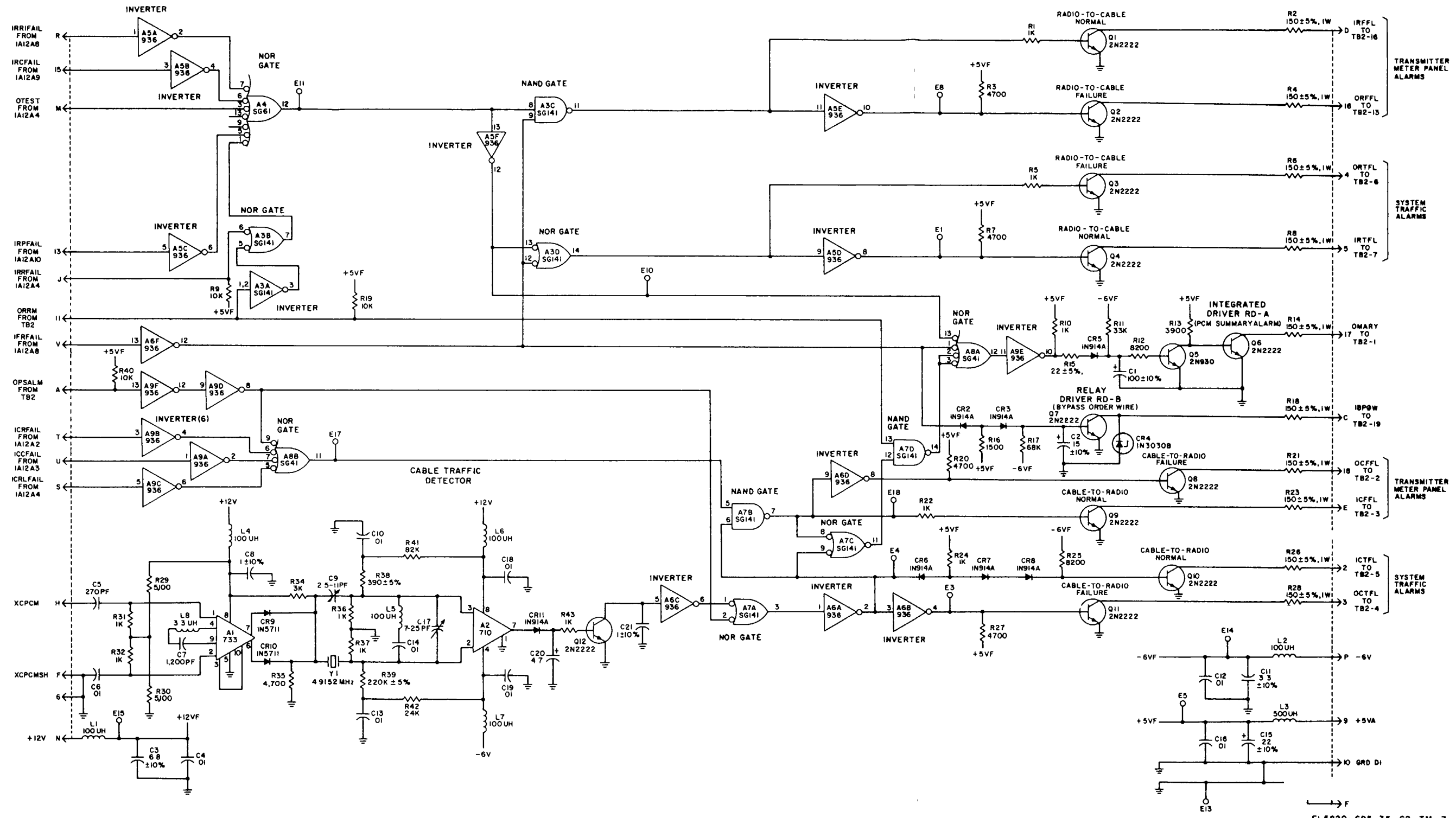


Figure 5-33.1. Alarm monitor 1A12A15, schematic diagram, asynchronous mode.

NOTES

- 1 UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS CAPACITANCES ARE IN MICROFARADS
- 2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN PREFIX REFERENCE DESIGNATIONS WITH IA12A6
- 3 SIGNAL RETURN FOR CCRWIN IS CONNECTED TO PIN 9.
- 4 SIGNAL RETURN FOR CCRW R IS CONNECTED TO PIN 8
- 5 ALL TERMINALS PREFIXED WITH E (E1, E2, ETC.) ARE TEST POINTS

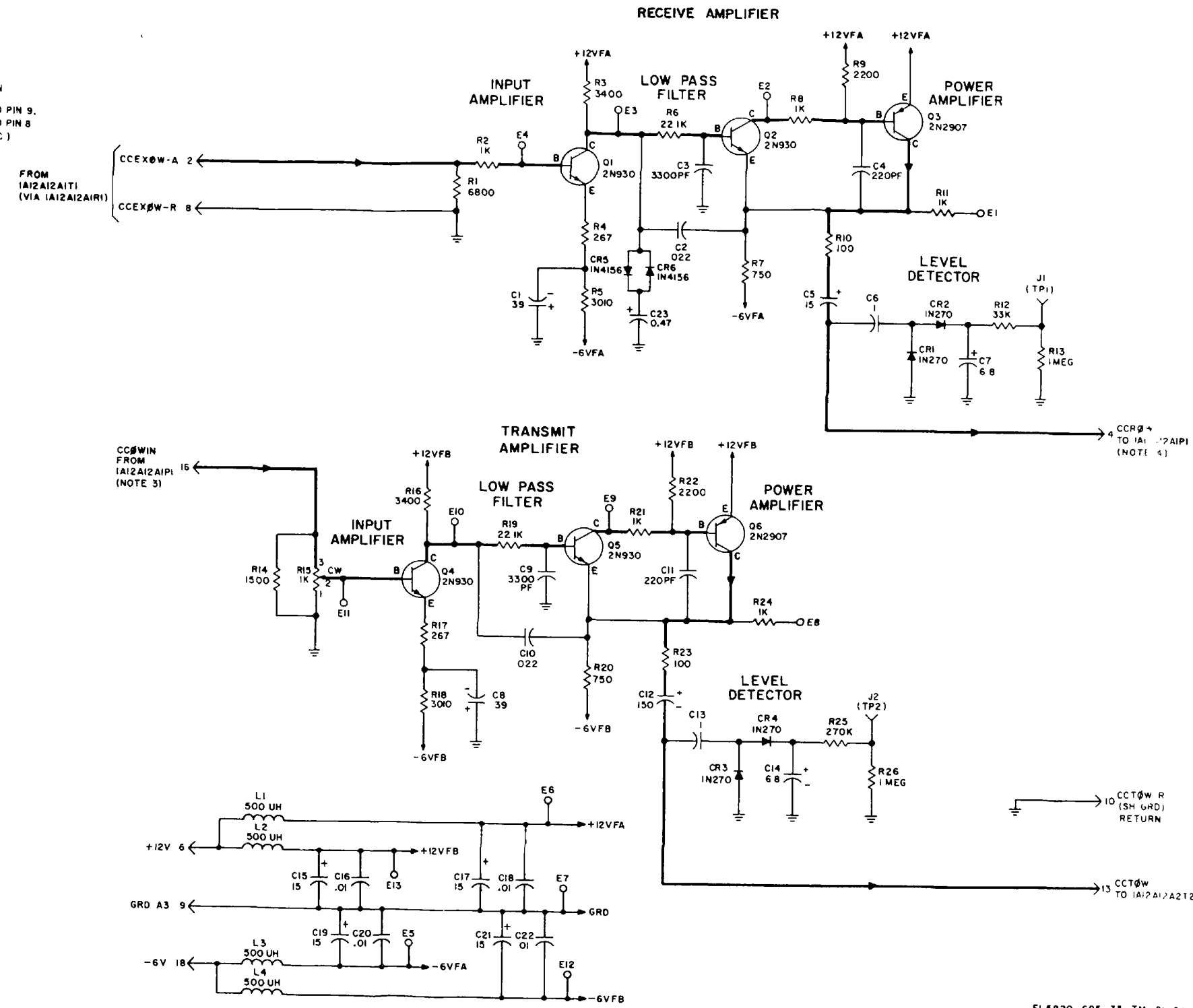


Figure 5-34. Af amplifier 1A12A6, schematic diagram.

- NOTES  
 1 UNLESS OTHERWISE SPECIFIED  
 RESISTANCES ARE IN OHMS  
 CAPACITANCES ARE IN MICROFARADS  
 INDUCTANCES ARE IN MICROHENRIES  
 2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.  
 PREFIX REFERENCE DESIGNATIONS WITH 1A12A7  
 3 ALL TERMINALS PREFIXED WITH E (E1, E2, ETC) ARE  
 TEST POINTS.  
 4 INTEGRATED CIRCUIT A1 IS TYPE MC1531G  
 5 CHARACTERISTICS CONTROLLED BY  
 SPECIFICATION DRAWING SM-B-652264  
 6 ON CONTRACT DAAB 05-72-C-5507,  
 R26 IS 36,500 OHMS

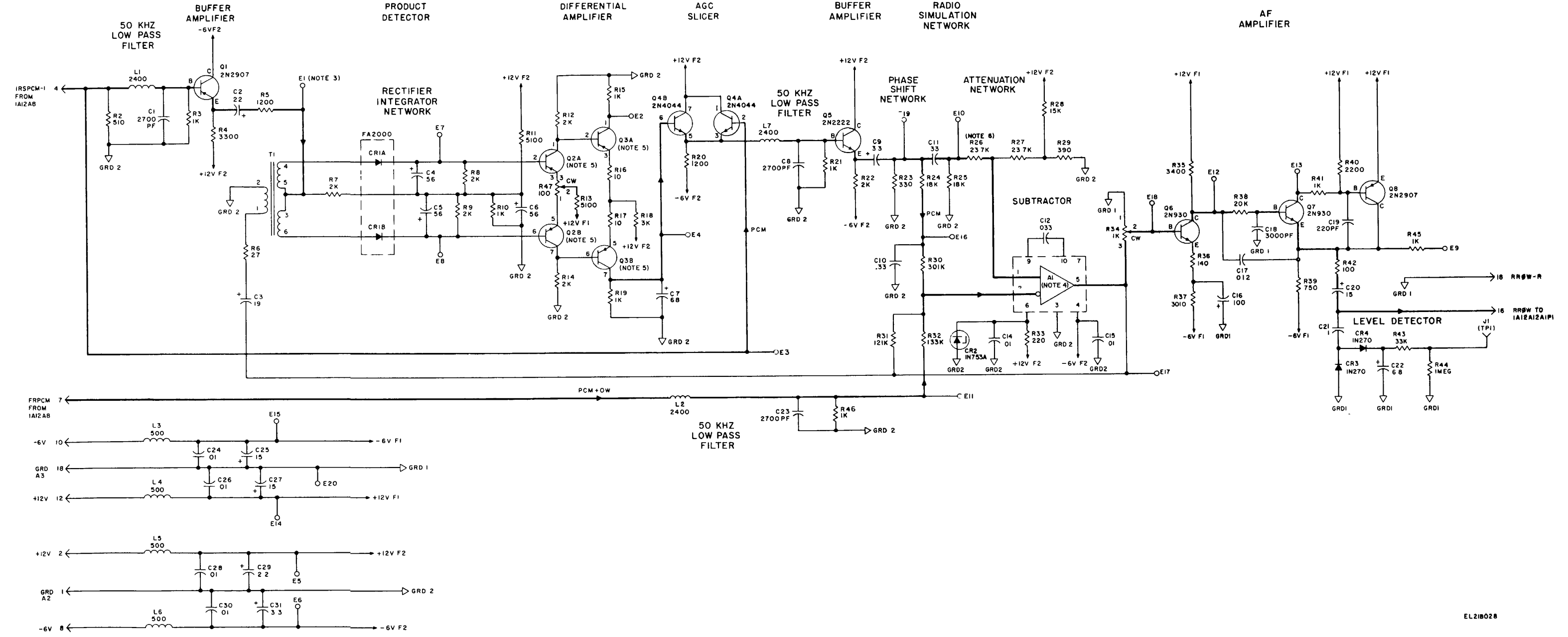


Figure 5-35. Radio-amplifier-detector 1A12A7, schematic diagram.

NOTES:

- UNLESS OTHERWISE SPECIFIED: RESISTANCES ARE IN OHMS. CAPACITANCES ARE IN MICROFARADS.
- PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX REFERENCE DESIGNATIONS WITH IA12A8.
- ALL TERMINALS PREFIXED WITH E (E1, E2, ETC.) ARE TEST POINTS.
- POWER CONNECTIONS FOR INTEGRATED CIRCUITS ARE SHOWN IN THE TABLE.

POWER CONNECTIONS		TYPE	
+5VF	GRD 2C		
A1	10	5	MC9446
A3	4	10	SG371-03
A4	4	10	SG141-03
A5	4	10	SG371-03
A6	SHOWN CONNECTED		U5B771031X
A7	SHOWN CONNECTED		U5B771031X
A8	SHOWN CONNECTED		U5B771031X
A9	SHOWN CONNECTED		U6A960151X
A10	SHOWN CONNECTED		U6A960151X
A11	SHOWN CONNECTED		SM-B-683816

- IN LOGIC SYMBOLS, THE NUMBER ABOVE THE REFERENCE DESIGNATOR IS PART OF TYPE DESIGNATOR.
- INTEGRATED CIRCUIT A11 IS A SPECIALLY SELECTED U5B771031X PER SPECIFICATION DRAWING SM-B-683816.
- CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM-B-652264.

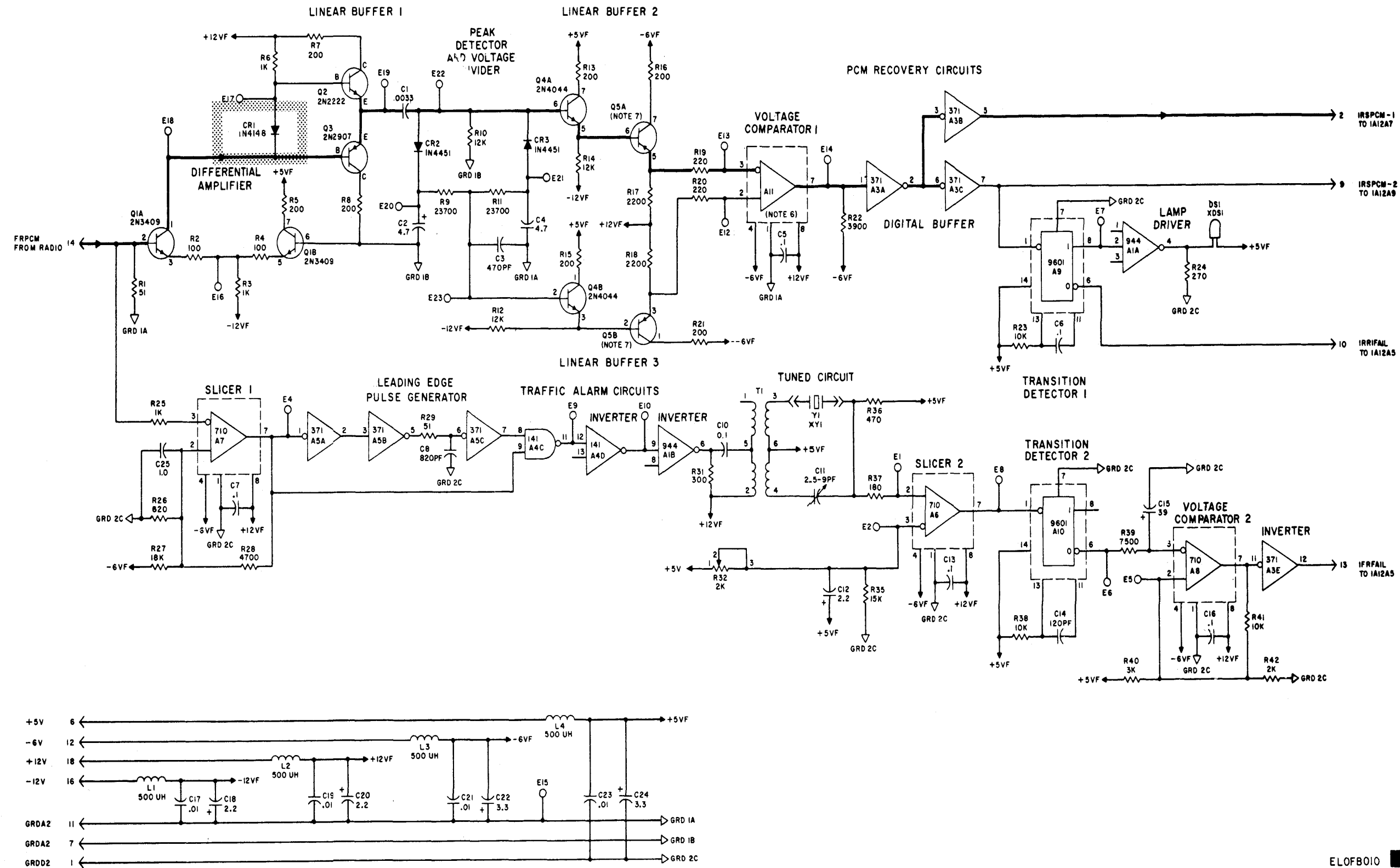
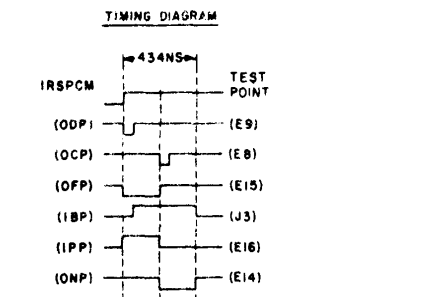


Figure 5-36. Radio digital regenerator 1A12A8, schematic diagram.  
Change 5 5-85



- NOTES:
- UNLESS OTHERWISE SPECIFIED: RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS, INDUCTANCES ARE IN MICROHENRIES.
  - PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, PREFIX REFERENCE DESIGNATIONS WITH IA12A9.
  - ALL TERMINALS PREFIXED WITH E (E1, E2, ETC.) ARE TEST POINTS.
  - POWER CONNECTIONS FOR INTEGRATED DIGITAL CIRCUITS ARE SHOWN IN THE TABLE.
  - IN THE LOGIC SYMBOL, THE NUMBER ABOVE THE REFERENCE DESIGNATOR IS PART OF TYPE DESIGNATOR.

POWER CONNECTIONS				
POS	+5VF	GRD	TYPE	
A2	4	10	SG221-03	
A3	4	10	SG141-03	
A4	4	10	SG141-03	
A5	4	10	SG141-03	
A6	A5 SHOWN		U6A9601SIX OR MIC-9601-ID	
A7	4	10	SG130-03	
A8	14	7	SN5474-J	
A9	14	7	SN5474-J	
A10	A5 SHOWN		RM711-D	
A1	A5 SHOWN		MC1531G	



6. SIGNAL MNEMONICS IN PARENTHESES ARE FOR ADDM ONLY.

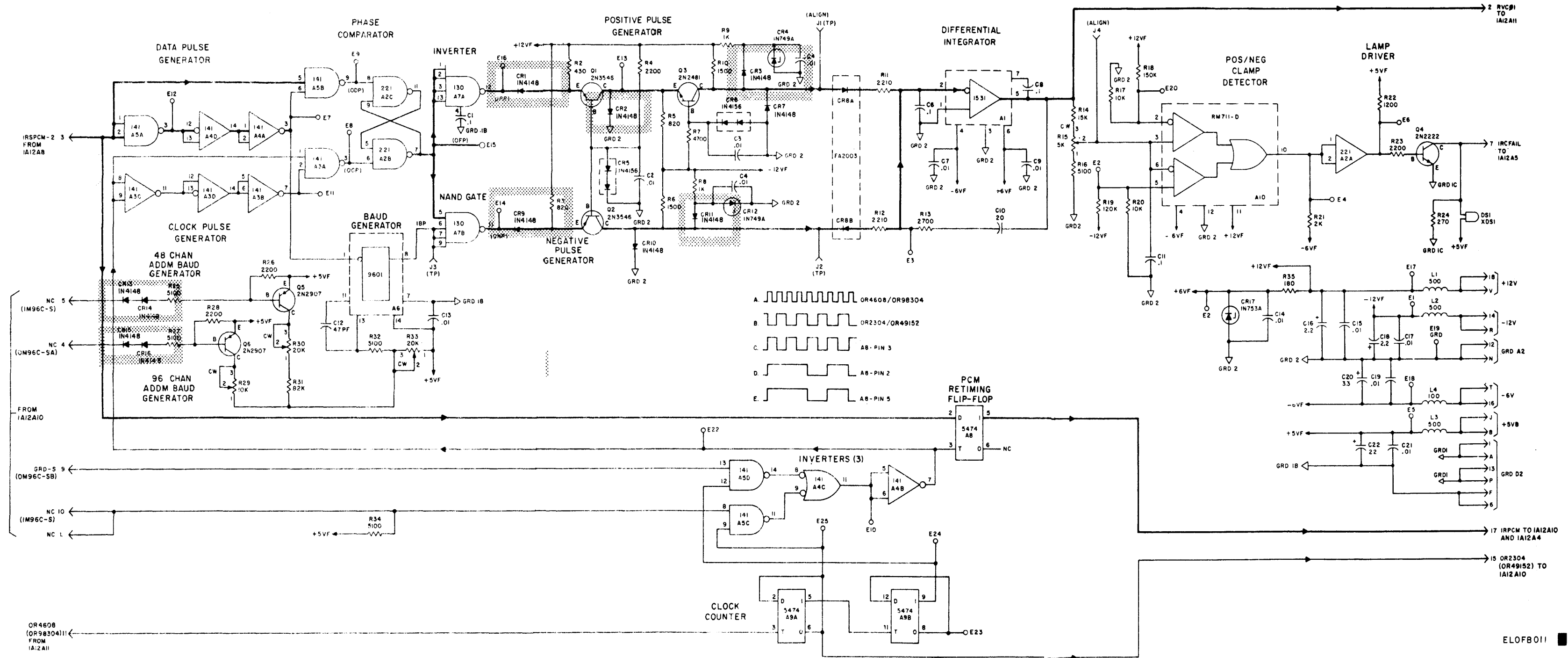


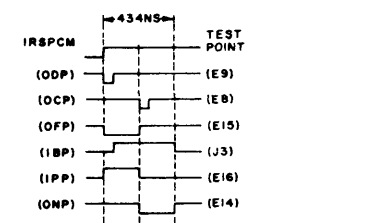
Figure 5-37. Radio control-comparator 1A12A9, schematic diagram.  
Change 5 5-87

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- NOTES**
- UNLESS OTHERWISE SPECIFIED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS, INDUCTANCES ARE IN MICROHENRIES
  - PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; PREFIX REFERENCE DESIGNATIONS WITH 1A12A9 ARE TEST POINTS
  - ALL TERMINALS PREFIXED WITH E (E1, E2, ETC.) ARE TEST POINTS
  - POWER CONNECTIONS FOR INTEGRATED DIGITAL CIRCUITS ARE SHOWN IN THE TABLE
  - IN THE LOGIC SYMBOL, THE NUMBER ABOVE THE REFERENCE DESIGNATOR IS PART OF TYPE DESIGNATOR

POWER CONNECTIONS				
POS	+5VF	GRD	TYPE	
A2	4	10	SG221-03	
A3	4	10	SG141-03	
A4	4	10	SG141-03	
A5	4	10	SG141-03	
A6	A5 SHOWN		US8A9601SX OR MIC-9601-ID	
A7	4	10	SG130-03	
AB	14	7	SN5474-J	
AB	14	7	SN5474-J	
A10	A5 SHOWN		RM711-D	
A1	A5 SHOWN		MC1531G	

**TIMING DIAGRAM**



8. SIGNAL MNEMONICS IN PARENTHESES ARE FOR ADDM ONLY.

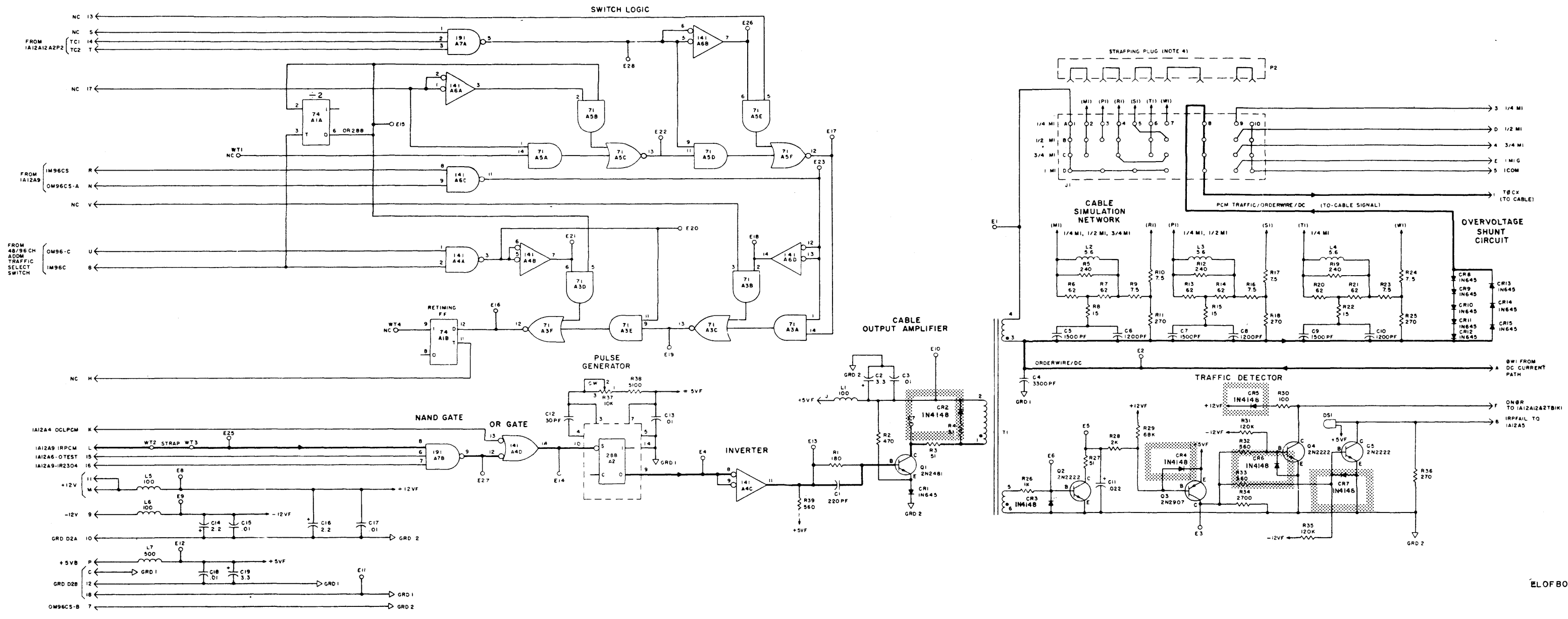


Figure 5-38. Radio digital processor 1A12A10, schematic diagram, synchronous mode. Change 5 5-89.

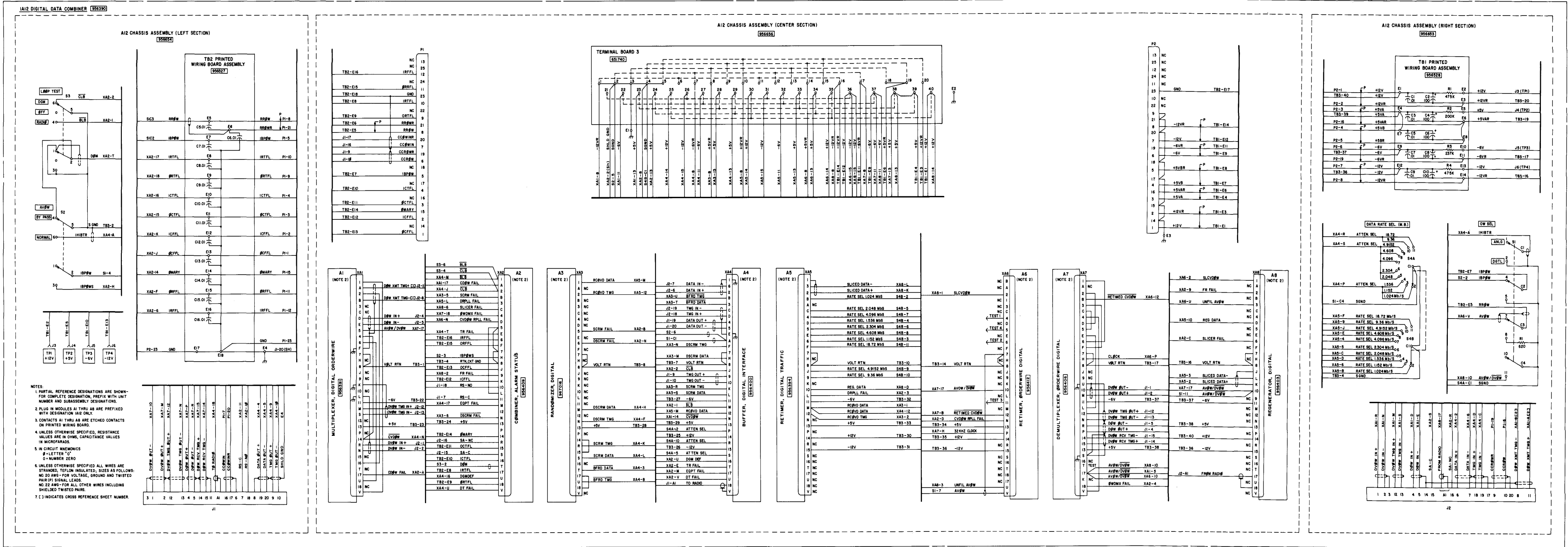


Figure 5-38.2. Digital data combiner 1A12, interconnecting diagram.  
 Change 6 5-89.3

- NOTE
- UNLESS OTHERWISE SPECIFIED CAPACITORS ARE IN MICROFARADS, INDUCTORS ARE IN MICROHENRIES, RESISTORS ARE IN OHMS AND ARE 1/4 WATT, 5 PERCENT
  - PARTIAL REFERENCE DESIGNATION ARE SHOWN FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION
  - POWER CONNECTIONS FOR INTEGRATED DIGITAL CIRCUITS ARE SHOWN IN THE TABLE BELOW DEVICE TYPE NUMBERS AND ILLUSTRATIONS ARE SHOWN IN FIGURE 5-24.1.

LOC	DEVICE	V <sub>CC</sub>	GND	-6V
U4,U10	SN55107	14	7	13
U6,U13	54LS00	14	7	
U9	54LS74	14	7	
U11	54LS86	14	7	
U8,U12	54LS123	16	8	
U2,U3	54LS161	16	8	
U5	54LS175	16	8	
U7	54S04	14	7	
U1	MC12561	1,11,16	8,9	

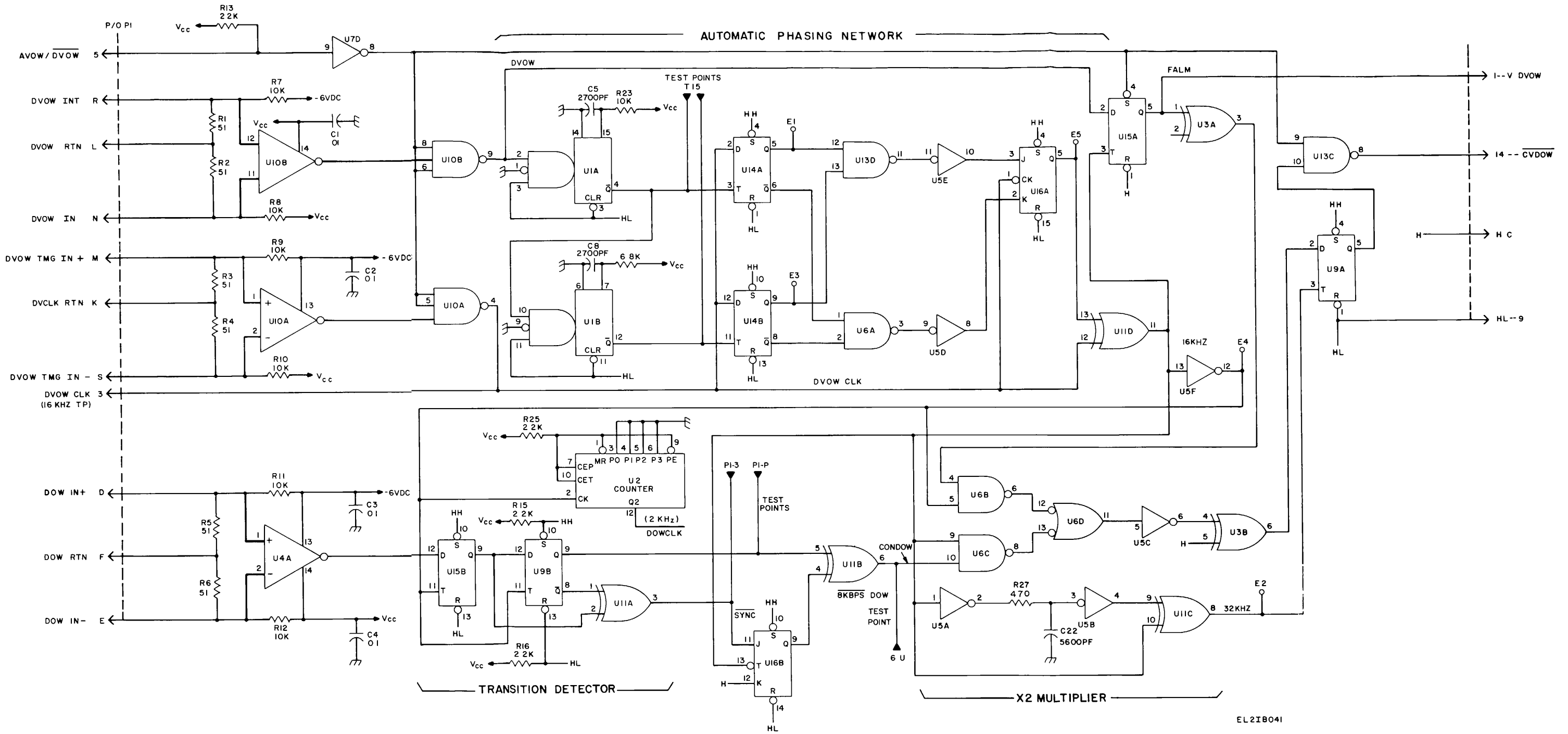


Figure 5-38.3(1). Multiplexer, digital orderwire 1A12A1, schematic diagram (sheet 1 of 4).  
Change 6 5-89.5

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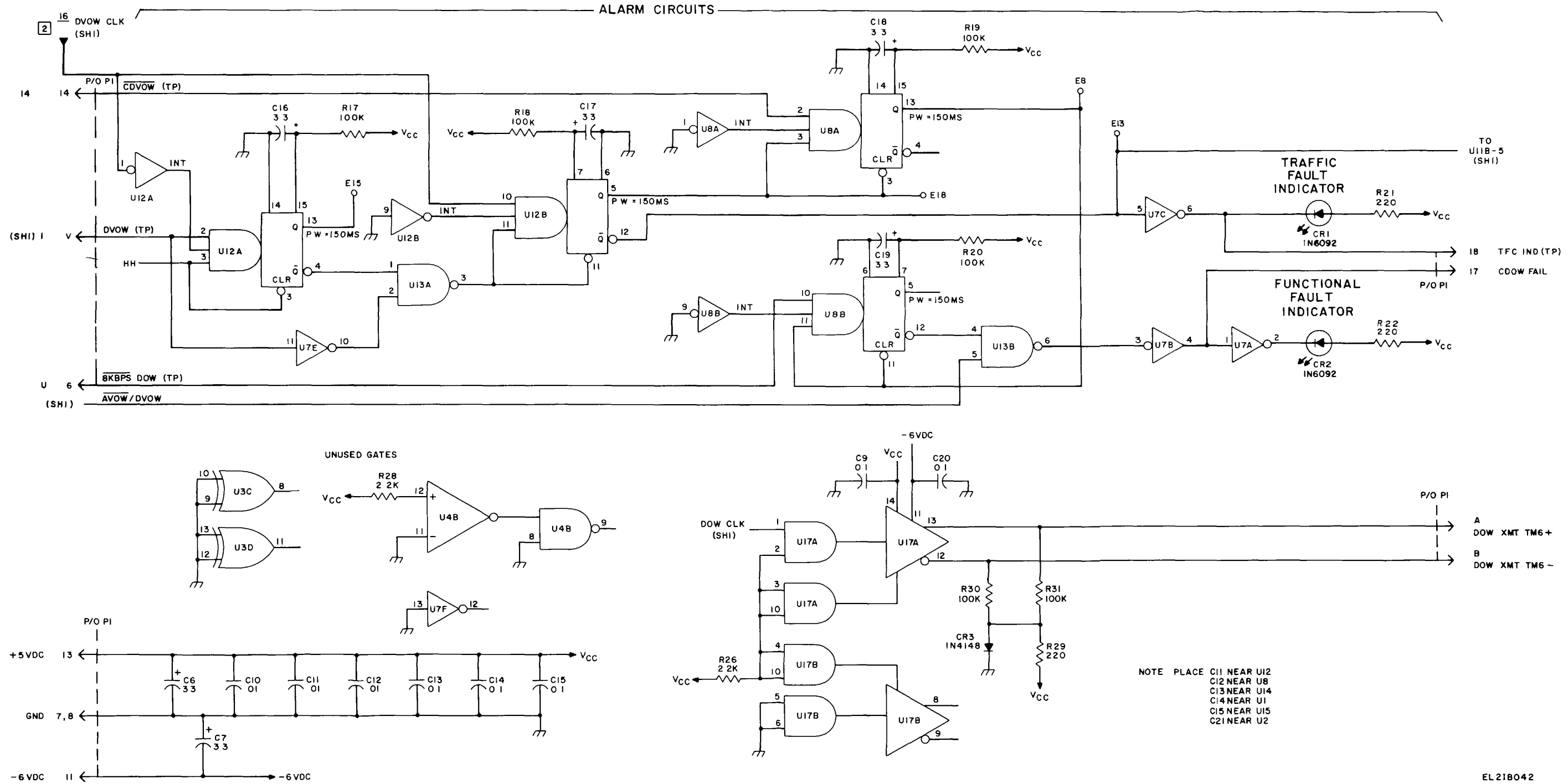
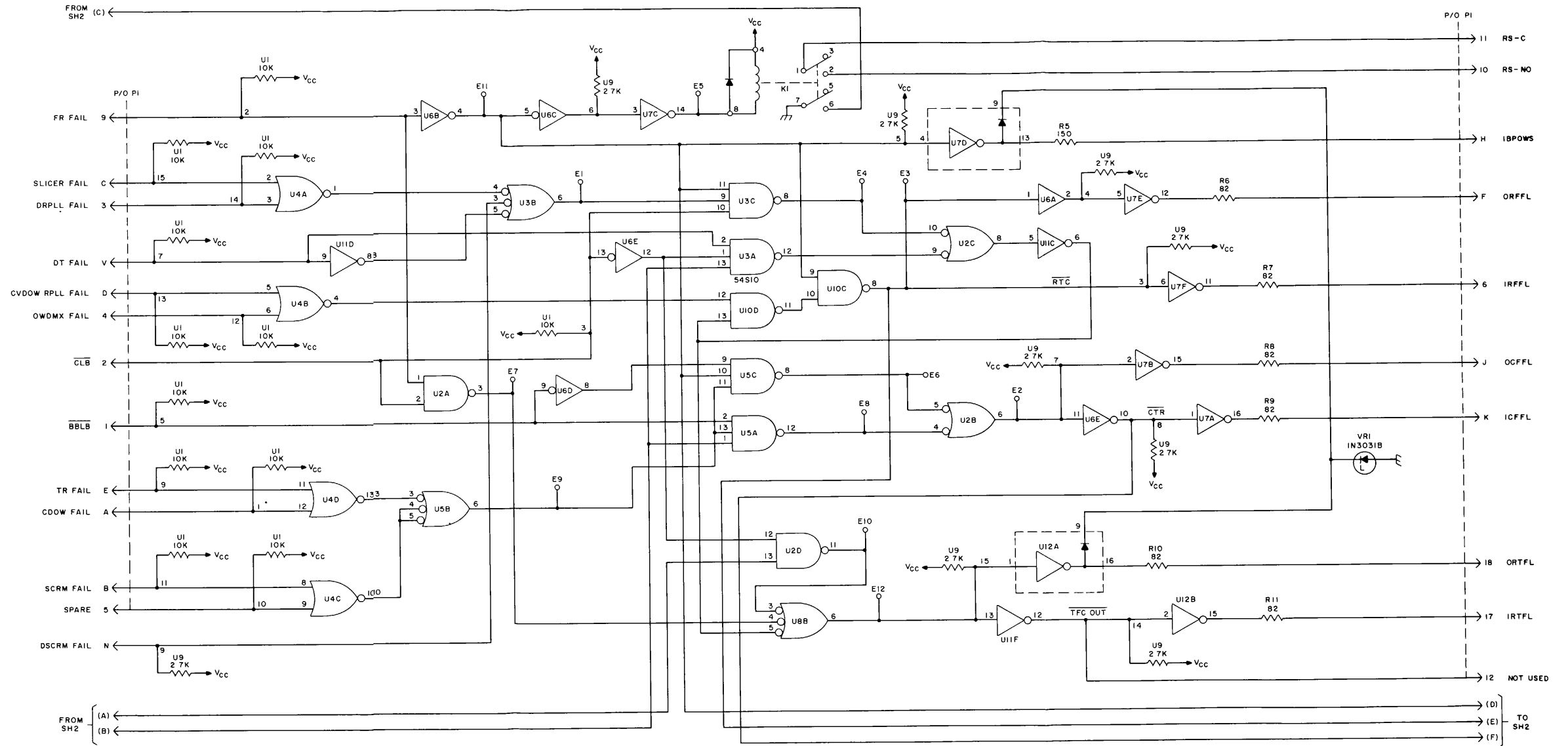


Figure 5-38.3(2). Multiplexer, digital orderwire 1A12A1, schematic diagram (sheet 2 of 4).  
Change 6 5-89.7

- NOTE**
- UNLESS OTHERWISE SPECIFIED CAPACITORS ARE IN MICROFARADS, INDUCTORS ARE IN MICROHENRIES, RESISTORS ARE IN OHMS AND ARE 1/4 WATT, 5 PERCENT
  - PARTIAL REFERENCE DESIGNATION ARE SHOWN FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION
  - POWER CONNECTIONS FOR INTEGRATED DIGITAL CIRCUITS ARE SHOWN IN THE TABLE BELOW DEVICE TYPE NUMBERS AND ILLUSTRATIONS ARE SHOWN IN FIGURE 5-241

LOC	DEVICE	V <sub>CC</sub>	GND	
U2, U10	54S00	14	7	SEE NOTE 6
U4	54S02	14	7	
U6, U11	54S04	14	7	SEE NOTE 4
U3, U5, U8	54S10	14	7	
U7, U12	ULN2003A		8	
U1	898-1-R27K	16		
U9	898-1-R27K	16		SEE NOTE 5

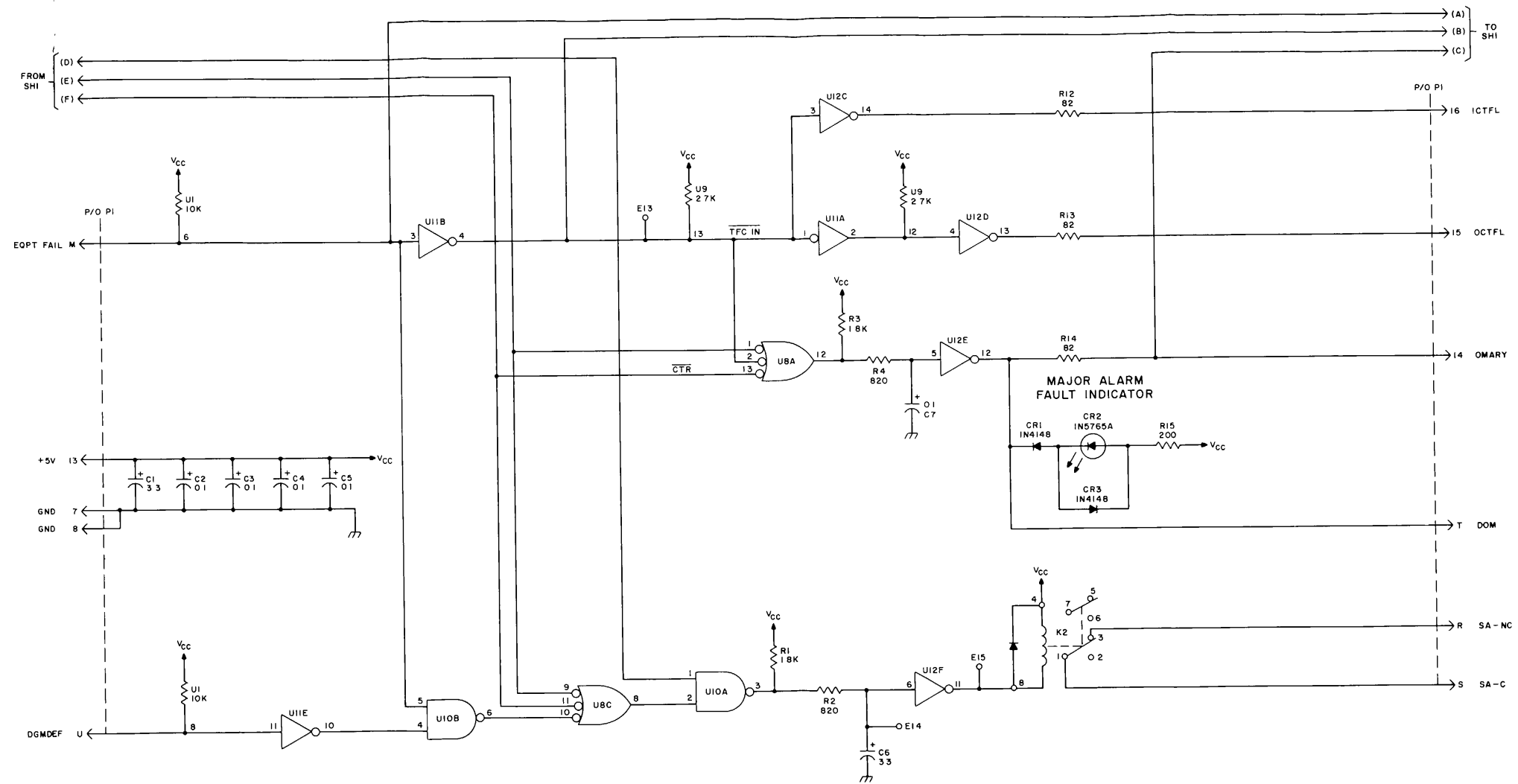
- U7 & U12 EACH CONTAIN 1 UNUSED DARLINGTON TRANSISTOR ARRAY (U7G, PINS 7, 10 U12G, PINS 7, 10) U7 & U12 PIN 9 USED FOR COMMON CONNECTIONS
- U9 CONTAINS 4 UNUSED 27K RESISTORS (PINS 1, 2, 10, 11)
- U10 CONTAINS 2 UNUSED GATES (U10C PINS 8, 9, 10 U10D PINS 11, 12, 13)



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Figure 5-38.4 (1). Combiner, alarm-status 1A12A2, schematic diagram (sheet 1 of 2).

Change 6 5-89.9



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Figure 5-38.4 (2).Combiner, alarm-status 1A12A2, schematic diagram (Sheet 2 of 2).

Change 6 5-89.11

NOTE  
 1 UNLESS OTHERWISE SPECIFIED:  
 CAPACITORS ARE IN MICROFARADS, INDUCTORS ARE  
 IN MICROHENRIES, RESISTORS ARE IN OHMS  
 AND ARE 1/4 WATT, 5 PERCENT  
 2 PARTIAL REFERENCE DESIGNATION ARE SHOWN FOR  
 COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER  
 AND SUB-ASSEMBLY DESIGNATION  
 3 POWER CONNECTIONS FOR INTEGRATED DIGITAL  
 CIRCUITS ARE SHOWN IN THE TABLE BELOW  
 DEVICE TYPE NUMBERS AND ILLUSTRATIONS  
 ARE SHOWN IN FIGURE 5-241

LOC	DEVICE	V <sub>CC</sub>	GND
U1, U3, U7, U10	54LS164	14	7
U2, U4, U6, U8	54S74	14	7
U5, U9	54LS123	16	8
U11, U15	54S86	14	7
U12, U13	54S140	14	7
U14	54LS00	14	7

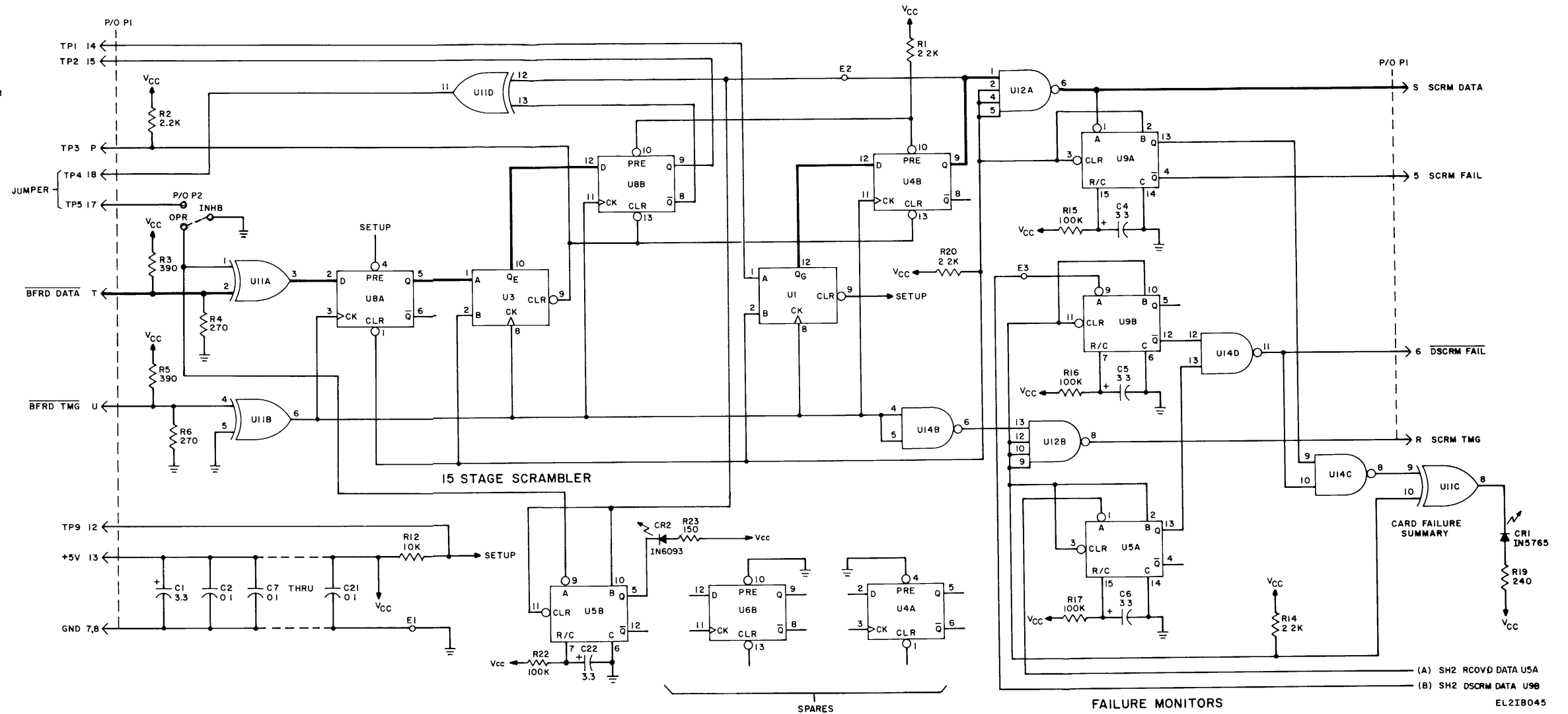


Figure 5-38.5 (1). Digital randomizer 1A12A3, schematic diagram (sheet 1 of 2).

Change 6 5-89.13.



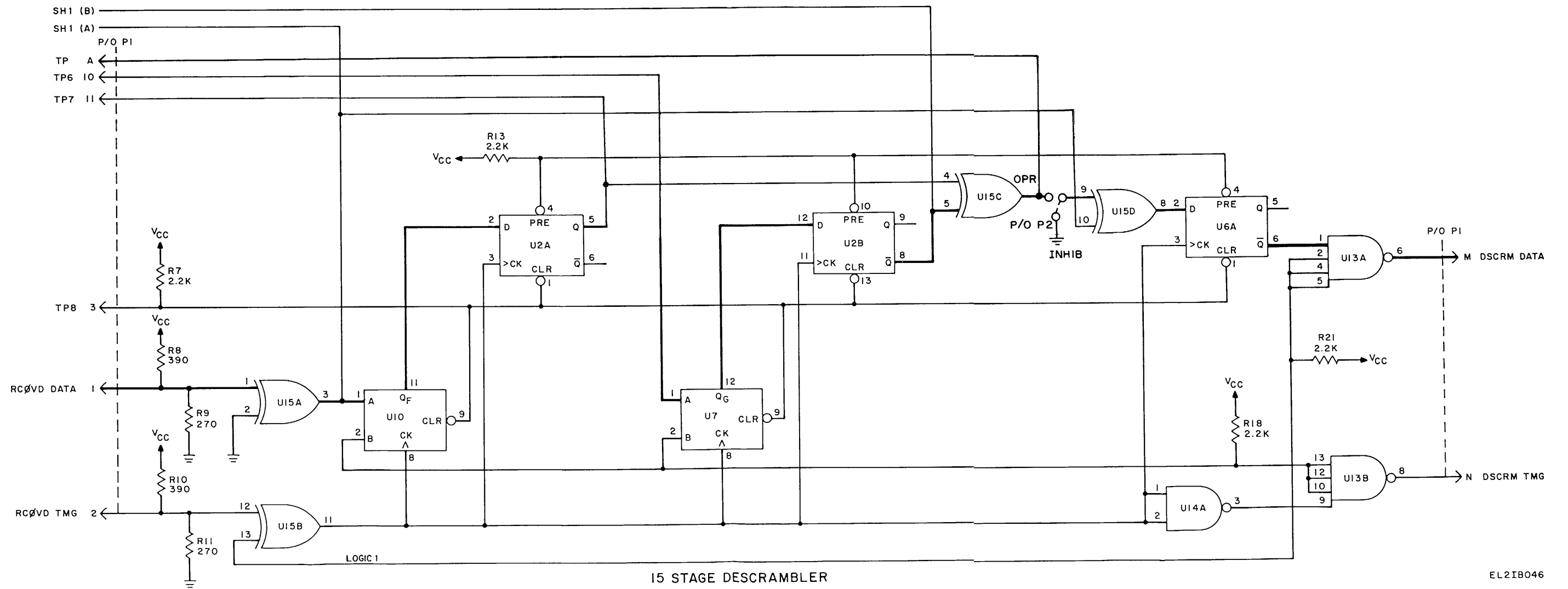


Figure 5-38.5 (2).Digital randomizer 1A12A3, schematic diagram (sheet 2 of 2).

Change 6 5-89.15.

NOTE  
 1 UNLESS OTHERWISE SPECIFIED CAPACITORS ARE IN MICROFARADS, INDUCTORS ARE IN MICROHENRIES, RESISTORS ARE IN OHMS AND ARE 1/4 WATT, 5 PERCENT  
 2 PARTIAL REFERENCE DESIGNATION ARE SHOWN FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION  
 3 POWER CONNECTIONS FOR INTEGRATED DIGITAL CIRCUITS ARE SHOWN IN THE TABLE BELOW  
 DEVICE TYPE NUMBERS AND ILLUSTRATIONS ARE SHOWN IN FIGURE 5-24 1

LOC	DEVICE	Vcc	GRD	-6V	O 1 BYPASS CAP
U1	SOB	14	7		C19
U2,U9	54LS123	16	8		C20,C24
U3	S140	14	7		C21
U4	55107AN	14	7	13	
U5	LS00	14	7		
U6	SO4	14	7		C22
U7,U2	LS158	16	8		C23,C26
U8	SO2	14	7		
U10	55109AN	14	7		
U11	S74	16	8		C25
U13	5426	14	7		
U14	SEE SHEET 2, ZONE 7 B				
U15	SO7	14	7		
U12	LS352	15	1		

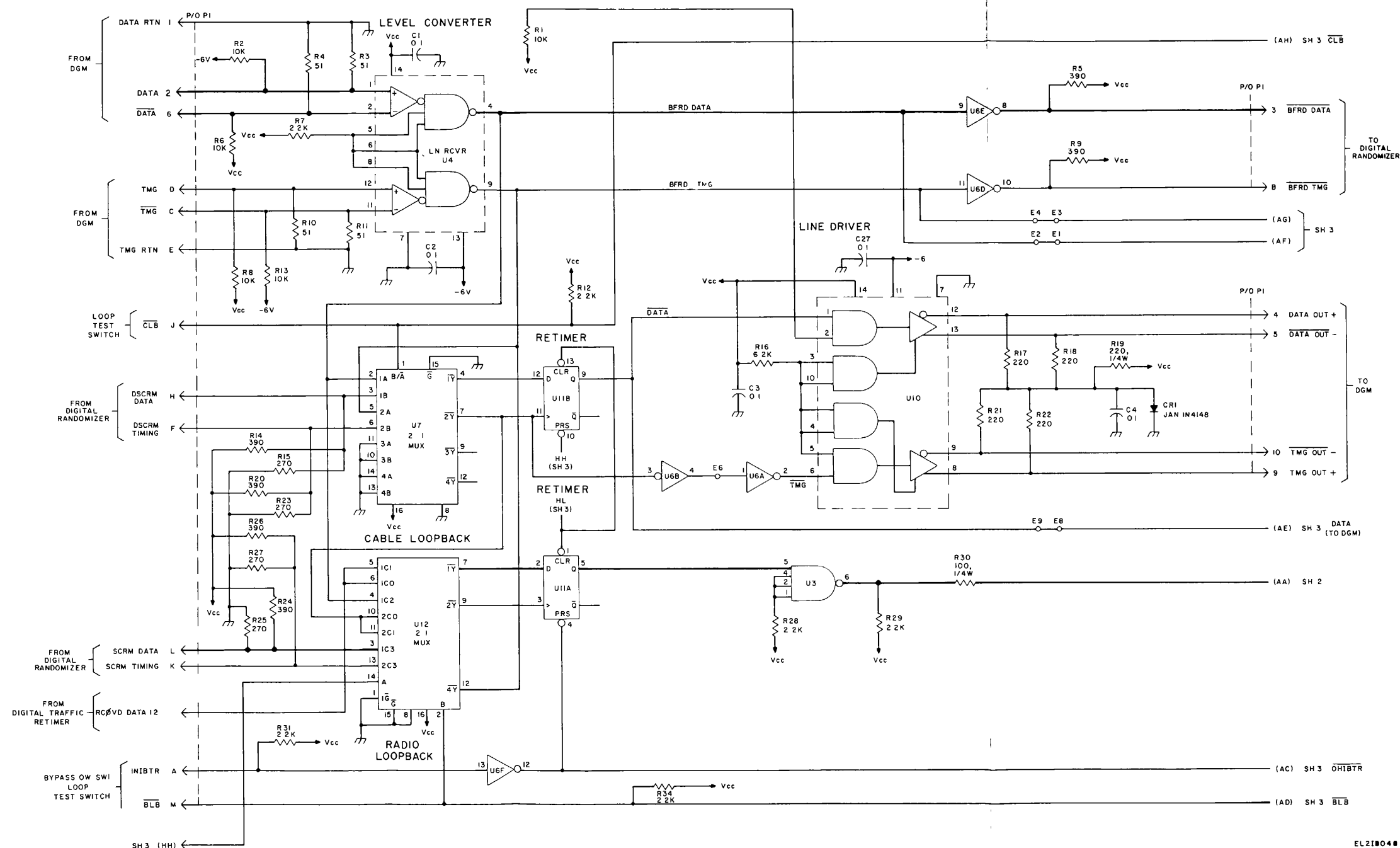


Figure 5-38.6 (1). Buffer, digital interface 1A12A4, schematic diagram (sheet 1 of 3).

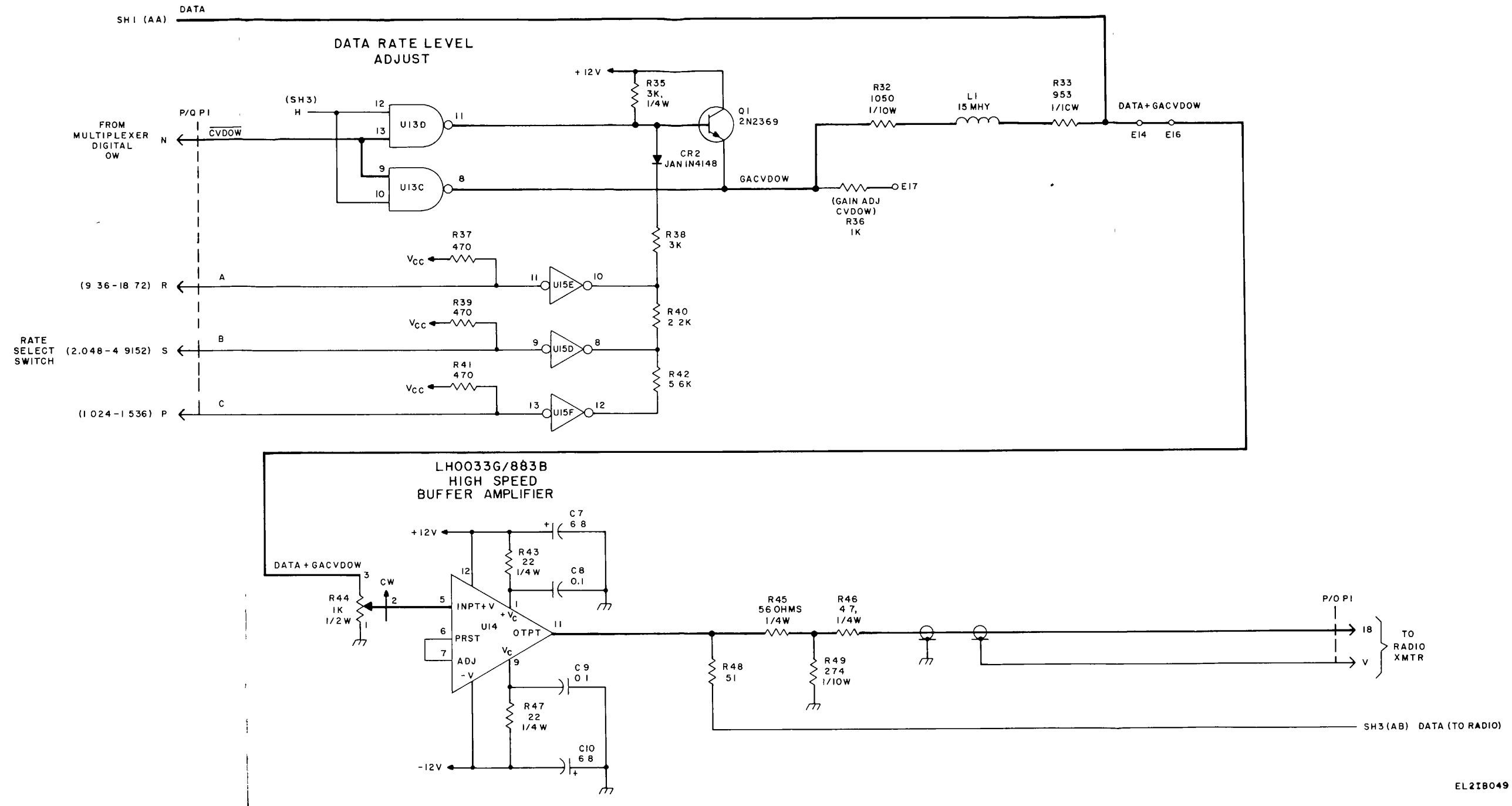


Figure 5-38.6 (2). Buffer, digital interface 1A12A4, schematic diagram (Sheet 2 of 3).

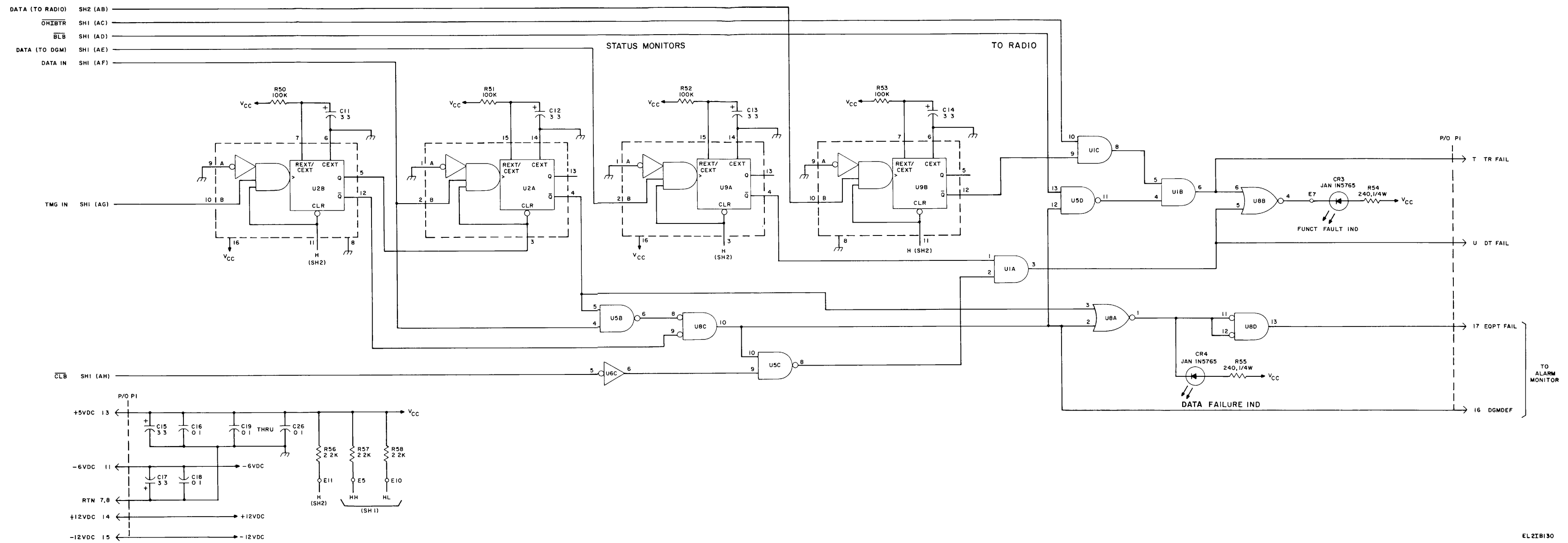


Figure 5-38.6(3). Buffer, digital interface 1A12A4, schematic diagram (sheet 3 of 3).  
Change 6 5-89.21

- NOTE**
- UNLESS OTHERWISE SPECIFIED CAPACITORS ARE IN MICROFARADS, INDUCTORS ARE IN MICRONHENRIES, RESISTORS ARE IN OHMS AND ARE 1/4 WATT, ± 5 PERCENT
  - PARTIAL REFERENCE DESIGNATION ARE SHOWN FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION
  - DIODES CR1 THROUGH CR4 ARE PURCHASED PER PL-SM-B-9563940
  - POWER CONNECTIONS FOR INTEGRATED DIGITAL CIRCUITS ARE SHOWN IN THE TABLE BELOW

LOC	DEVICE	VCC	GND	+12V	-12V	-6V
U1	DG182A	7	8	6	9	
U2	5406	14	7,11,13			
U3	AM686	3	11,12			6
U4	LM108L			11	7	
U5	54S163	16	8			
U6	54LS11	14	7			
U7	54LS20	14	7			
U8	1K RES NET	16				
U9	LM2111		2,10	1	5	
U10	54LS04	14	7,13			
U11	54LS00	14	7,13			
U12	54LS74	14	7			
U13	54S86	14	7			
U14	54S51	14	7			
U15	54LS74	14	7,13			
U16	54S03	14	7,13			
U17	54S140	14	7			
U18	MC12561	1	8-16			
U19	AM686		11,12			
U20	54LS123	16	1,6,8,14			

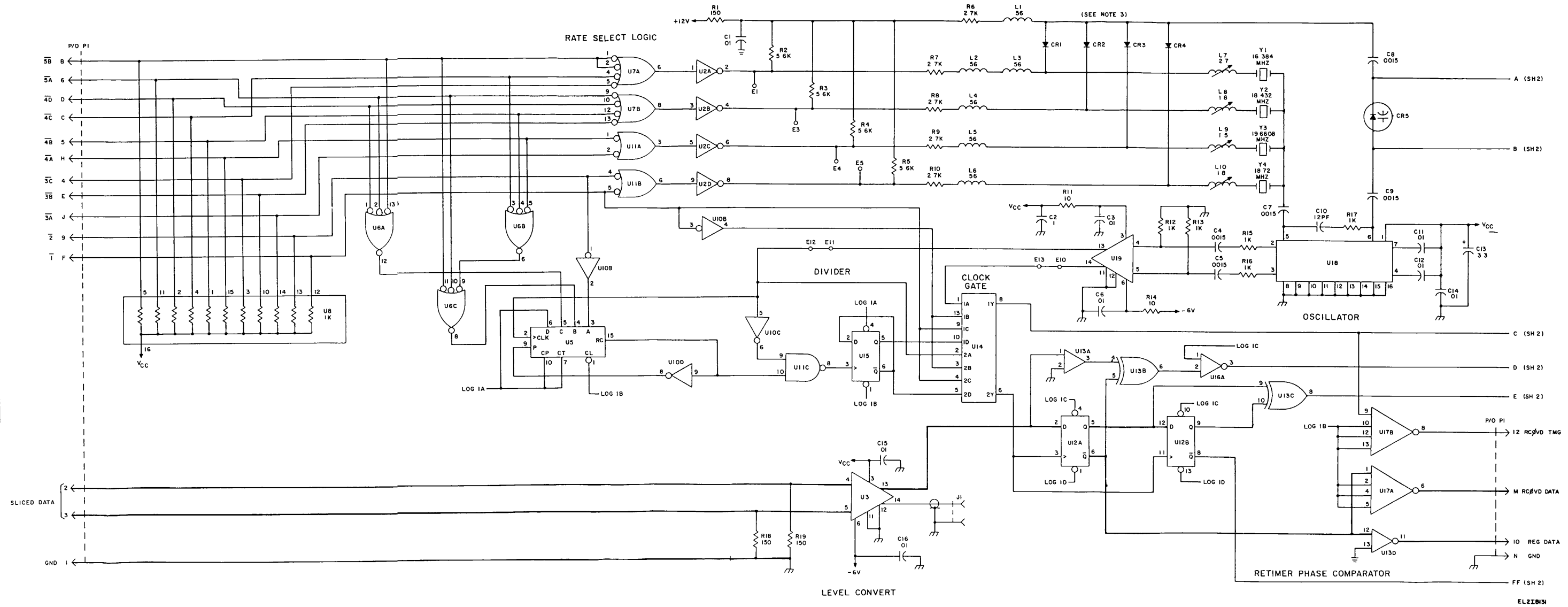


Figure 5-38.7(1). Retimer, digital traffic 1A12A5, schematic diagram (sheet 1 of 2)  
Change 5 5-89.23

NOTE  
 1 UNLESS OTHERWISE SPECIFIED CAPACITORS ARE IN MICROFARADS, INDUCTORS ARE IN MICROHENRIES, RESISTORS ARE IN OHMS AND ARE 1/4 WATT, 5 PERCENT  
 2 PARTIAL REFERENCE DESIGNATION ARE SHOWN FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION  
 3 POWER CONNECTIONS FOR INTEGRATED DIGITAL CIRCUITS ARE SHOWN IN THE TABLE BELOW  
 DEVICE TYPE NUMBERS AND ILLUSTRATIONS ARE SHOWN IN FIGURE 5-24 1

LOC	DEVICE	V <sub>cc</sub>	GND	μF BY PASS
U2	LS86	14	7	C38
U3	LS12	14	7	C33
U5	LS74	14	7	C34
U6	LS74	14	7	C35
U8	LS123	16	8	C36
U9	Q4	14	7	C37
U7, U10	747	-	-	-
U1	XR2207	-	-	-
U4	LM1081	-	-	-
U11	LS02	14	7	-

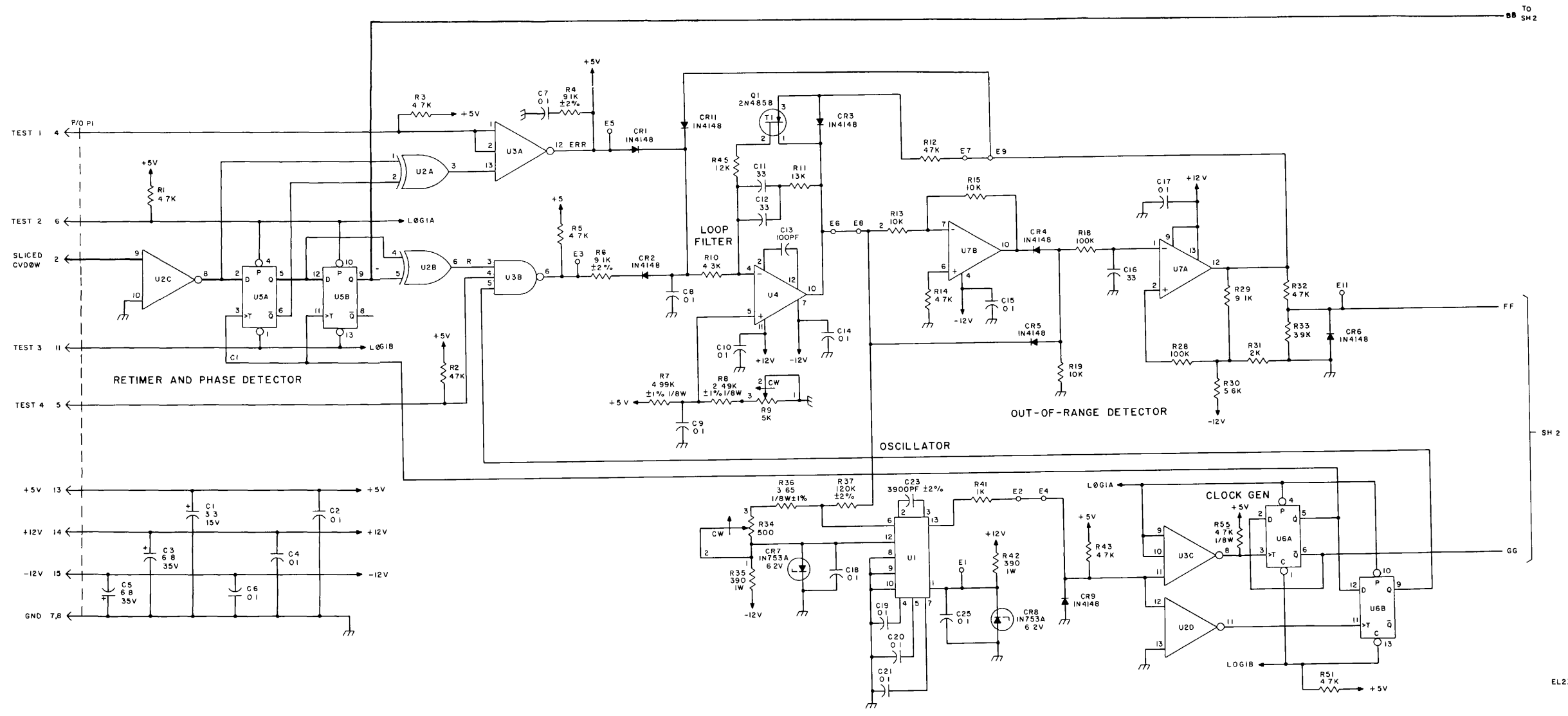
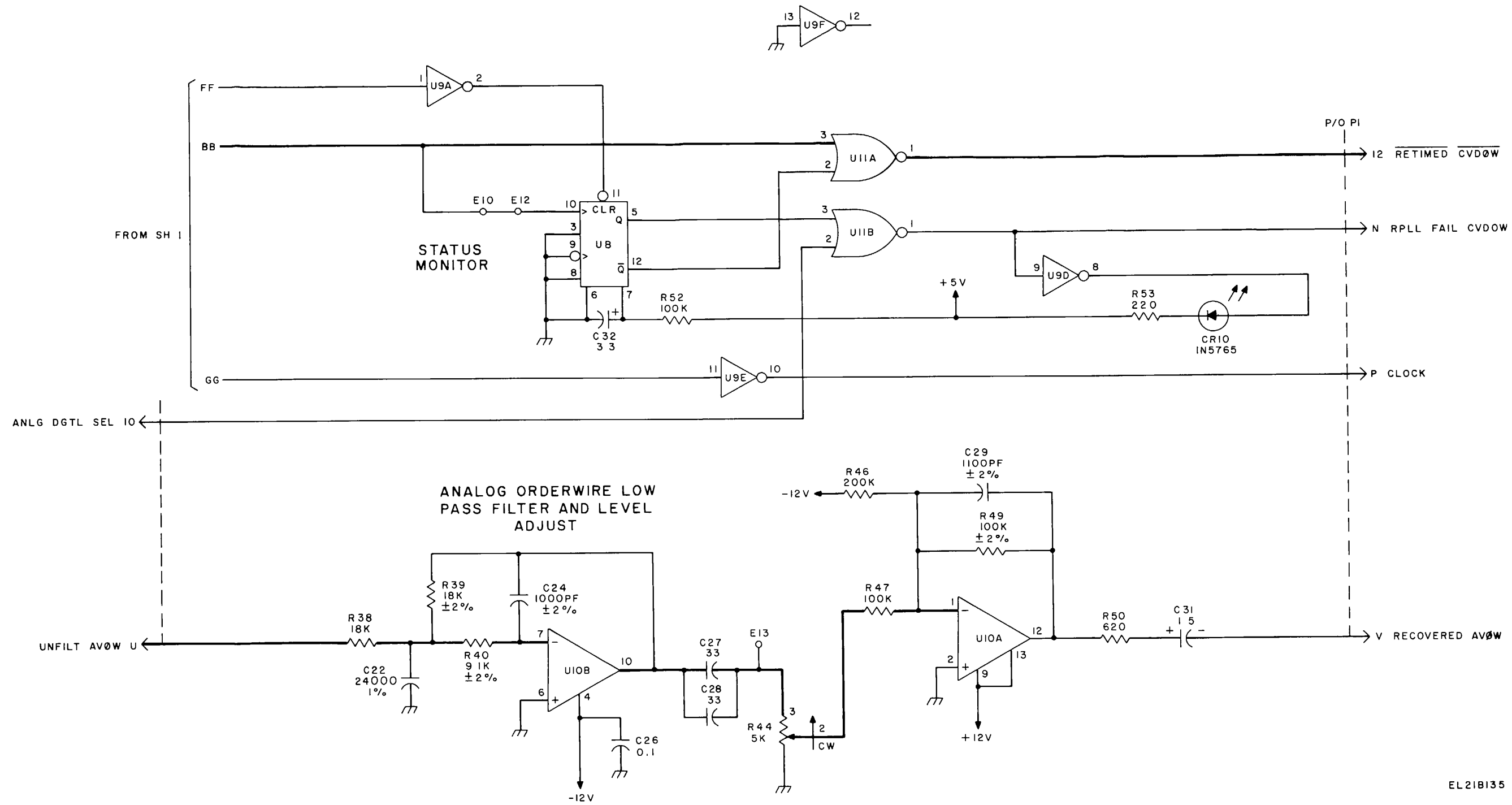


Figure 5-38.8 (1). Retimer, digital orderwire 1A12A6, schematic diagram (sheet 1 of 2).  
 Change 6 5-89.27

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Figure 5-38.8(2). Retimer, digital orderwire 1A12A6, schematic diagram (sheet 2 of 2).  
Change 6 5-89.29

- NOTE
- UNLESS OTHERWISE SPECIFIED, CAPACITORS ARE IN MICROFARADS, INDUCTORS ARE IN MICROHENRIES, RESISTORS ARE IN OHMS AND ARE 1/4 WATT, 5 PERCENT
  - PARTIAL REFERENCE DESIGNATION ARE SHOWN FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION
  - DECOUPLING CAPACITORS C11 THRU C14 WILL BE ADJACENT TO DIPS AS FOLLOWS: 1 FOR EVERY 3 DIPS
  - POWER CONNECTIONS FOR INTEGRATED DIGITAL CIRCUITS ARE SHOWN IN THE TABLE BELOW. DEVICE TYPE NUMBERS AND ILLUSTRATIONS ARE SHOWN IN FIGURE 5-24 1

LOC	DEVICE	VCC	GND
U1,U2,U10	LS175	16	8
U3	LS191	16	8
U4	LS04	14	7
U5	LS86	14	7
U6	LS00	14	7
U7	LS74	14	7
U8,U9	SN5109A	14	7
U11	LS123	16	8
U12	LS10	14	7
U13	S04	14	7

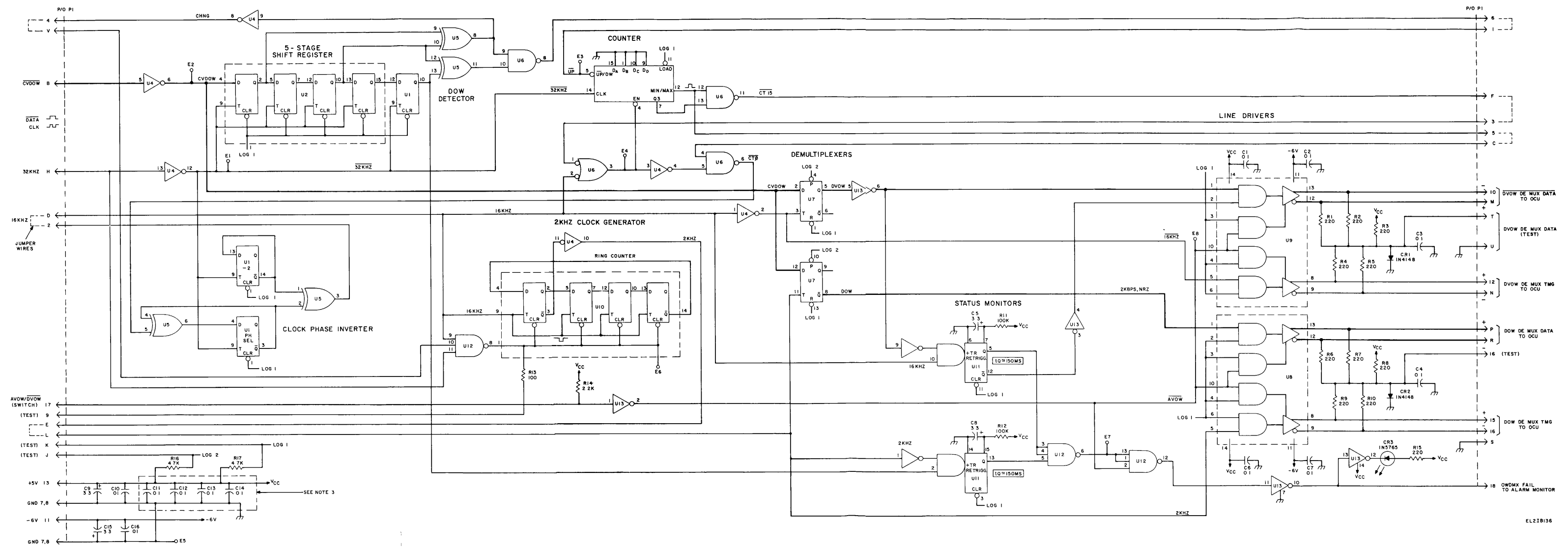
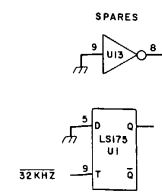


Figure 5-38.9. Demultiplexer, digital orderwire, 1A12A7, schematic diagram.  
Change 6 5-89.31

EL21B136



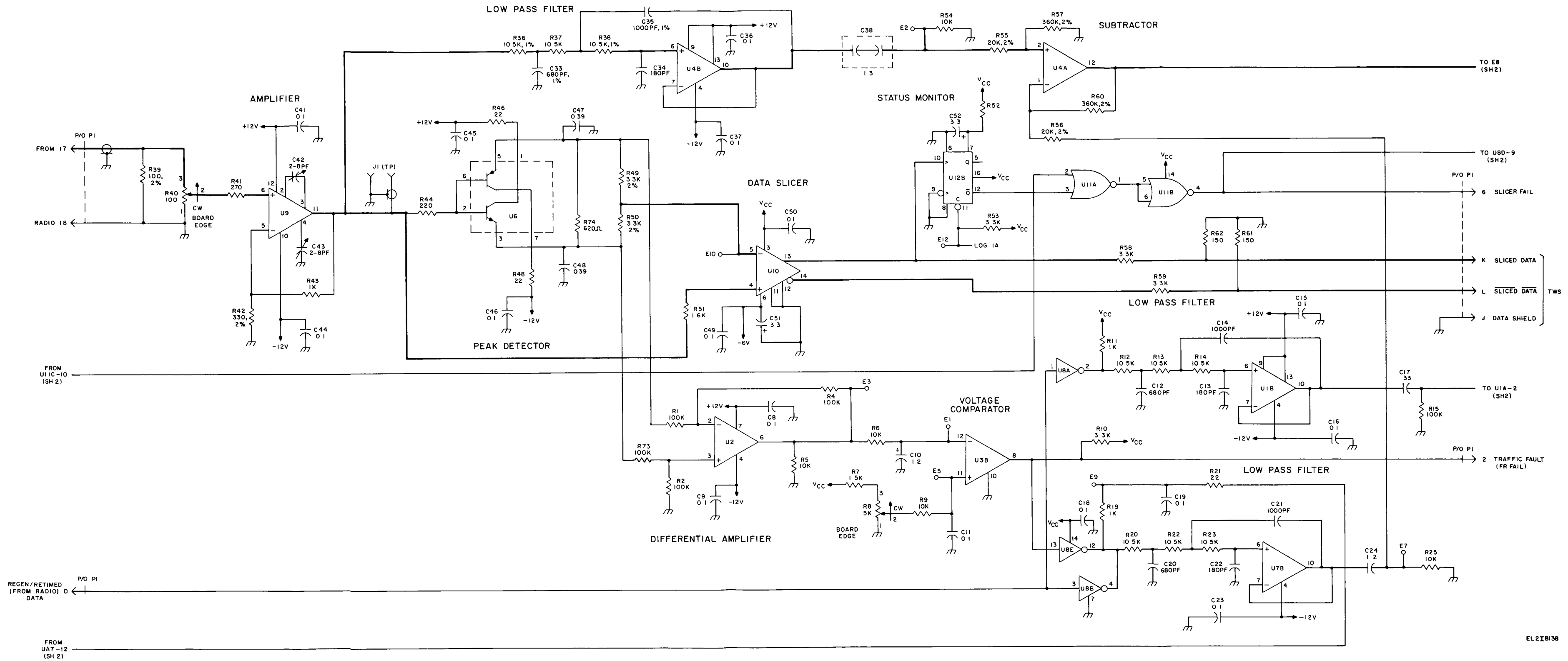


Figure 5-38.10 (1). Regenerator, digital 1A12A8, schematic diagram (sheet 1 of 2).  
Change 6 5-89.33

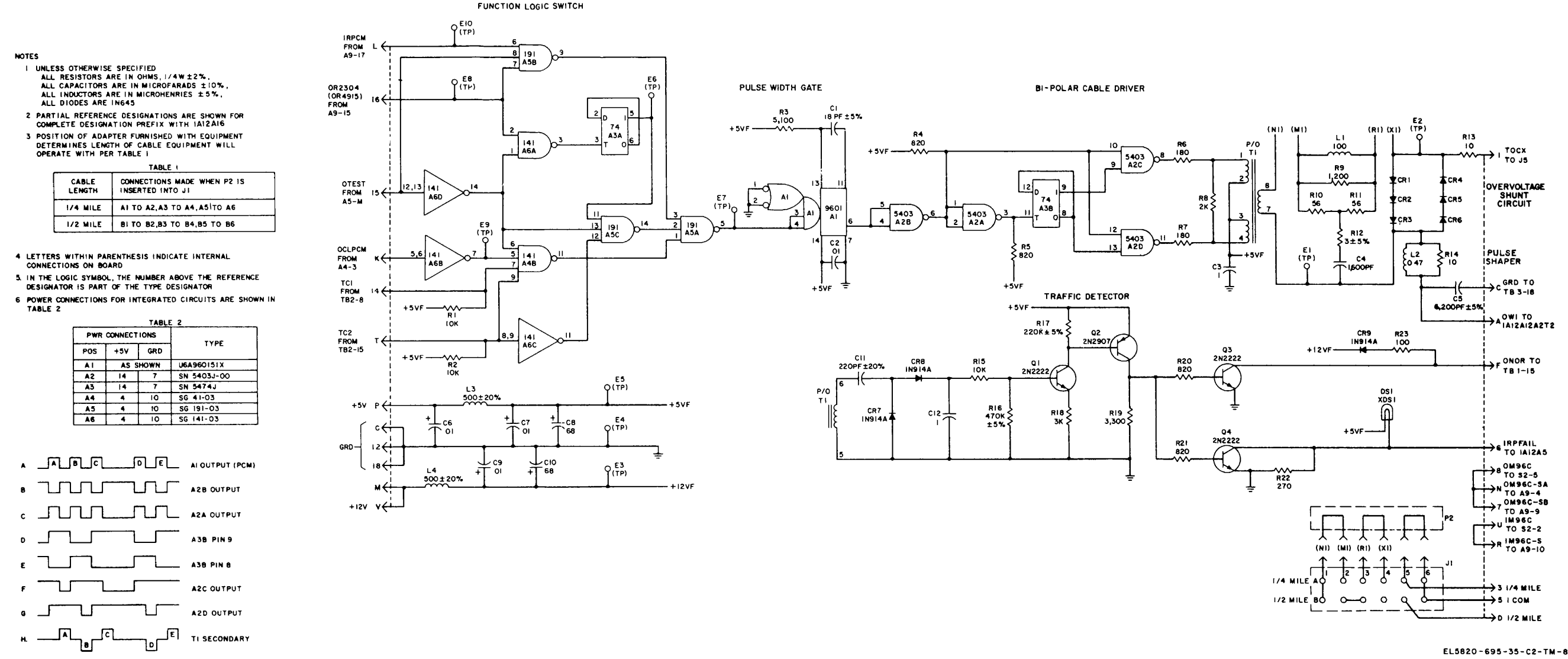
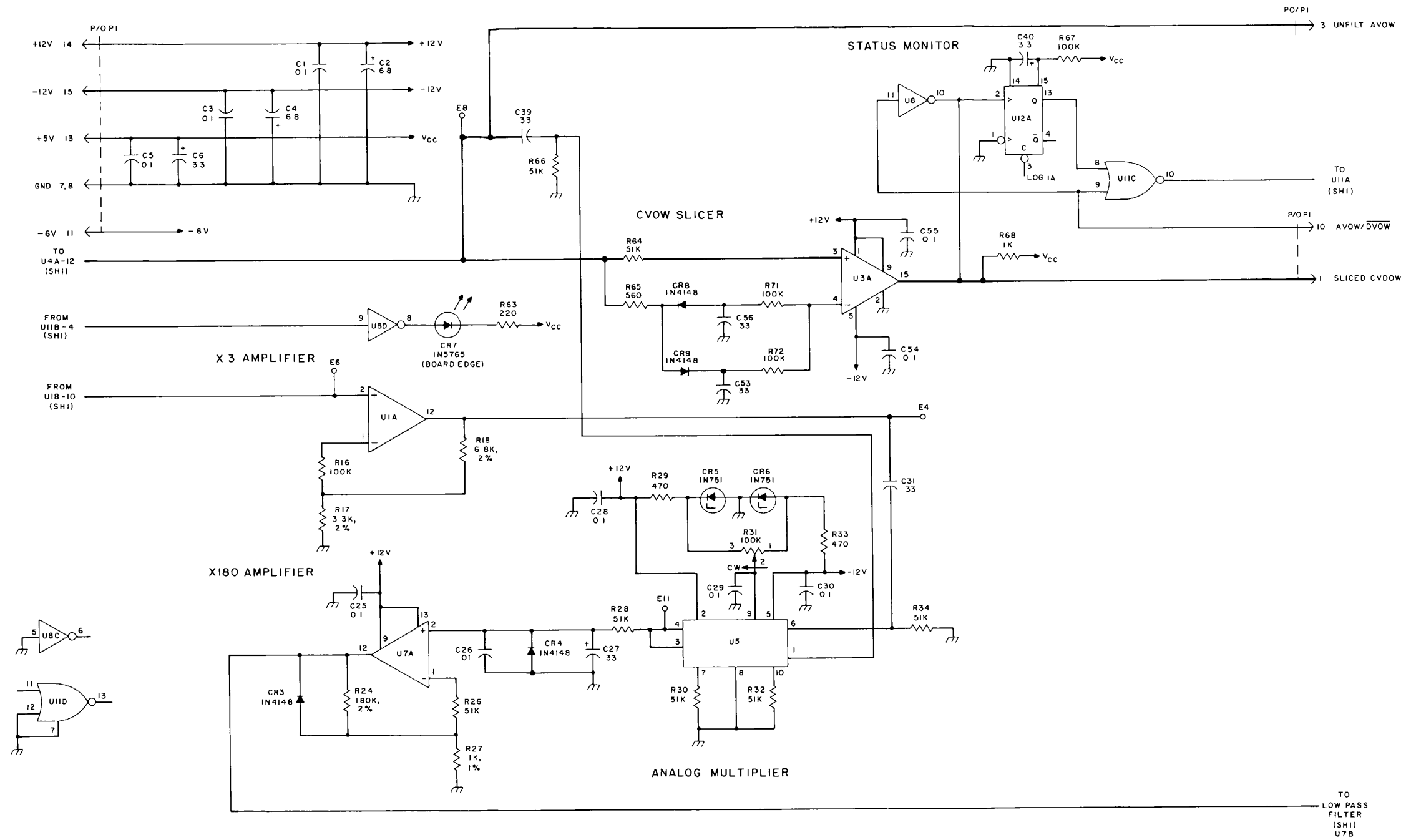


Figure 5-38.1. Radio digital processor 1A12A16, schematic diagram, asynchronous mode.  
Change 2 5-90.1

NOTE  
 1 UNLESS OTHERWISE SPECIFIED CAPACITORS ARE IN MICROFARADS INDUCTORS ARE MICRONHENRIES RESISTORS ARE IN OHMS AND ARE 1/4 WATT, 5 PERCENT  
 2 PARTIAL REFERENCE DESIGNATION ARE SHOWN FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION  
 3 POWER CONNECTIONS FOR INTEGRATED DIGITAL CIRCUITS ARE SHOWN IN THE TABLE BELOW DEVICE TYPE NUMBERS AND ILLUSTRATIONS ARE SHOWN IN FIGURE 5-24.1

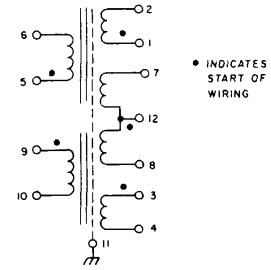
LOC	DEVICE	V <sub>CC</sub>	GND
U1, U4, U7	747	-	-
U2	LM118D		
U3	LM2111		
U5	4213		
U6	MD6001	-	-
U8	06	14	7
U9	LH0032		
U10	AM686		
U11	LS02	14	7
U12	LS123	14	7



EL1B139

Figure 5-38.10(2). Regenerator, digital 1A12A8, schematic diagram (sheet 2 of 2).  
 Change 6 5-89.35

- NOTES
- PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER & SUBASSEMBLY DESIGNATION
  - ALL WIRE IS NO 24 AWG STRANDED, TEFLON INSULATED, EXCEPT W1 & W2
  - CONNECTORS ON A1 THRU A5 ARE ETCHED CONTACTS ON PRINTED WIRING BOARD
  - ALL RESISTOR VALUES ARE IN OHMS
  - SCHEMATIC FOR HYBRID TRANSFORMER 1A13A77B11 IS SHOWN BELOW



\* INDICATES START OF WIRING

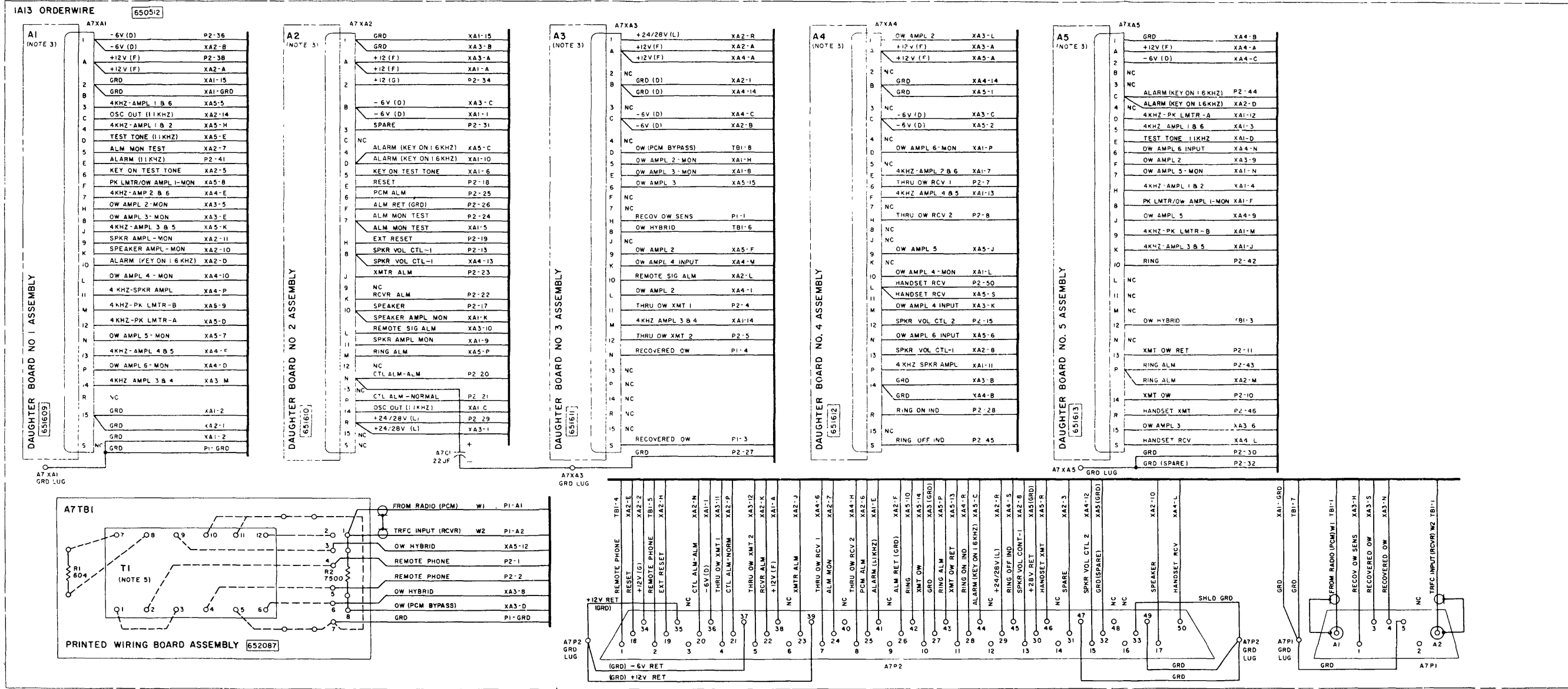


Figure 5-39. Orderwire assembly 1A13, interconnecting diagram.

NOTES

- 1 UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS CAPACITANCES ARE IN MICROFARADS
- 2 INDICATES MARKING ON EQUIPMENT
- 3 TERMINALS E1 THROUGH E45, ARE MOUNTED ON PRINTED WIRING BOARD, 1A13A1B1
- 4 PARTIAL REFERENCE DESIGNATION SHOWN PREFIX REFERENCE DESIGNATIONS WITH 1A13A1
- 5 LIGHT SWITCH ASSEMBLY S2 IS A SEALED UNIT (PART NO SM-9-650B2-1) AND CONTAINS A PRESS-TO-TEST SWITCH AND A LAMP DRIVER FOR MODULAR TEST INDICATOR DSL
- 6 SWITCH S1 IS VIEWED FROM END NEAREST CONTROL KNOBS AND SHOWN IN POSITION 1 SECTION A IS CLOSEST TO KNOB

SWITCH MONITOR FUNCTIONS

SW POS	FUNCTION	BOARD	I C CRT
1	NORMAL (4KHZ OSC MON)	A1	4 02 OSC
2	AMPLIFIER 1	A5	A5
3	AMPLIFIER 2	A3	A2
4	AMPLIFIER 3	A3	A1
5	AMPLIFIER 4	A4	A1
6	AMPLIFIER 5	A5	A4
7	AMPLIFIER 6	A4	A2
8	PEAK LIMITER	A5	A2 A3
9	SPEAKER AMPL	A2	A2
10	OSC. AF (SIDETONE)	A5	1.6 OSC
11	OSC. AF	A2	1.6 OSC
12	AUDIBLE ALM MON	A2	A1

7 IN THE LOGIC SYMBOL, THE NUMBER BELOW THE REFERENCE DESIGNATOR IS THE TYPE DESIGNATOR

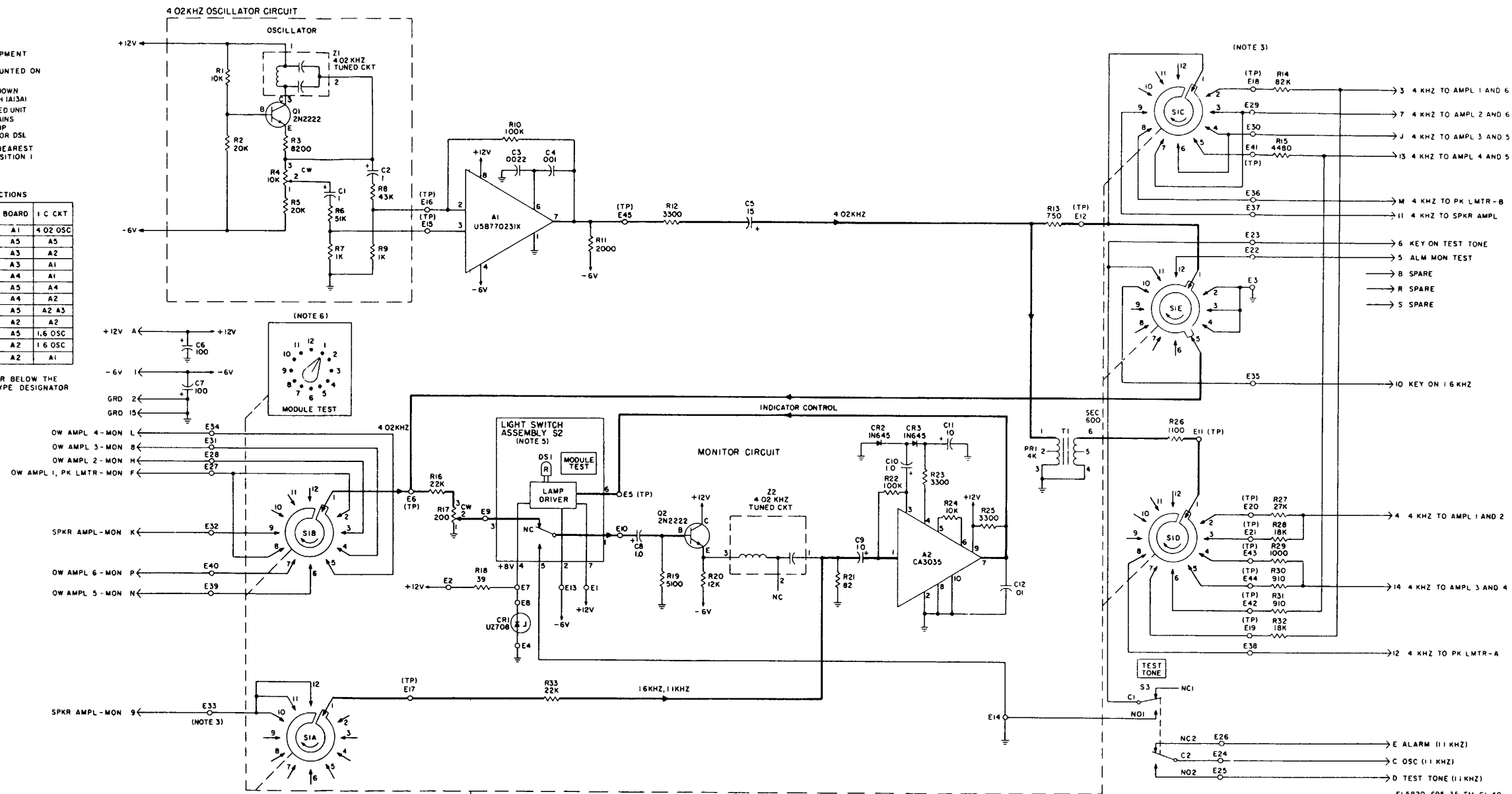


Figure 5-40. Daughter board No.1 assembly 1A13A1, schematic diagram.  
Change 1 5-93

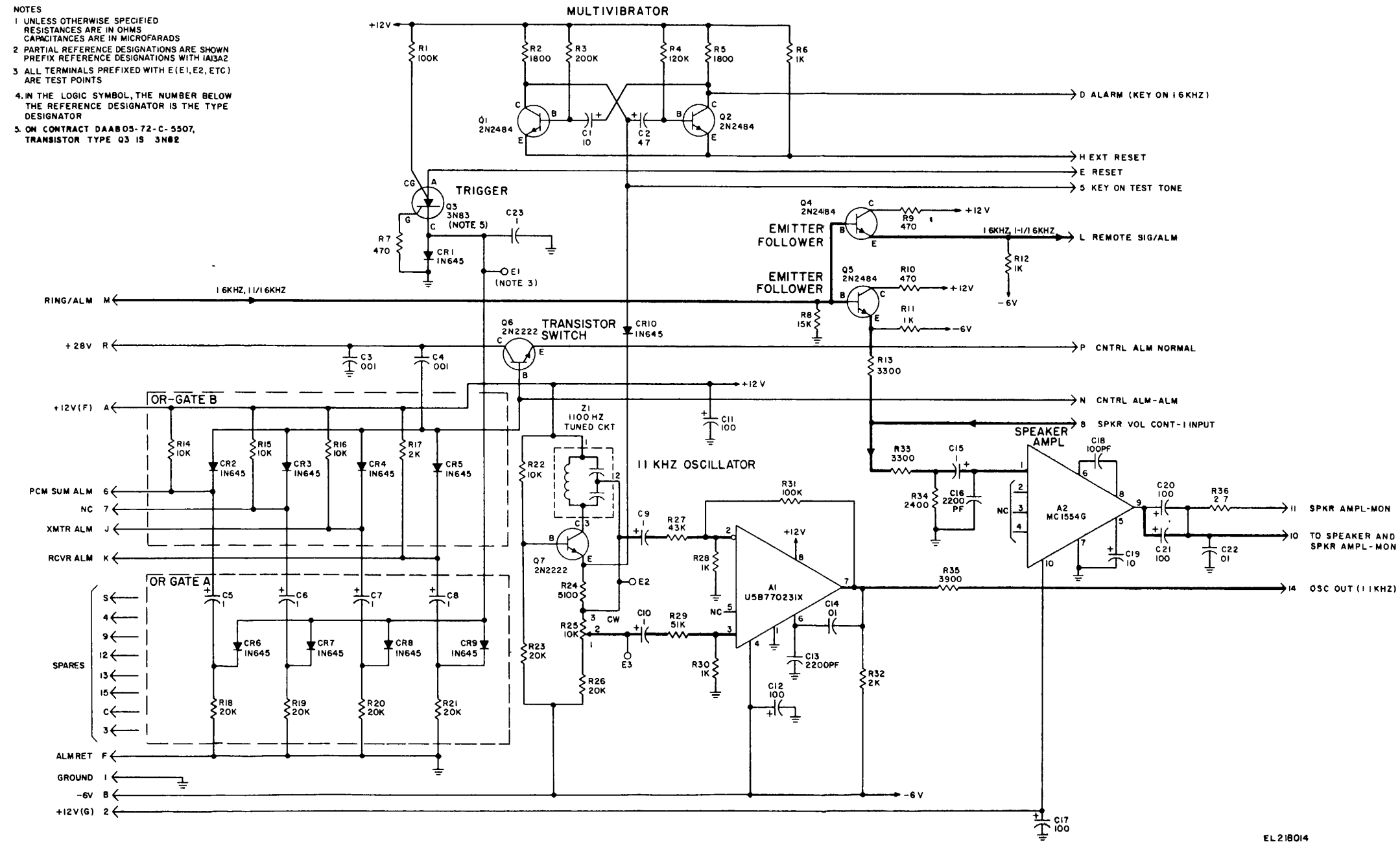
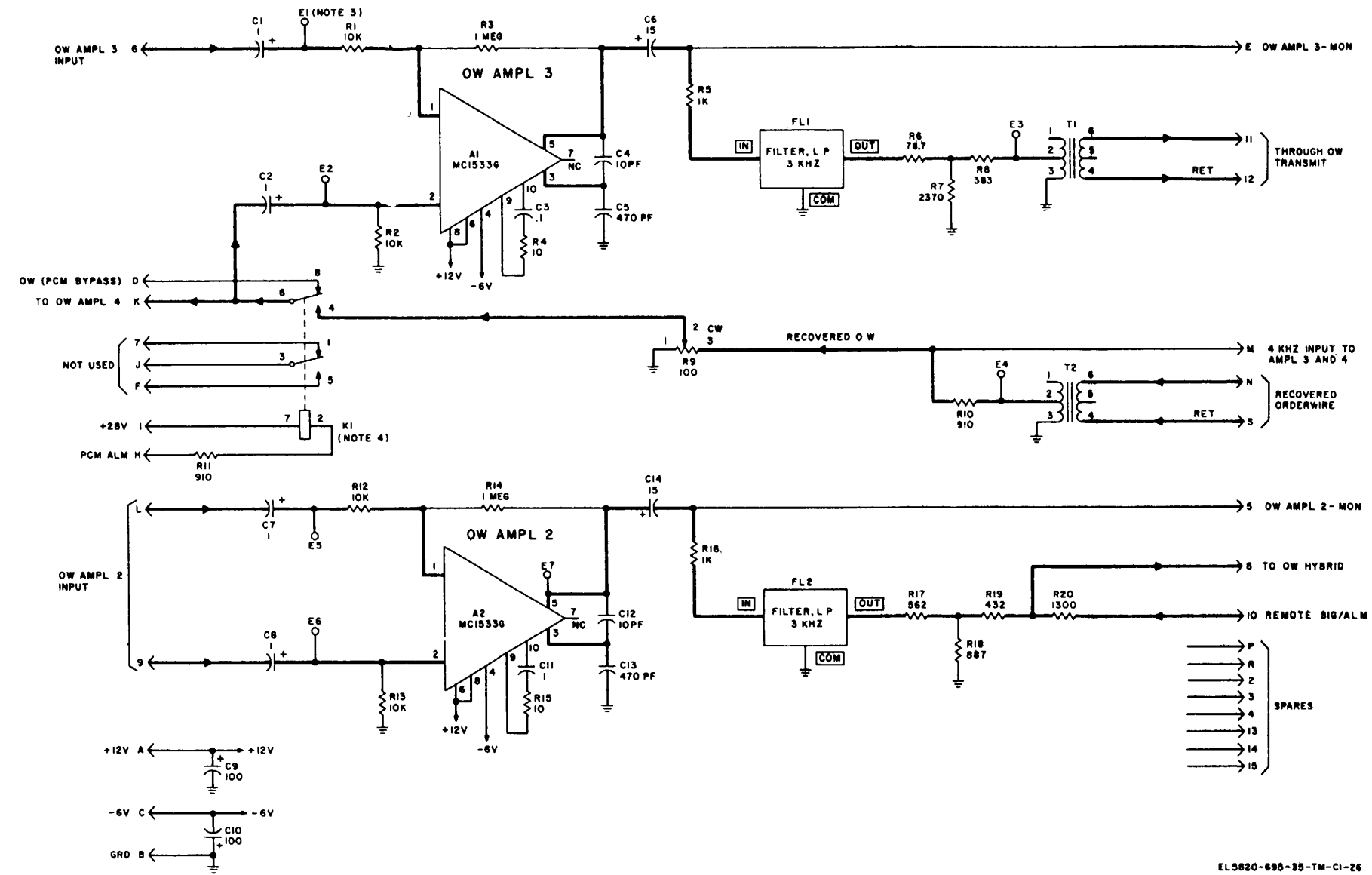


Figure 5-41. Daughter board No. 2 assembly 1A13A2, schematic diagram.

- NOTES:
1. UNLESS OTHERWISE SPECIFIED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS.
  2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN PREFIX REFERENCE DESIGNATIONS WITH IA3A3.
  3. ALL TERMINALS PREFIXED WITH E (E1, E2, ETC.) ARE TEST POINTS.
  4. RELAY K1 SHOWN IN DE-ENERGIZED POSITION.
  5. IN THE LOGIC SYMBOL, THE NUMBER BELOW THE REFERENCE DESIGNATOR IS THE TYPE DESIGNATOR.



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Figure 5-42. Daughter board No. 3 assembly 1A1A3A3, schematic diagram.  
Change 1 5-97

- NOTES:  
 1. UNLESS OTHERWISE SPECIFIED:  
 RESISTANCES ARE IN OHMS,  
 CAPACITANCES MICROFARADS.  
 2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN  
 PREFIX REFERENCE DESIGNATIONS WITH 1A13A4.  
 3. ALL TERMINALS PREFIXED WITH E (E1, E2, ETC)  
 ARE TEST POINTS.  
 4. RELAY K1 SHOWN IN DE-ENERGIZED POSITION.  
 5. IN THE LOGIC SYMBOL, THE NUMBER BELOW  
 THE REFERENCE DESIGNATOR IS THE TYPE  
 DESIGNATOR.  
 6. ON CONTRACT DAAB05-72-C-5507, R15 AND R17  
 ARE 649 OHMS, R16 IS 442 OHMS, AND R27  
 IS 100,000 OHMS.

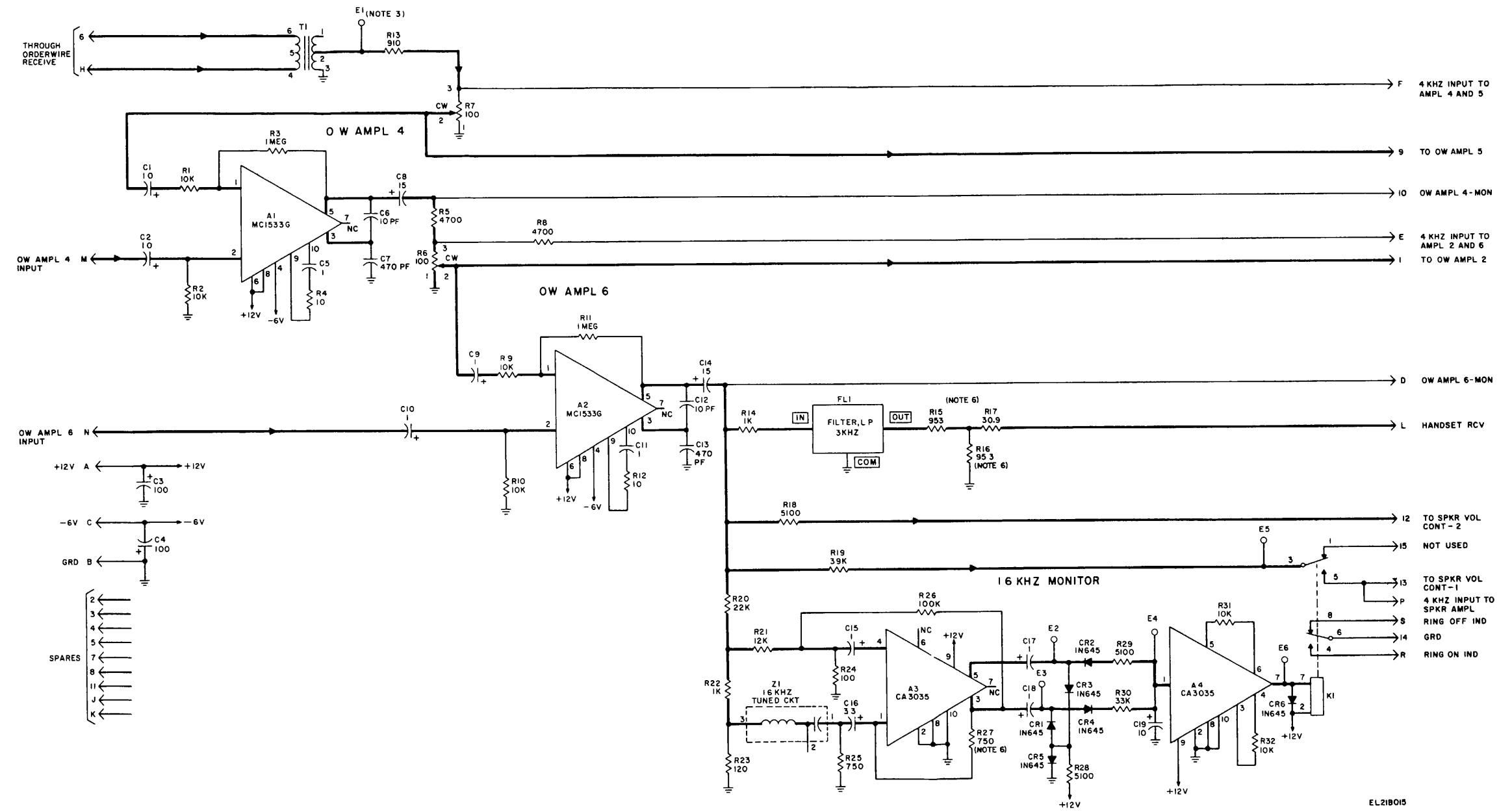
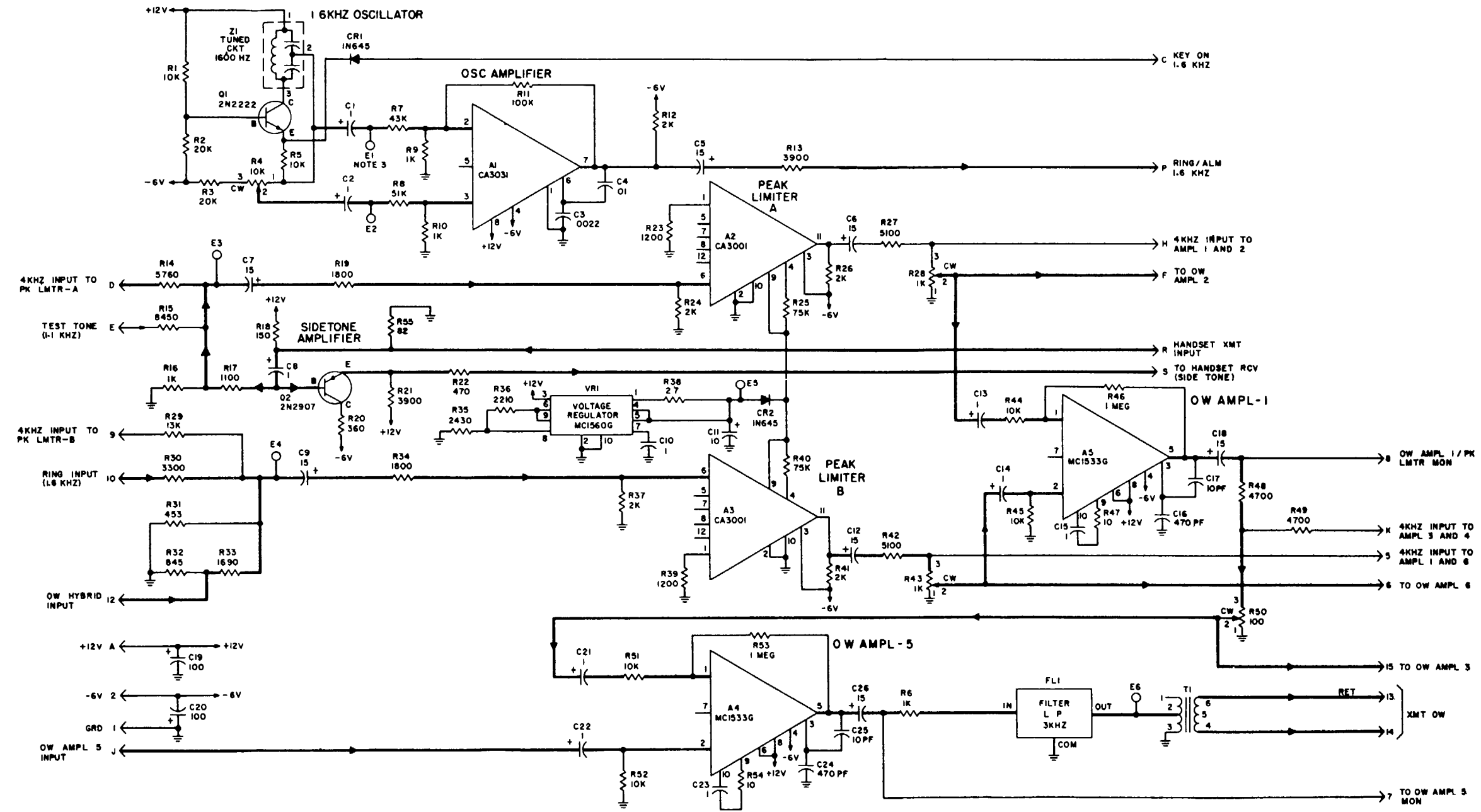


Figure 5-43. Daughter board No. 4 assembly 1A13A4, schematic diagram.

EL21B015




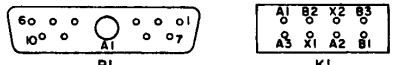
- NOTES:  
 1. UNLESS OTHERWISE SPECIFIED:  
 RESISTANCES ARE IN OHMS.  
 CAPACITANCES ARE IN MICROFARADS.  
 2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN:  
 PREFIX REFERENCE DESIGNATIONS WITH IAJ3AS.  
 3. ALL TERMINALS PREFIXED WITH E (E1, E2, ETC.)  
 ARE TEST POINTS.



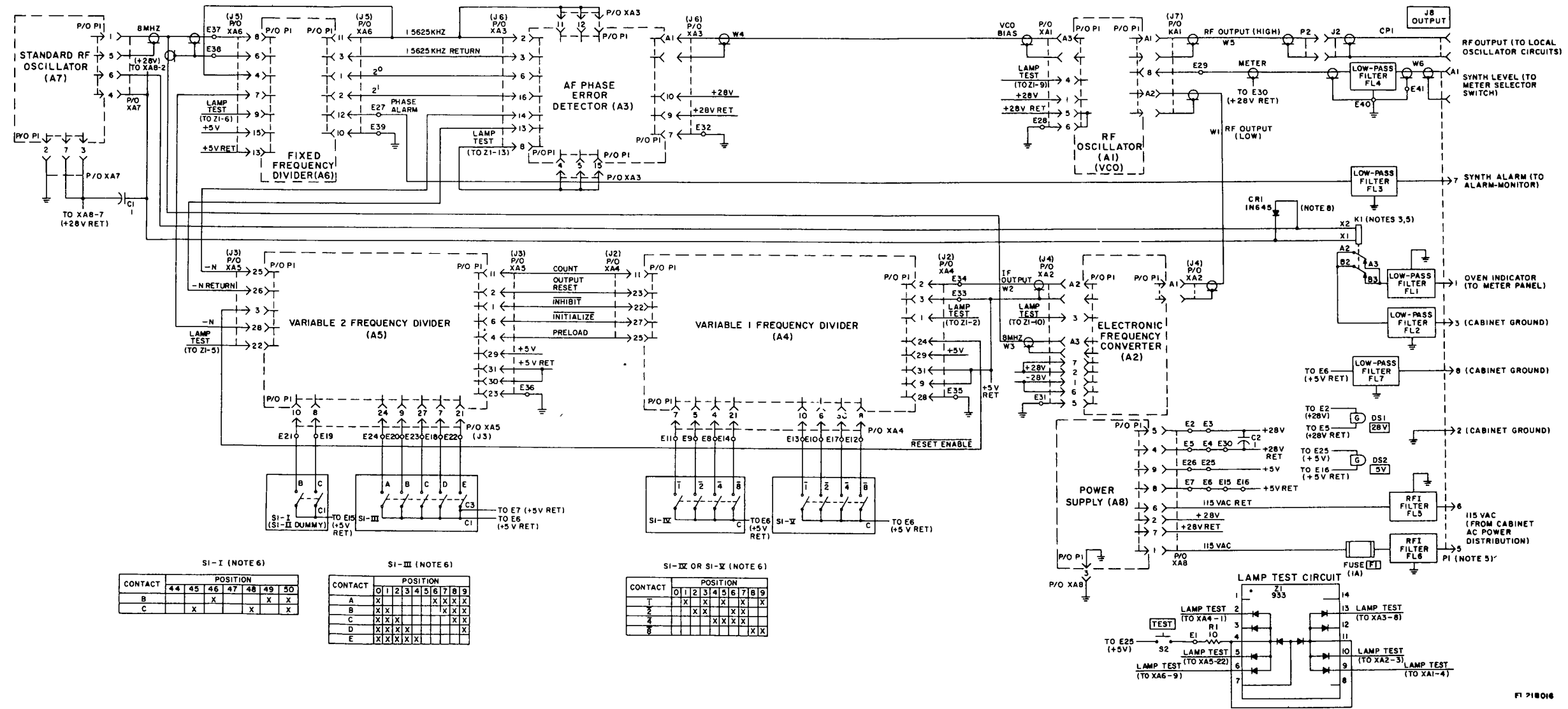
EL5820-695-35-TM-C1-28

Figure 5-44. Daughter board No. 5 assembly 1A13A5, schematic diagram.  
 Change 1 5-101

NOTES:

1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A14 (T-1054/GRC-144) OR 2A14 (R-1467/GRC-144).
2. UNLESS OTHERWISE INDICATED: RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS.
3. RELAY KI IS SHOWN IN DE-ENERGIZED POSITION.
4.  INDICATES EQUIPMENT MARKING.
5. PI AND KI PIN ORIENTATIONS ARE SHOWN BELOW:  


REAR VIEW      BOTTOM VIEW
6. THE CLOSED SWITCH (SI) CONTACTS (INDICATED BY AN X) AND ASSOCIATED SWITCH POSITIONS ARE SHOWN BELOW EACH SWITCH SECTION (SI-I, II, III, IV AND V).
7. TERMINALS E1 THROUGH E40, RESISTOR R1, CAPACITOR C2, INTEGRATED CIRCUIT Z1, AND CONNECTORS XA1 THROUGH XA6 ARE MOUNTED ON PRINTED WIRING BOARD ASSEMBLY 1A14A9/2A14A9.
8. CONNECTOR DESIGNATIONS IN PARENTHESES ARE APPLICABLE TO CONTRACT DAAB05-72-C-5507. DIODE CRI IS ADDED ON CONTRACT DAAB05-72-C-5507.



SI-I (NOTE 6)	
CONTACT	POSITION
B	X
C	X

SI-III (NOTE 6)	
CONTACT	POSITION
A	X
B	X
C	X
D	X
E	X

SI-IV OR SI-V (NOTE 6)	
CONTACT	POSITION
1	X
2	X
4	X
8	X

Figure 5-45 (1). Electrical frequency synthesizer 1A14/2A14, interconnecting diagram (part 1 of 3).

**NOTES**  
 1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT, UNIT NUMBER AND SUBASSEMBLY DESIGNATION.  
 2. ALL WIRE IS NO 22 AWG, UNLESS SPECIFIED AS NO 22 AWG

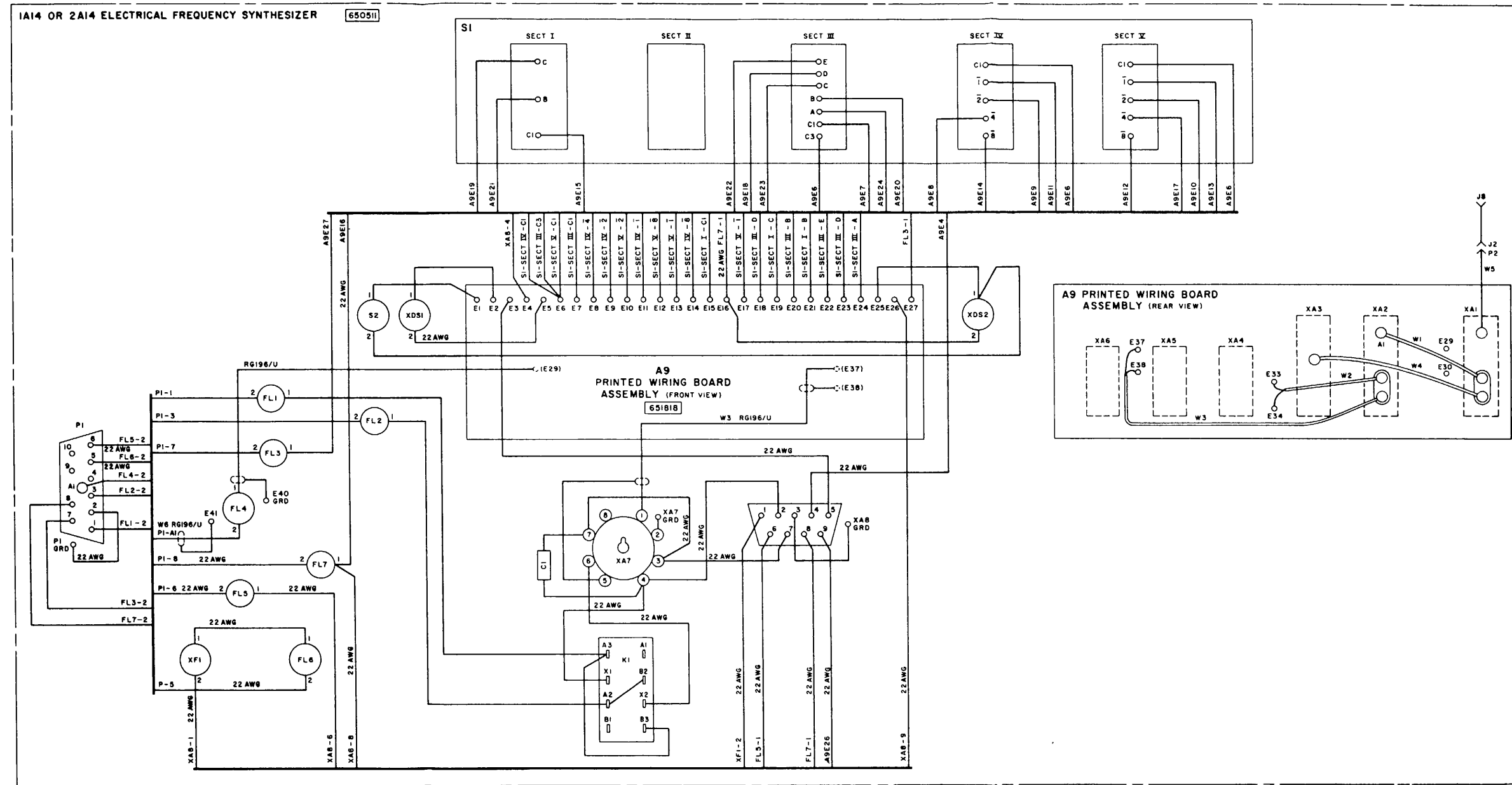
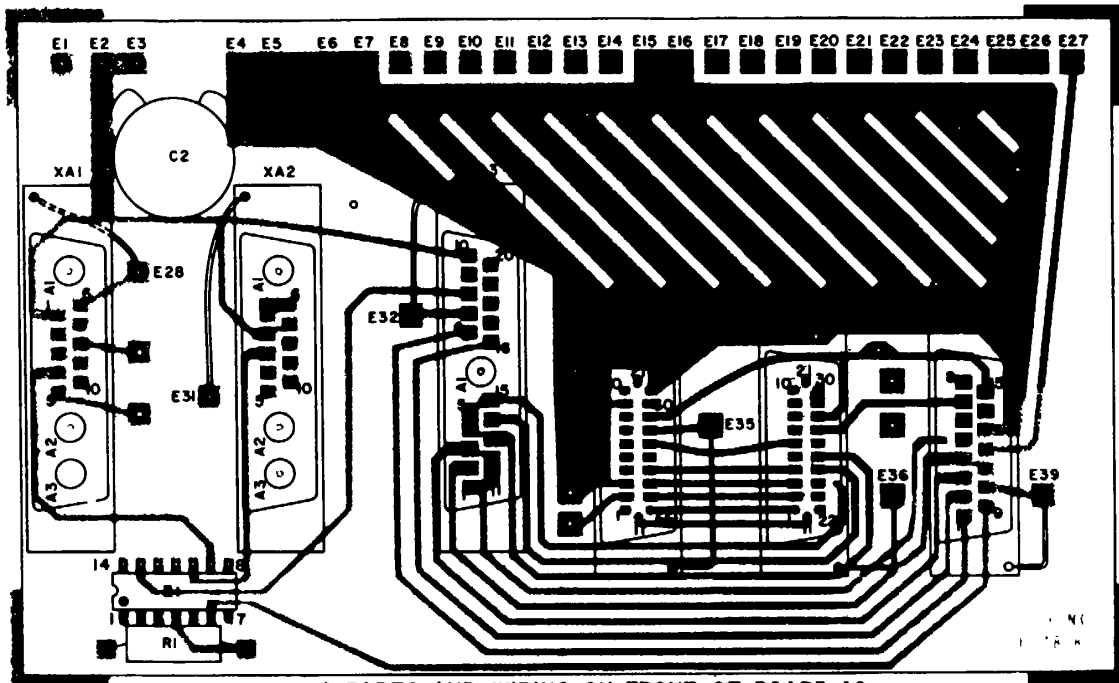
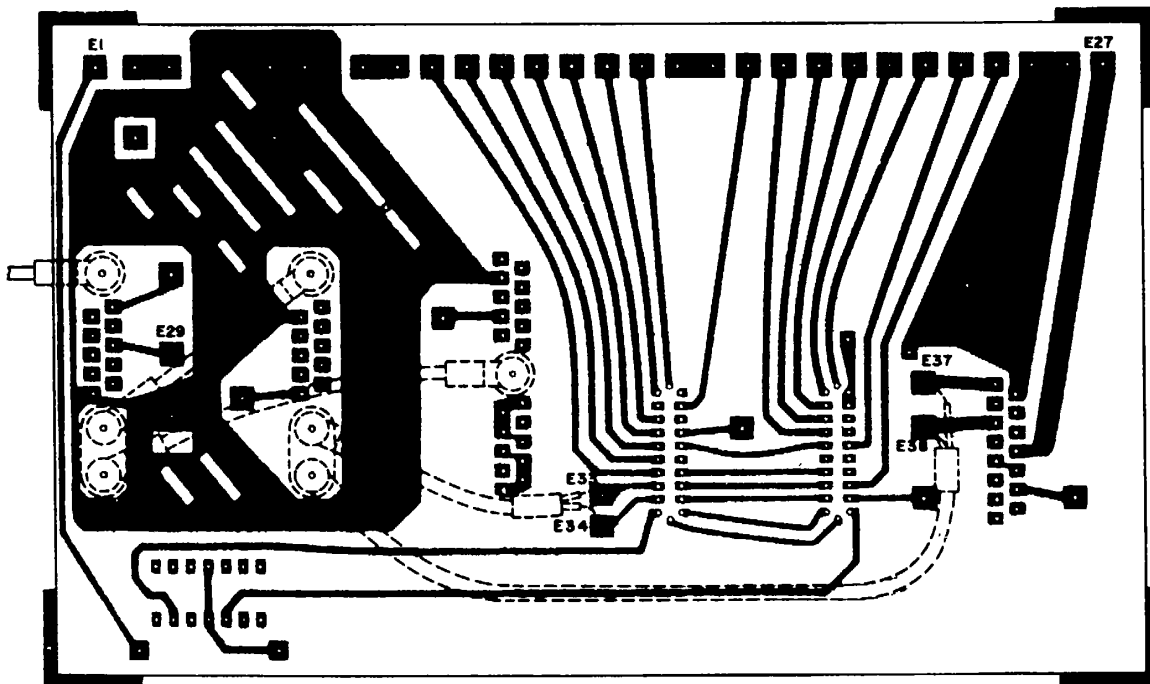


Figure 5-45 (2). Electrical frequency synthesizer 1A14/2A14, interconnecting diagram (part 2 of 3).  
 5-105



A. PARTS AND WIRING ON FRONT OF BOARD A9.



B. WIRING ON BACK OF BOARD A9-  
(VIEWED THROUGH FRONT)

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Figure 5-45(3). Electrical frequency synthesizer 1A14/2A14, interconnecting diagram (part 3 of 3).

- NOTES:
- UNLESS OTHERWISE INDICATED, RESISTORS ARE IN OHMS, CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE INDICATED.
  - PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH IN-44 (7-155A/B/C-144) OR 2A14A1(R-1447/B/C-144).
  - VALUES FOR RESISTORS R20 AND R23 ARE DETERMINED DURING FINAL TESTS.
  - SPARE TERMINALS P-2, P-3, P-7, P-9 AND P-10.

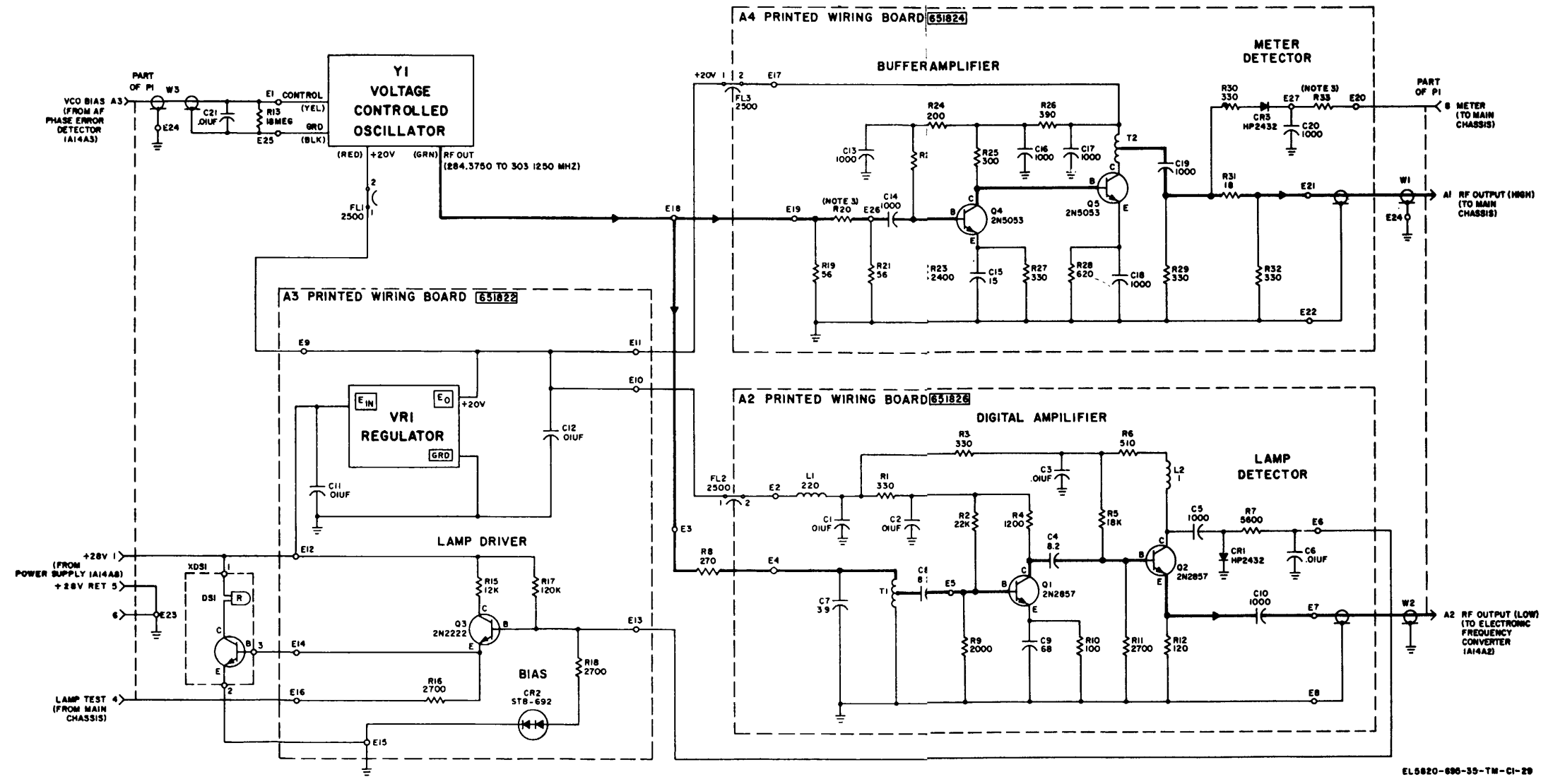


Figure 5-46. Radio frequency oscillator 1A14A1/2A14A1, schematic diagram.  
Change 1 5-109

NOTES

- 1 UNLESS OTHERWISE INDICATED RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS, INDUCTANCES ARE IN MICROHENRIES.
- 2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH 1A14A2 (T-1054/GRC-144) OR 2A14A2 (R-1467/GRC-144).
- 3 VALUE FOR RESISTOR R22 IS DETERMINED DURING FINAL TEST.

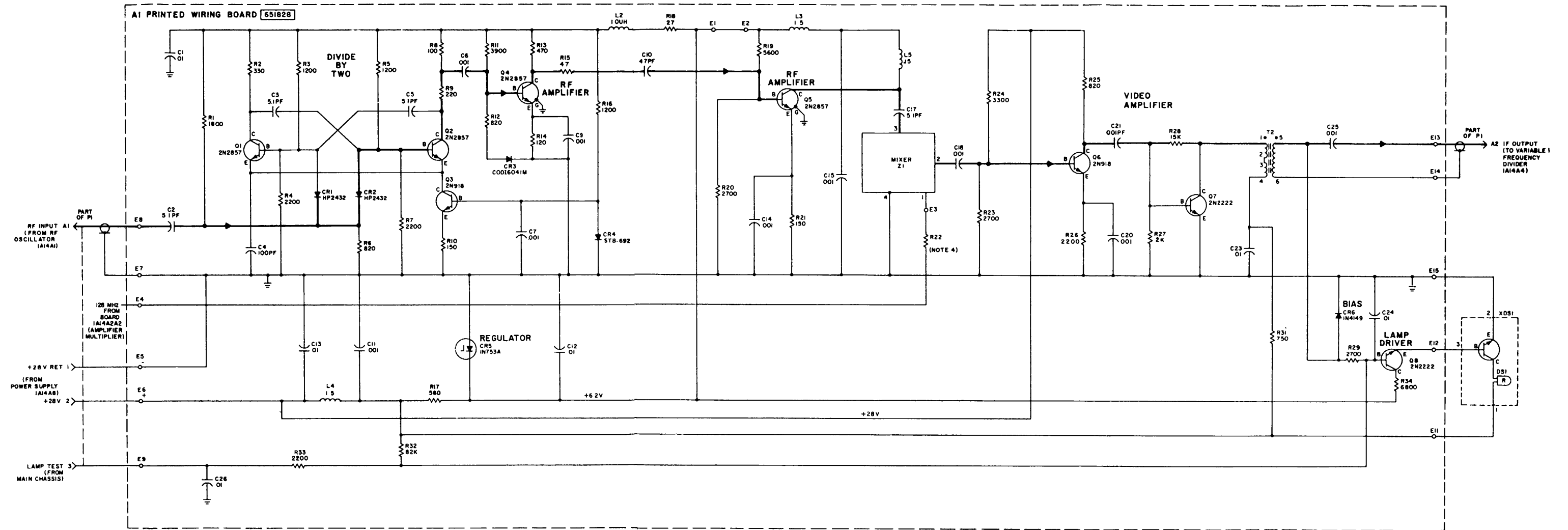


Figure 5-47. Electronic frequency converter board 1A14A2A1/2A14A2A1, schematic diagram.

Change 1 5-111

- NOTES  
 1 UNLESS OTHERWISE INDICATED  
 RESISTANCES ARE IN OHMS,  
 CAPACITANCES ARE IN MICROFARADS,  
 INDUCTANCES ARE IN MICROHENRIES  
 2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN  
 FOR COMPLETE DESIGNATION PREFIX WITH  
 1A14A2 (T-1054/GRC-144) OR 2A14A2 (R-1467/GRC-144)

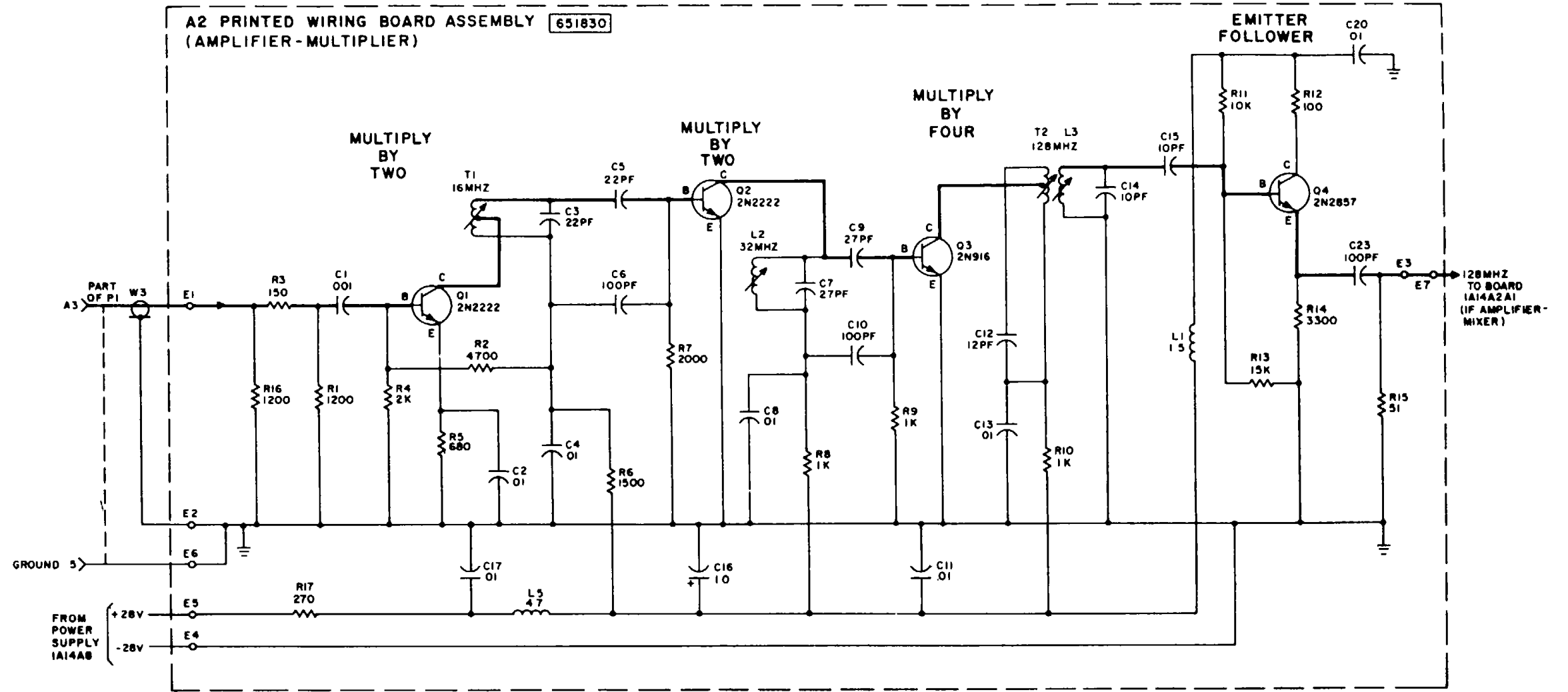
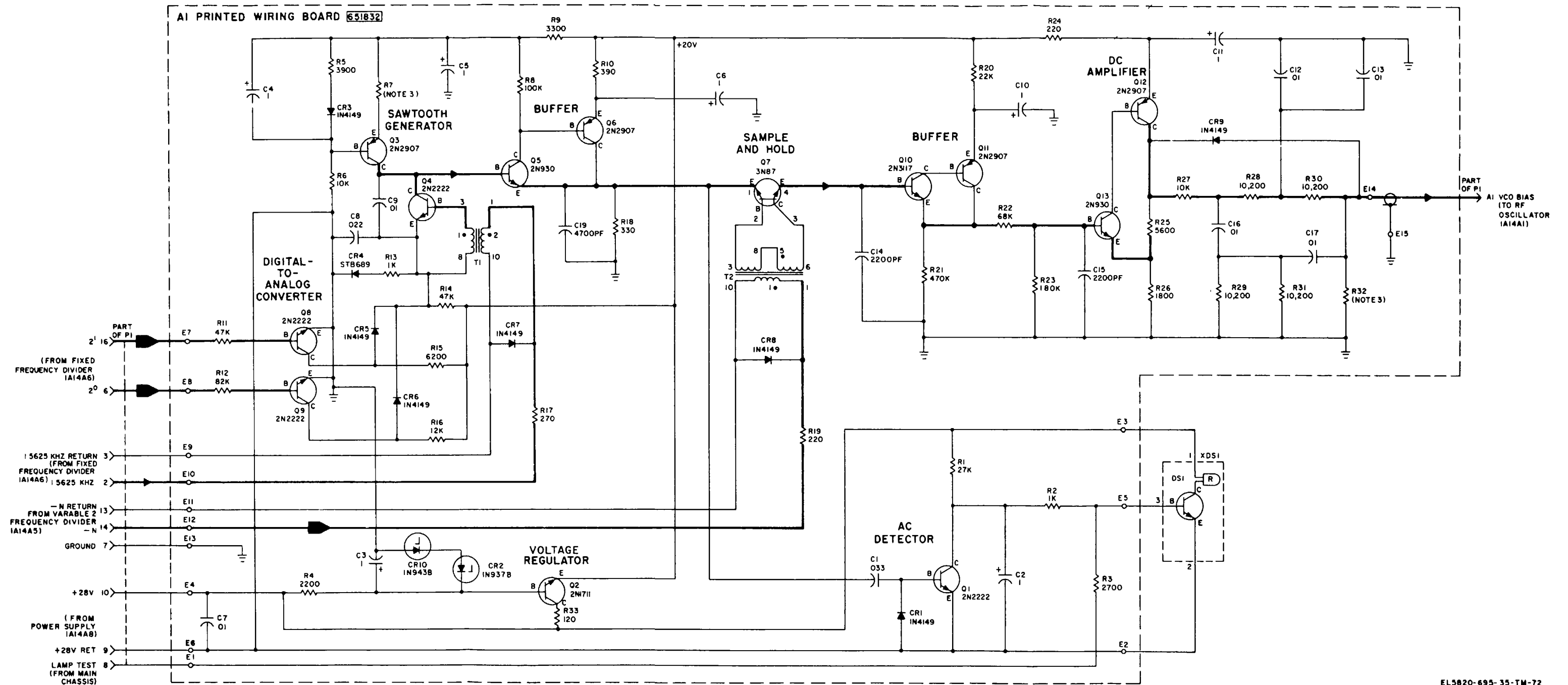
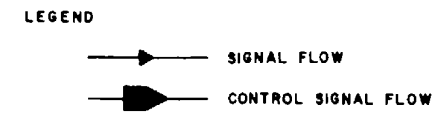


Figure 5-48. Electronic frequency converter board 1A14A2A2/2A14A2A2, schematic diagram.

- NOTES
- UNLESS OTHERWISE INDICATED RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS
  - PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH 1A14A3 (T-1054/GRC-144) OR 2A14A3 (R-1467/GRC-144)
  - VALUES FOR R7 AND R32 SELECTED AT TEST



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Figure 5-49. Audio frequency phase error detector 1A14A3/2A14A3 schematic diagram.



- NOTES
- UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS.
  - PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH 1A14A4 (T-1054/GRC-144) OR 2A14A4 (R-1467/GRC-144).
  - PIN 14 ON EACH INTEGRATED CIRCUIT IS CONNECTED TO +5 VOLTS, PIN 7 ON EACH INTEGRATED CIRCUIT IS CONNECTED TO -5 VOLTS.
  - INTEGRATED CIRCUIT TYPES ARE LISTED IN TABLE.

Z1	MSC6847L	Z10	MIC950-ID
Z2	SL50604	Z11	MIC963-ID
Z3	MIC932-ID	Z12	MIC950-ID
Z4	MIC963-ID	Z13	MIC950-ID
Z5	MSC6847L	Z14	SL50604
Z6	MSC6847L	Z15	MIC950-ID
Z7	MSC6847L	Z16	MIC949-ID
Z8	MIC950-ID	Z17	MIC950-ID
Z9	MIC949-ID	Z18	MIC950-ID

- IN THE LOGIC SYMBOL, THE NUMBER BELOW THE REFERENCE DESIGNATOR IS PART OF THE TYPE DESIGNATOR.
- ON CONTRACT DAAB05-72-C-5507, C1 IS 15 MF.

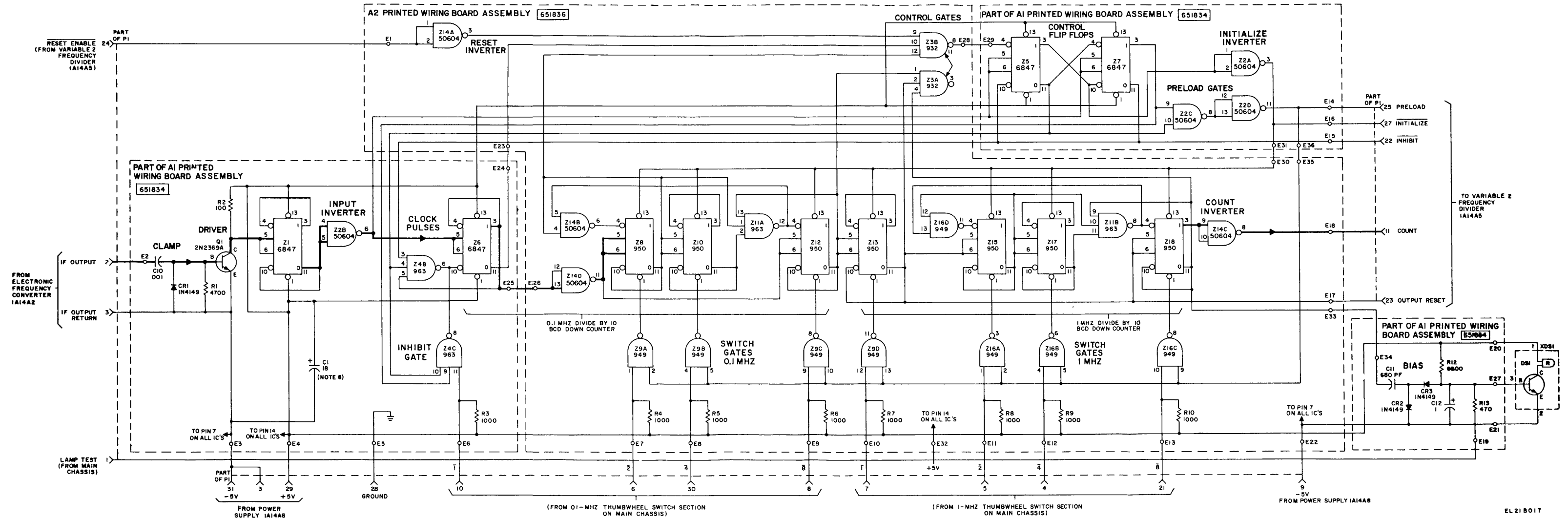


Figure 5-50. Variable 1 frequency divider 1A14A4A4/2A14A4, schematic diagram.

- NOTES
- UNLESS OTHERWISE INDICATED RESISTANCES ARE IN OHMS CAPACITANCES ARE IN MICROFARADS
  - PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH 1A14A5 (T-1054/GRC-144) OR 2A14A5 (R-1467/GRC-144)
  - PIN 14 ON EACH INTEGRATED CIRCUIT IS CONNECTED TO +5 VOLTS PIN 7 ON EACH INTEGRATED CIRCUIT IS CONNECTED TO GROUND
  - INTEGRATED CIRCUIT TYPES ARE LISTED IN TABLE
- |    |           |     |           |
|----|-----------|-----|-----------|
| Z1 | MIC932-ID | Z8  | MIC950-ID |
| Z2 | MIC950-ID | Z9  | MIC950-ID |
| Z3 | MIC950-ID | Z10 | MIC950-ID |
| Z4 | MIC950-ID | Z11 |           |
| Z5 | MIC950-ID | Z12 | MIC946-ID |
| Z6 | MIC950-ID | Z13 | MIC946-ID |
| Z7 | MIC950-ID | Z14 | MIC946-ID |
- IN THE LOGIC SYMBOL THE NUMBER BELOW THE REFERENCE DESIGNATOR IS PART OF THE TYPE DESIGNATOR
  - ON CONTRACT DAAB05-72-C-5507, C1 IS 15 MF

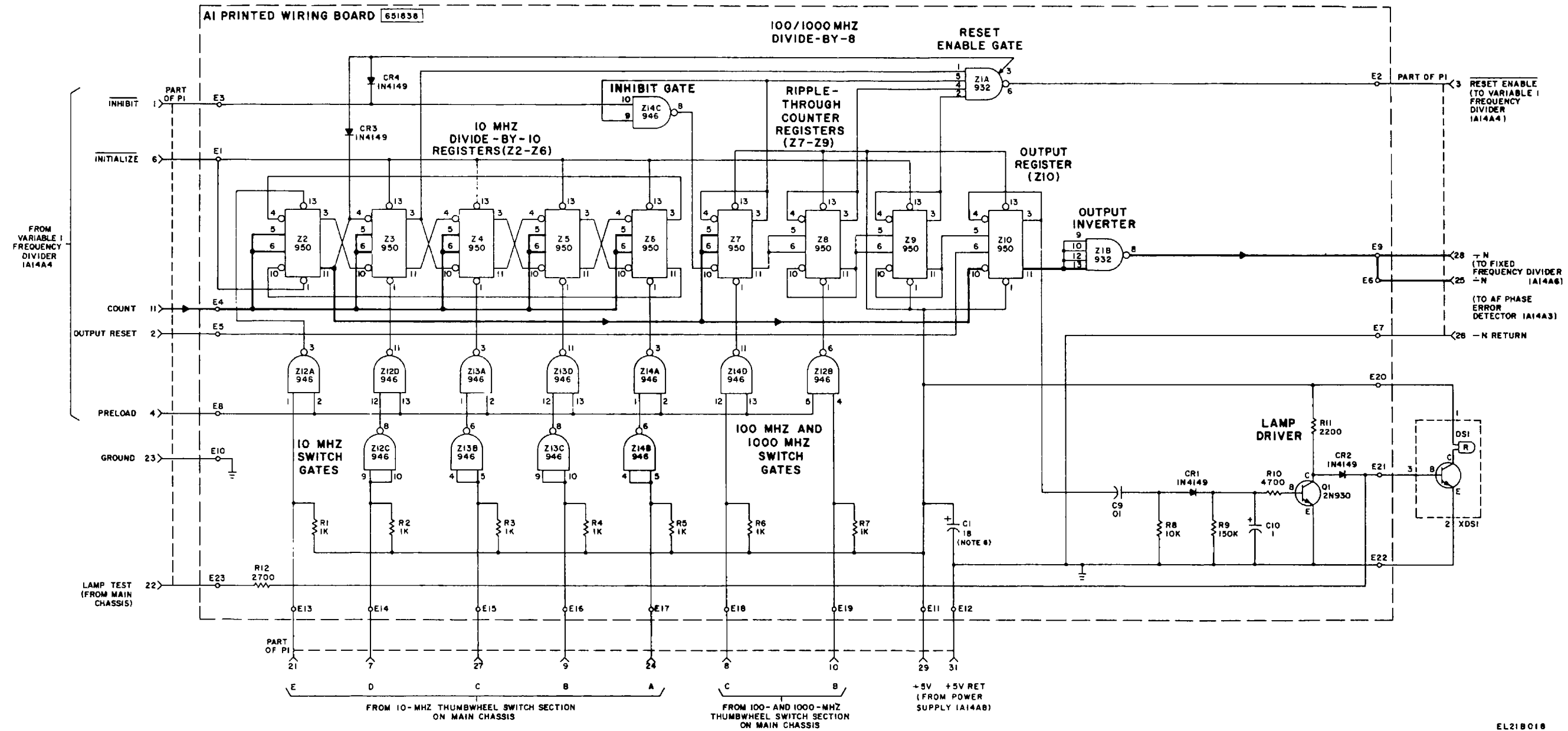
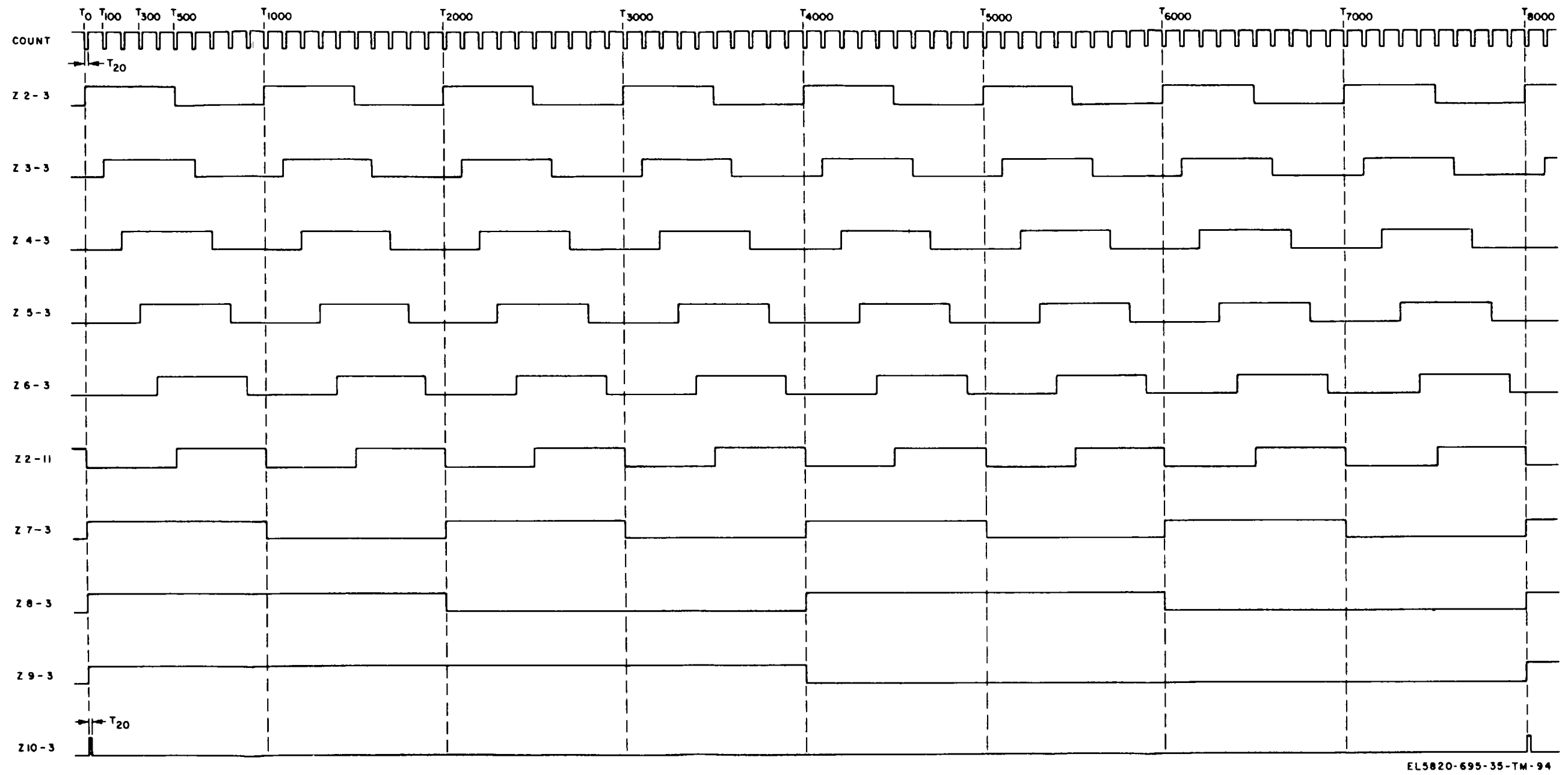


Figure 5-51. Variable 2 frequency divider 1A14A5/2A14A5, schematic diagram.



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Figure 5-52. Variable 2 frequency divider 1A14A5/2A14A5 timing during jump count.

- NOTES
- UNLESS OTHERWISE INDICATED RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS
  - PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH 1A14A6 (T-354/GRC-144) OR 2A14A6 (R-1467/GRC-144.)
  - PIN 14 ON EACH INTEGRATED CIRCUIT IS CONNECTED TO +5 VOLTS PIN 7 ON EACH INTEGRATED CIRCUIT IS CONNECTED TO GROUND
  - INTEGRATED CIRCUIT TYPES ARE LISTED IN TABLE.

Z1	MIC950-ID	Z13	MIC950-ID
Z2	MIC950-ID	Z14	MIC950-ID
Z3	MIC950-ID	Z15	UGA90025IX
Z4	MIC950-ID	Z16	MIC946-ID
Z5	MIC950-ID	Z17	MIC950-ID
Z6	MIC950-ID	Z18	MIC946-ID
Z7	MIC950-ID	Z19	MIC950-ID
Z8	MIC950-ID	Z20	MIC950-ID
Z9	MIC950-ID	Z21	MIC950-ID
Z10	MIC950-ID	Z22	MIC950-ID
Z11	MIC950-ID	Z23	MIC950-ID
Z12	MIC950-ID	Z24	MIC932-ID

- IN THE LOGIC SYMBOL, THE NUMBER BELOW THE REFERENCE DESIGNATOR IS PART OF THE TYPE DESIGNATOR.
- ON CONTRACT DAAB05-72-C-5507, C1 AND C3 ARE .15 MF

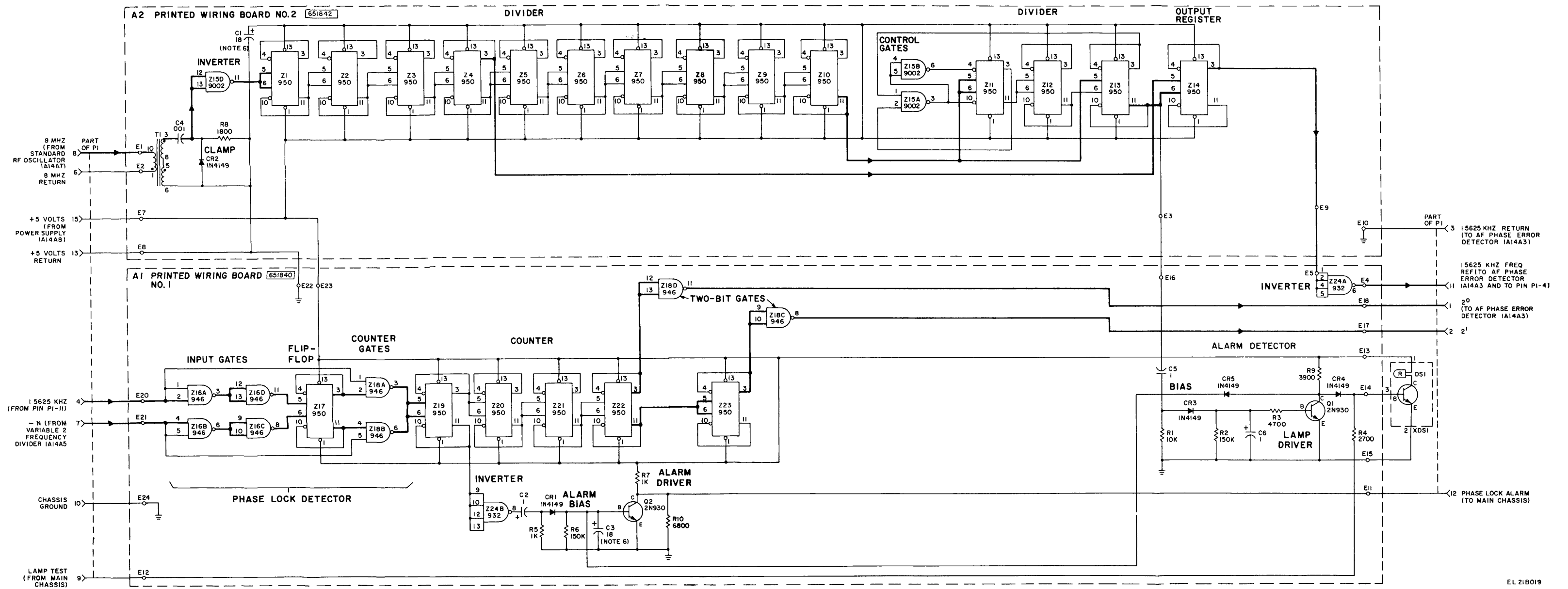


Figure 5-53. Fixed frequency divider 1A14A6/2A14A6, schematic diagram.

- NOTES**
- UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS CAPACITANCES ARE IN PICOFARADS INDUCTANCES ARE IN MICROHENRIES
  - PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, PREFIX REFERENCE DESIGNATIONS WITH 2A4
  - INDICATES MARKING ON EQUIPMENT.
  - ON CONTRACT DAAB05-72-C-5507, C43 IS O.B.-16 PF, C45 IS O.B.-11 PF, AND DIODES CR3 AND CR4 ARE TYPE IN 3600

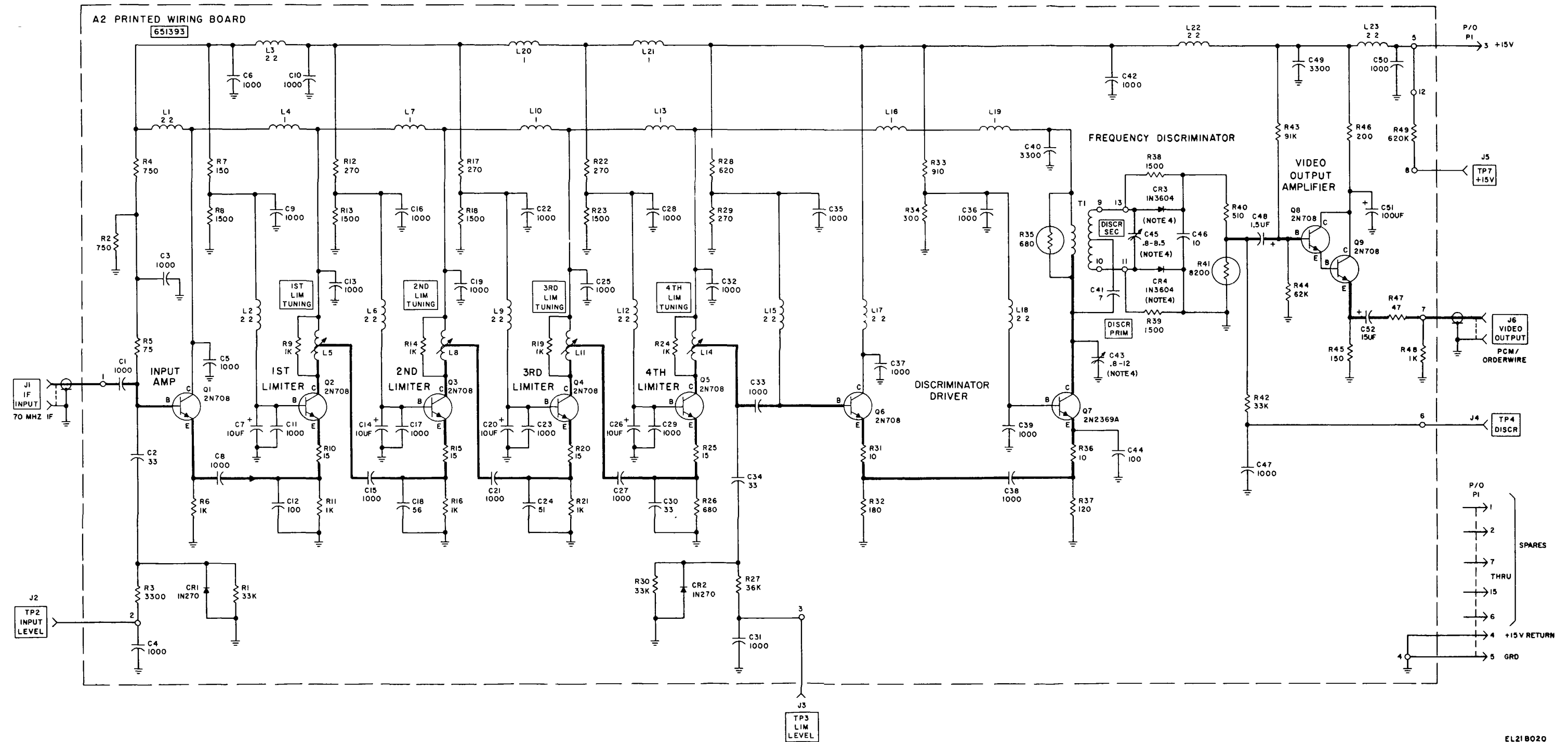


Figure 5-54. Demodulator 2A4, schematic diagram.

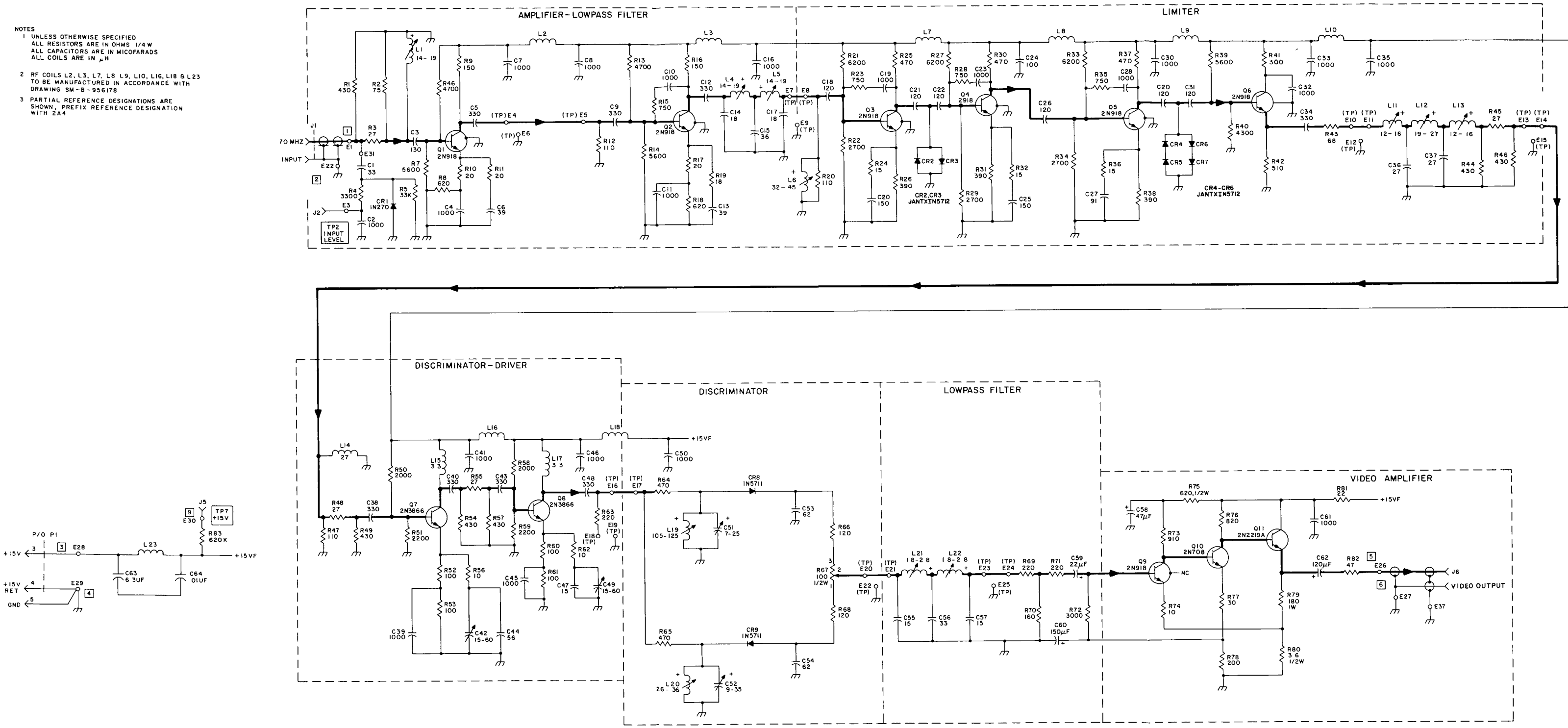


Figure 5-54.1. Demodulator 2A4 (956415), schematic diagram.

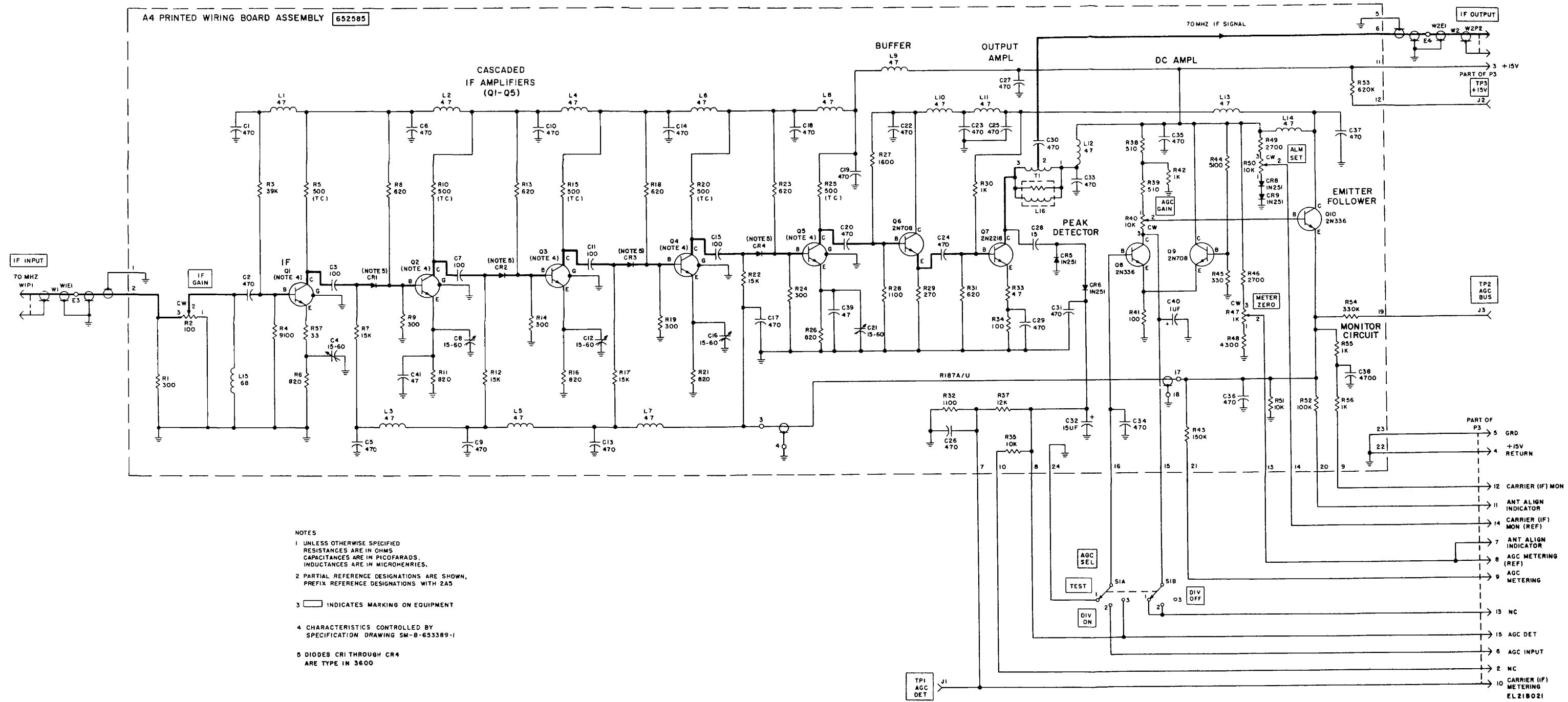


Figure 5-55. 70 MHz intermediate frequency amplifier 2A5, schematic diagram.

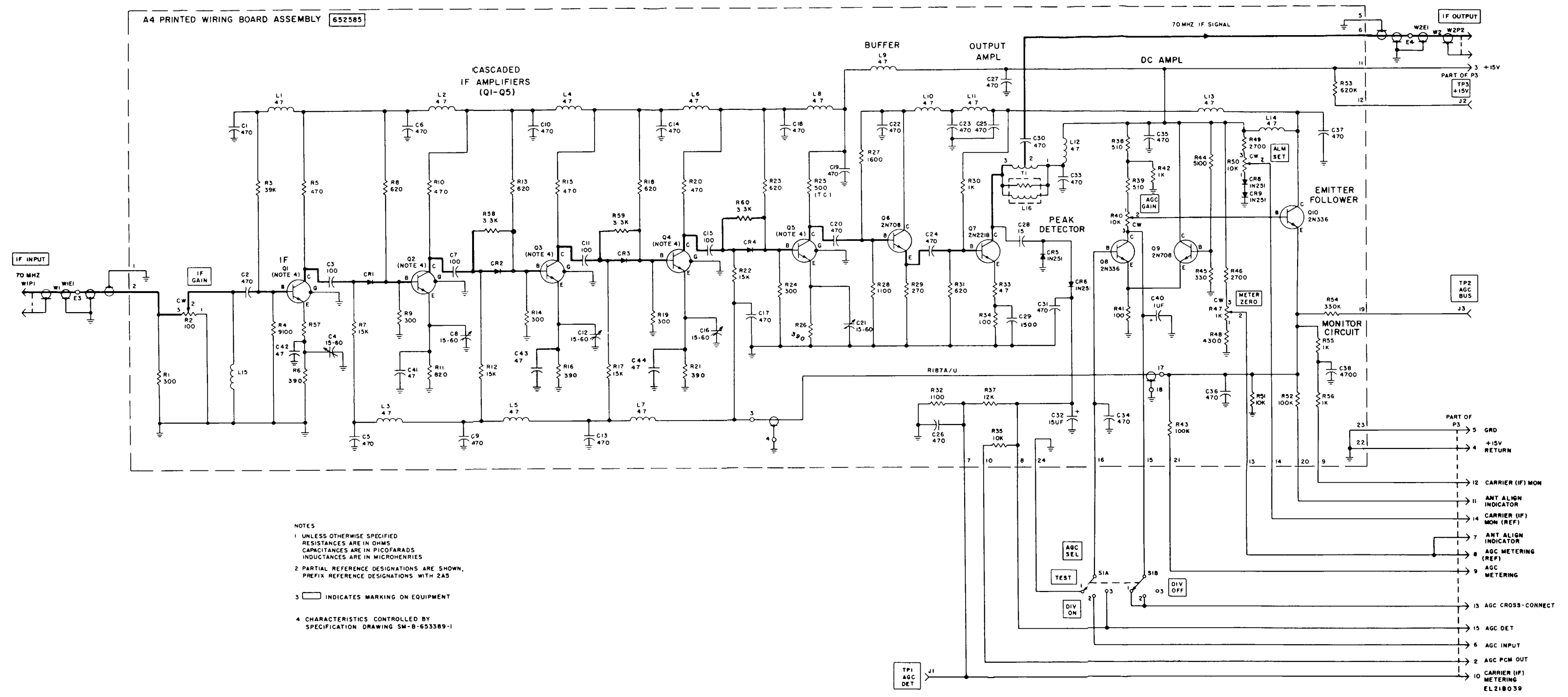


Figure 5-55.1. 70 MHz intermediate frequency amplifier 2A5 (956423), schematic diagram.

Change 6 5-127.1



- NOTES.
- 1 UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS CAPACITANCES ARE IN MICROHENRIES
  - 2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN PREFIX REFERENCE DESIGNATION WITH 2A8
  - 3    INDICATES MARKING ON EQUIPMENT

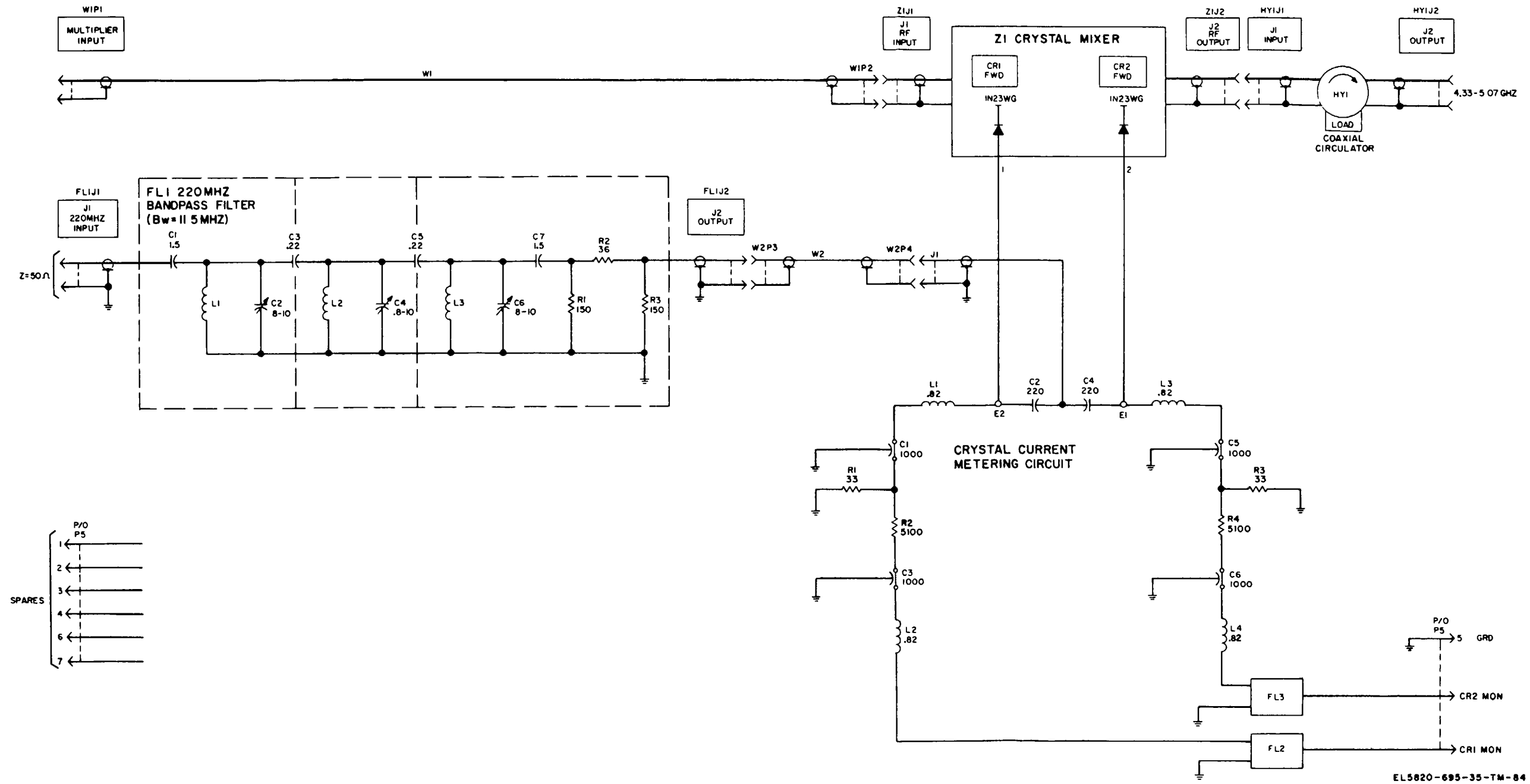


Figure 5-56. Receiver frequency mixer stage 2A8, schematic diagram.

NOTES

- 1 UNLESS OTHERWISE SPECIFIED  
RESISTANCES ARE IN OHMS  
CAPACITANCES ARE IN PICOFARADS
- 2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN  
FOR COMPLETE DESIGNATIONS, PREFIX WITH 2A10

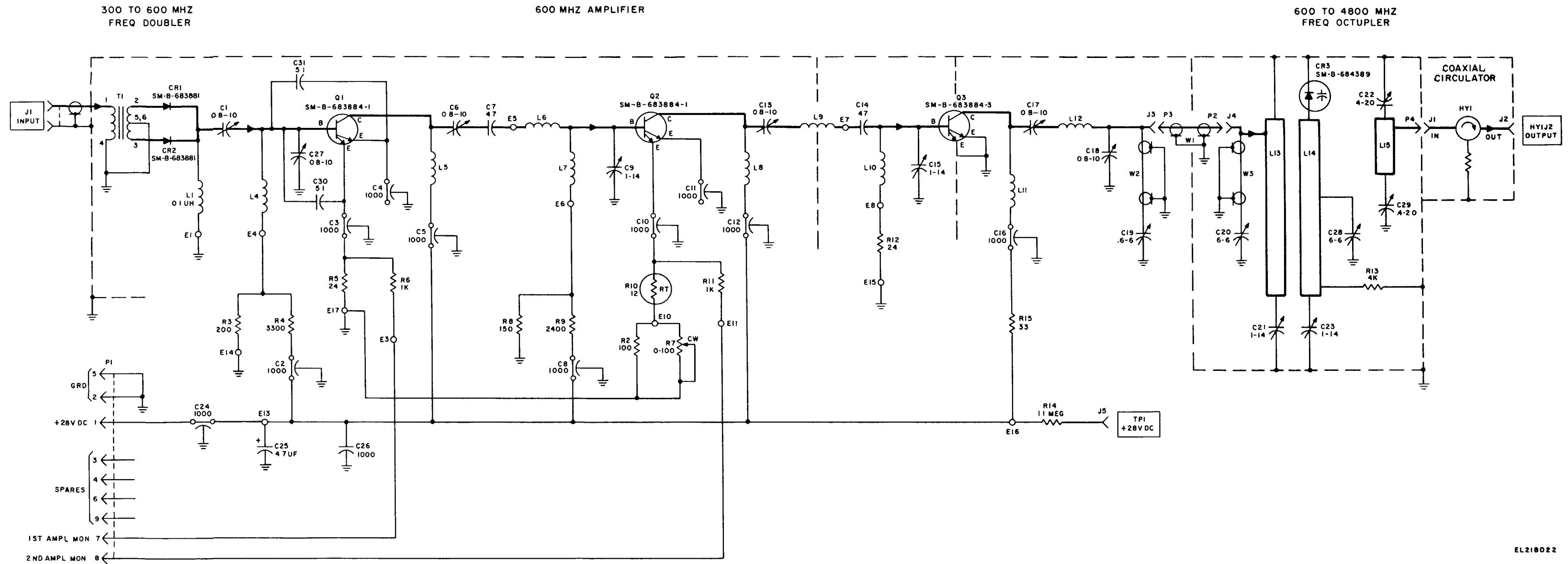


Figure 5-57. Amplifier-frequency multiplier 2A10, schematic diagram.

NOTES  
 1. UNLESS OTHERWISE SPECIFIED:  
 RESISTANCES ARE IN OHMS  
 CAPACITANCES ARE IN PICOFARADS  
 INDUCTANCES ARE IN MICROHENRIES  
 2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN  
 PREFIX REFERENCE DESIGNATIONS WITH 2A13.  
 3.    INDICATES MARKING ON EQUIPMENT

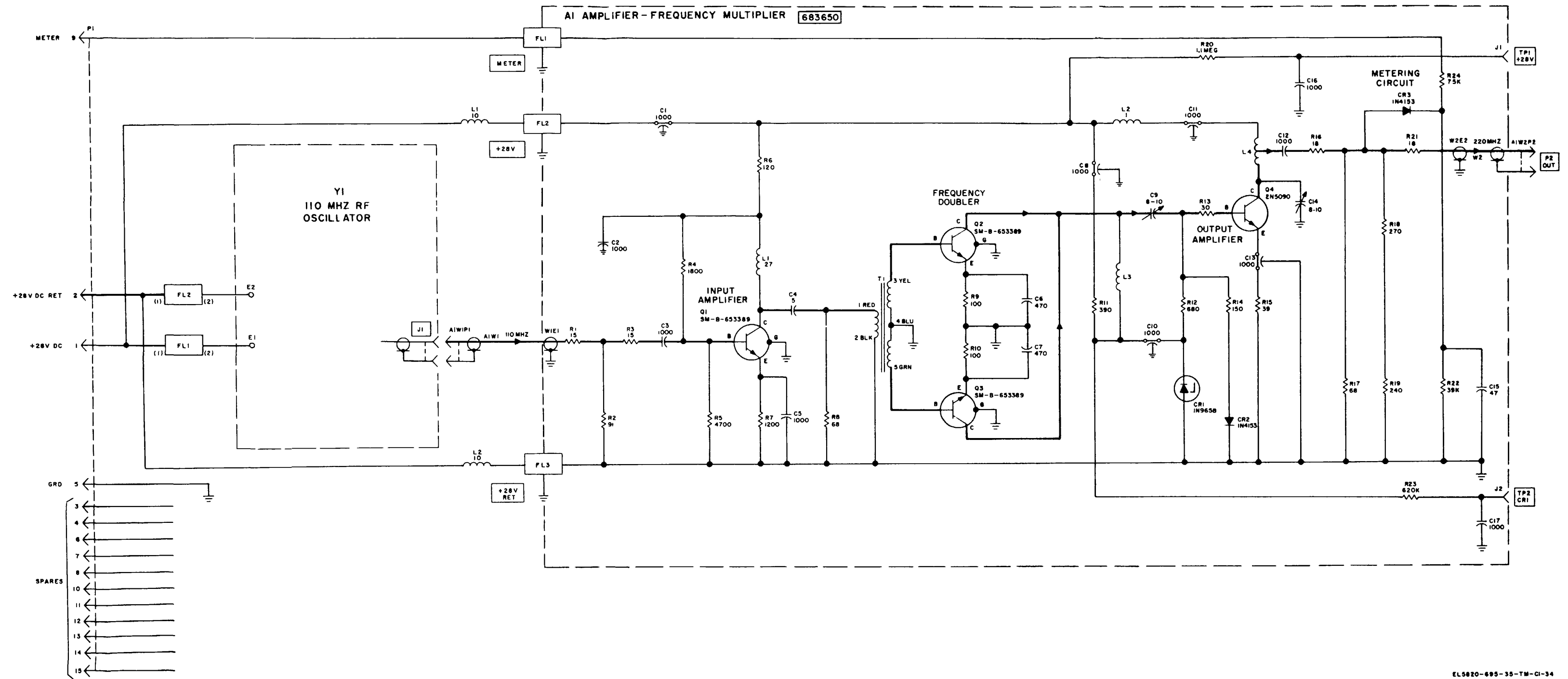
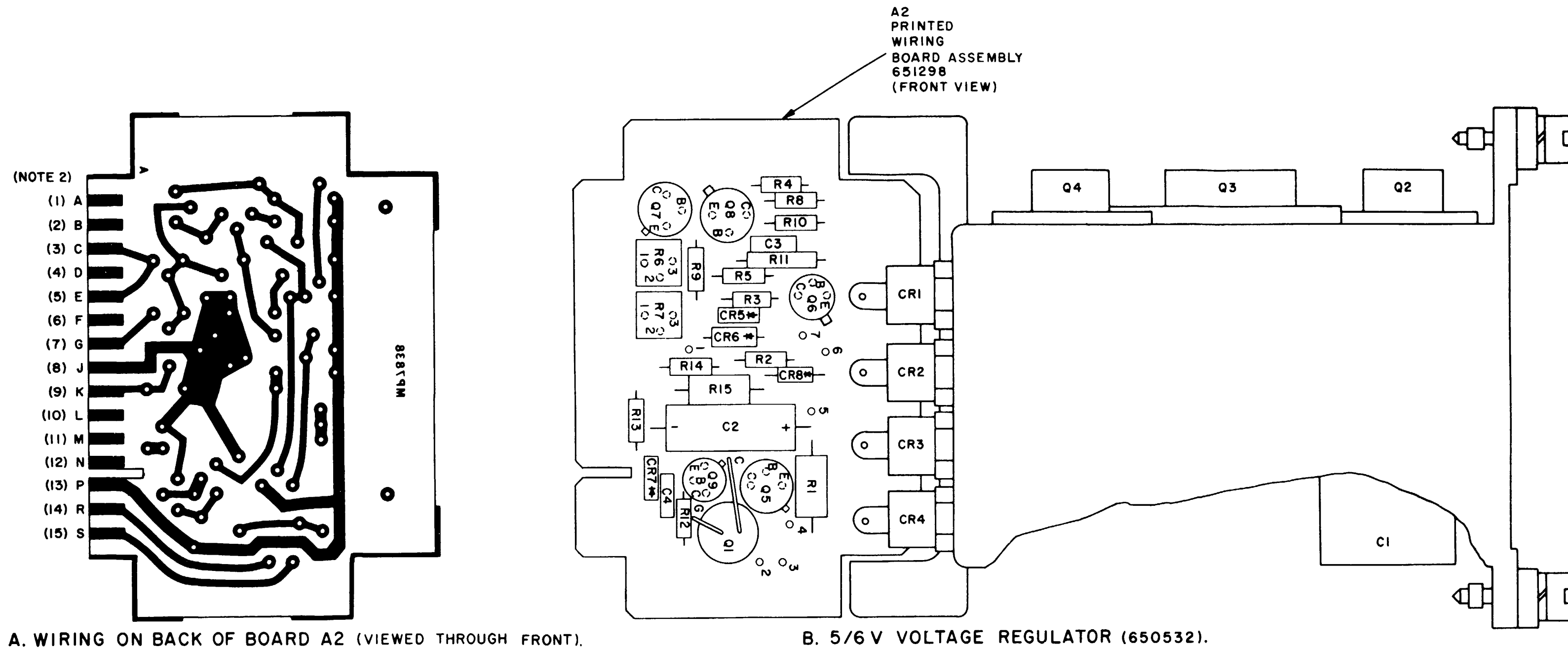


Figure 5-58. 220 MHz frequency multiplier-osc 2A13, schematic diagram.

Change 1 5-133



A. WIRING ON BACK OF BOARD A2 (VIEWED THROUGH FRONT).

B. 5/6 V VOLTAGE REGULATOR (650532).

NOTES:

1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A1A1, 1A1A2, 1A1A3, OR 1A1A4 AND THE SUBASSEMBLY DESIGNATION.

2. TERMINAL DESIGNATIONS IN ( ) ARE THOSE APPEARING ON MATING CONNECTOR OF POWER SUPPLY CHASSIS 1A1A13.

3. PRINTED CIRCUIT BOARD MP7838 OR MP7838-2C IS USED FOR THE VOLTAGE REGULATOR. REFER TO APPROPRIATE PARTS LOCATION AND PRINTED WIRING DIAGRAM ① OR ②.

EL5820-695-35-TM-C1-35 ①

Figure 5-59 (1). 5/6 v voltage regulator 1A1A1 through 1A1A4, parts location and printed wiring diagram (part 1 of 2).

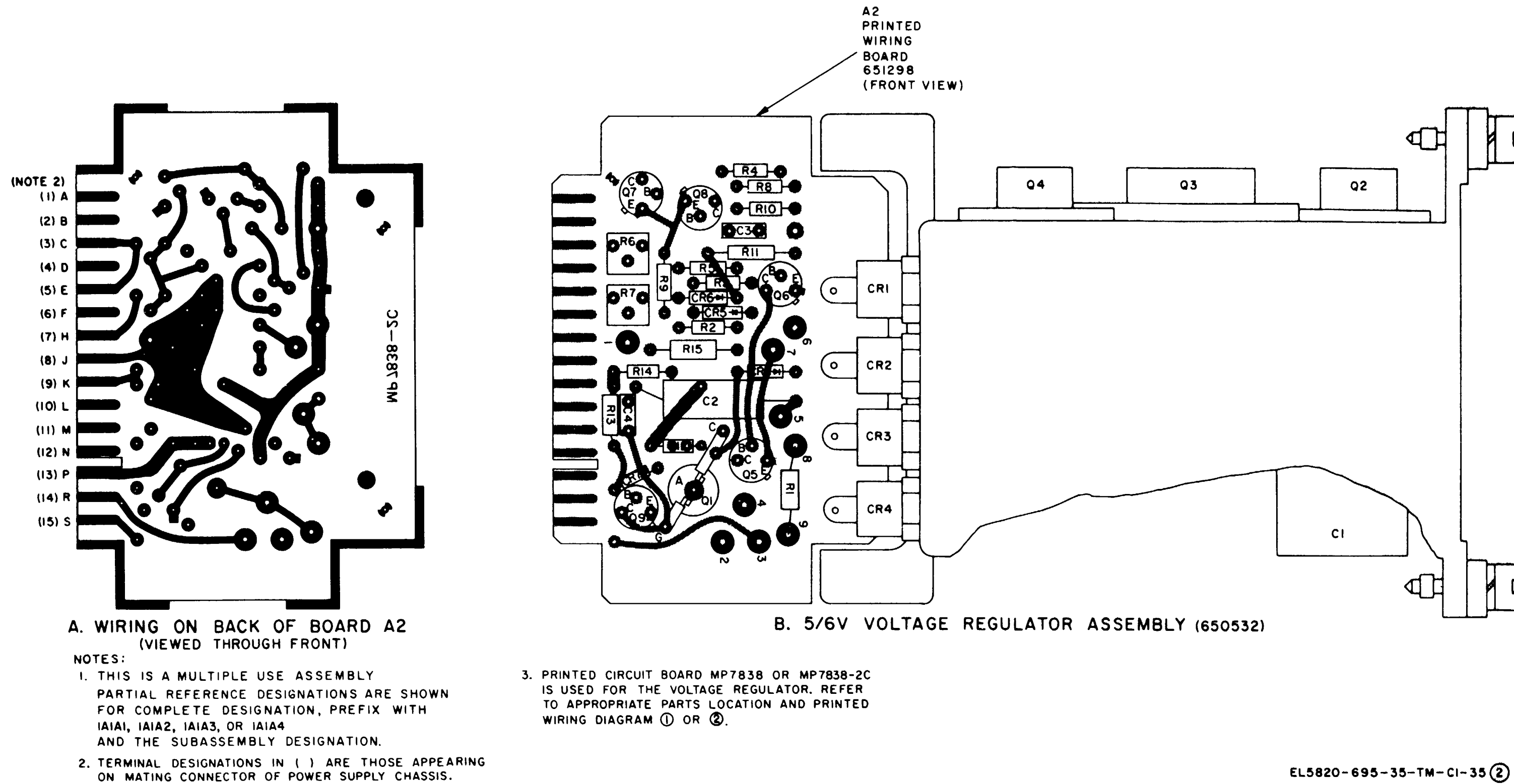
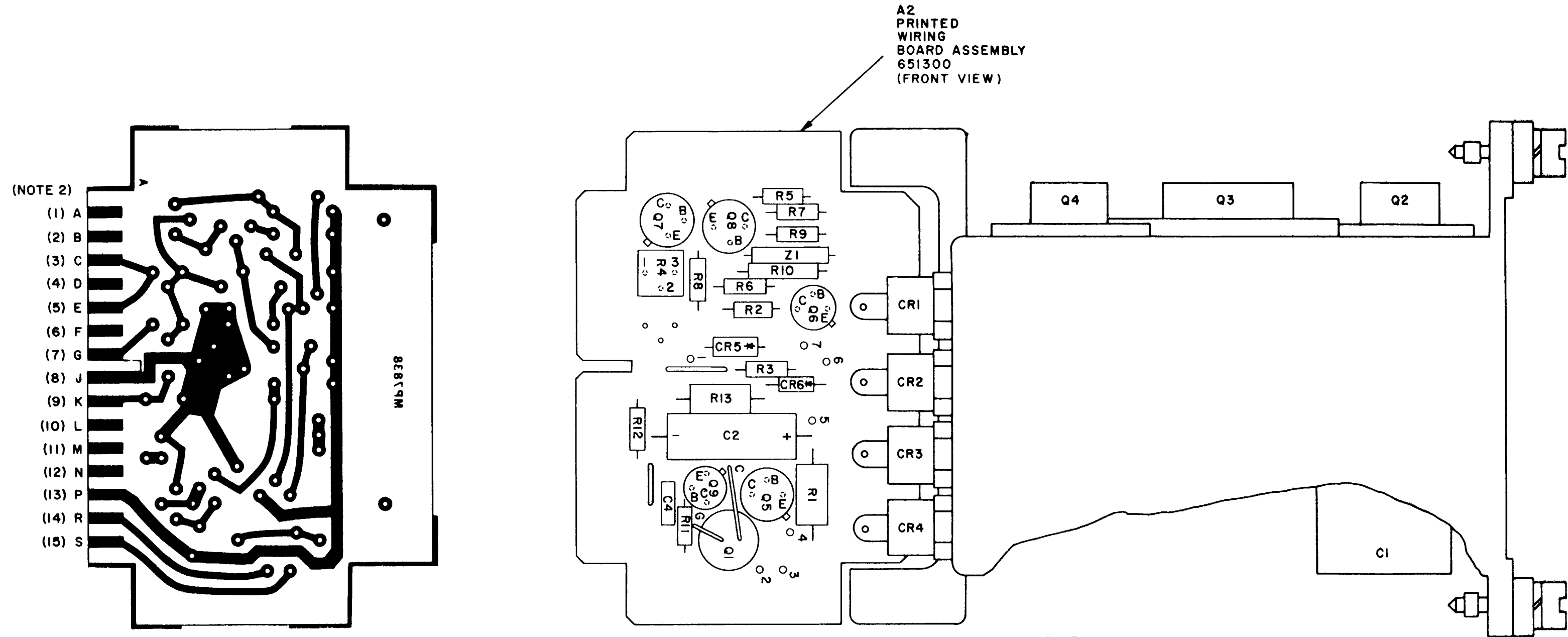


Figure 5-59 (2). 5/6 v voltage regulator 1A1A1 through 1A1A4, parts location and printed wiring diagram (part 2 of 2).



NOTES:

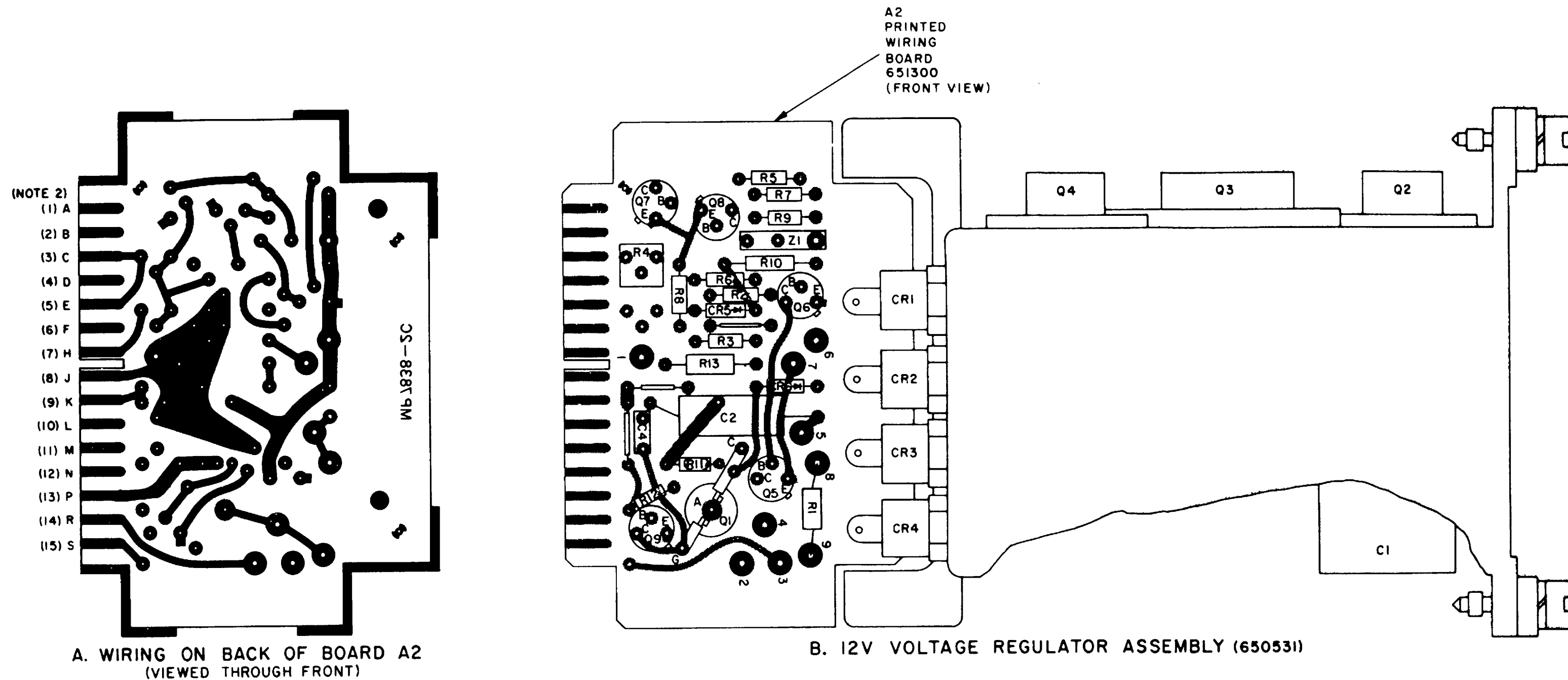
1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A1A6, 1A1A7, 1A1A8, 1A1A9, OR 2A1A3 AND THE SUBASSEMBLY DESIGNATION.

2. TERMINAL DESIGNATIONS IN ( ) ARE THOSE APPEARING ON MATING CONNECTOR OF POWER SUPPLY CHASSIS.

3. PRINTED CIRCUIT BOARD MP7858 OR MP7858-2C IS USED FOR THE VOLTAGE REGULATOR. REFER TO APPROPRIATE PARTS LOCATION AND PRINTED WIRING DIAGRAM ① OR ②.

EL5820-695-35-TM-C1-36 ①

Figure 5-60 (1). 12 v voltage regulator 1A1A6 through 1A1A9 and 2A1A3, parts location and printed wiring diagram (part 1 of 2).



A. WIRING ON BACK OF BOARD A2  
(VIEWED THROUGH FRONT)

B. 12V VOLTAGE REGULATOR ASSEMBLY (650531)

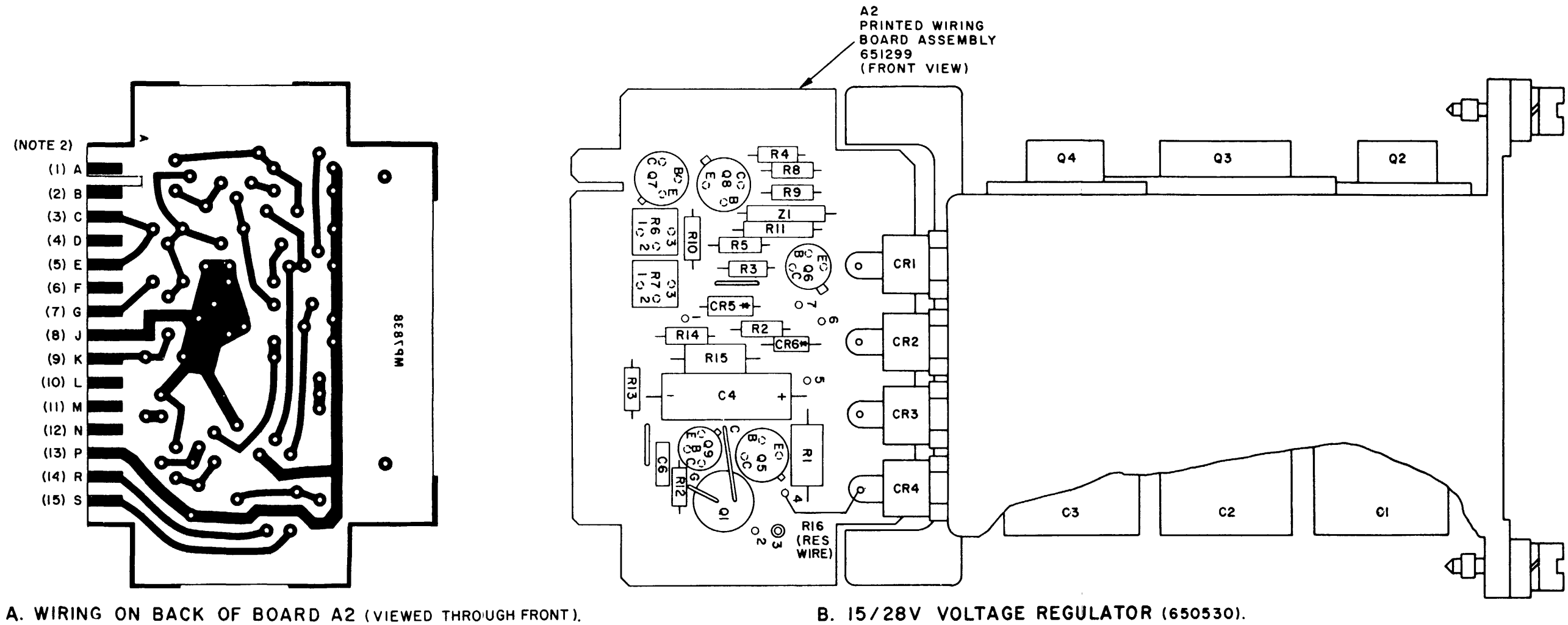
NOTES:

1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A1A6, 1A1A7, 1A1A8, 1A1A9, OR 2A1A3 AND THE SUBASSEMBLY DESIGNATION.
2. TERMINAL DESIGNATIONS IN ( ) ARE THOSE APPEARING ON MATING CONNECTOR OF POWER SUPPLY CHASSIS.

3. PRINTED CIRCUIT BOARD MP7838 OR MP7838-2C IS USED FOR THE VOLTAGE REGULATOR. REFER TO APPROPRIATE PARTS LOCATION AND PRINTED WIRING DIAGRAM ① OR ②.

EL5820-695-35-TM-CI-36 ②

Figure 5-60 (2). 12 v voltage regulator 1A1A6 through 1A1A9 and 2A1A3, parts location and printed wiring diagram (part 2 of 2).



NOTES:

1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A1A10, 1A1A11, 1A1A12, 2A1A1, 2A1A2, OR 2A1A4 AND THE SUBASSEMBLY DESIGNATION.

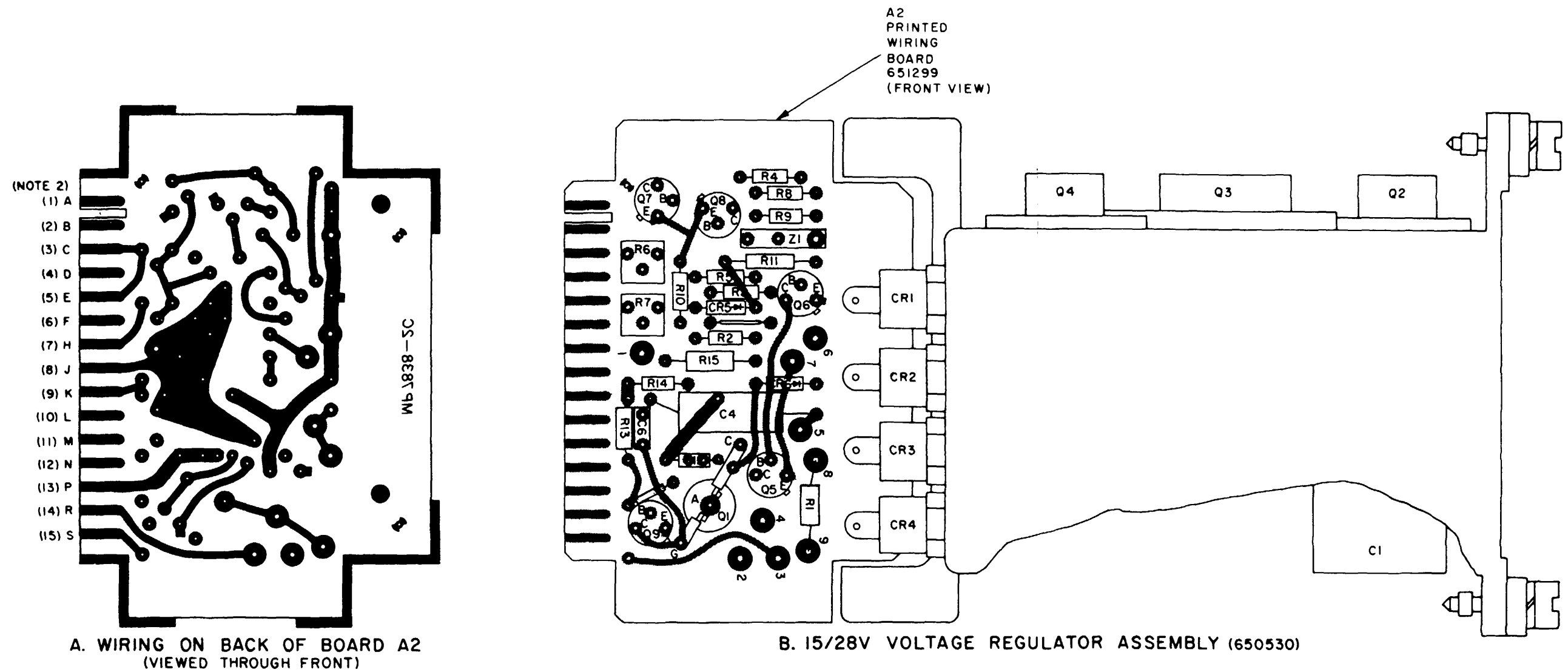
2. TERMINAL DESIGNATIONS IN ( ) ARE THOSE APPEARING ON MATING CONNECTOR OF POWER SUPPLY CHASSIS.

3. PRINTED CIRCUIT BOARD MP3878 OR MP3878-2C IS USED FOR THE VOLTAGE REGULATOR. REFER TO APPROPRIATE PARTS LOCATION AND PRINTED WIRING DIAGRAM ① OR ②.

EL5820-695-35-TM-C1-37 ①

Figure 5-61.(1). 15/28 v voltage regulator 1A1A10 through 1A1A12, 2A1A1, 2A1A2, and 2A1A4, parts location and printed wiring diagram (part 1 of 2).





A. WIRING ON BACK OF BOARD A2  
(VIEWED THROUGH FRONT)

B. 15/28V VOLTAGE REGULATOR ASSEMBLY (650530)

NOTES:

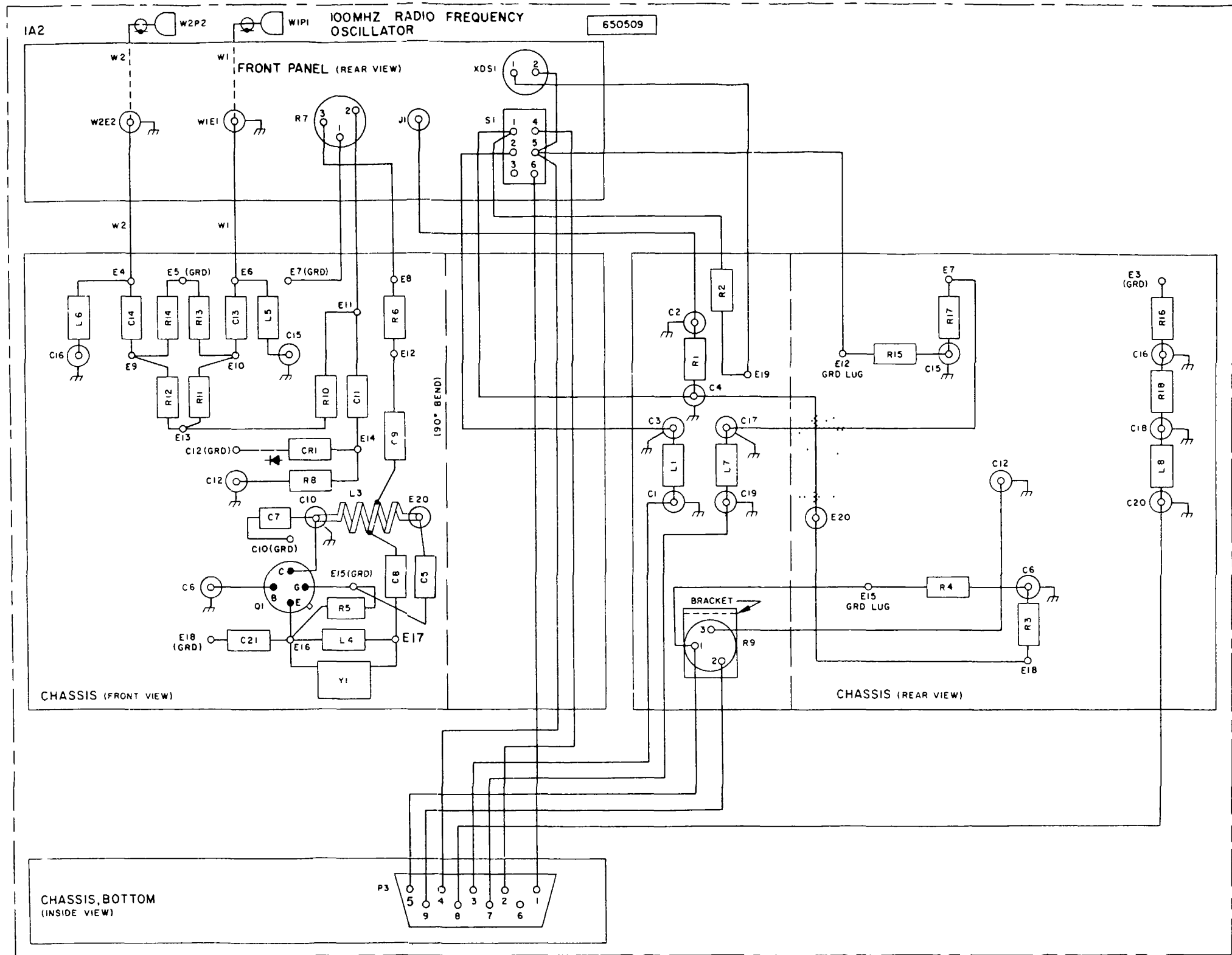
1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH 1A1A10, 1A1A11, 1A1A12, 2A1A1, 2A1A2, OR 2A1A4 AND THE SUBASSEMBLY DESIGNATION.
2. TERMINAL DESIGNATIONS IN ( ) ARE THOSE APPEARING ON MATING CONNECTOR OF POWER SUPPLY CHASSIS.

3. PRINTED CIRCUIT BOARD MP7838 OR MP7838-2C IS USED FOR THE VOLTAGE REGULATOR. REFER TO APPROPRIATE PARTS LOCATION AND PRINTED WIRING DIAGRAM (1) OR (2).

EL5820-695-35-TM-CI-37 (2)

Figure 5-61 (2). 15/28 v voltage regulator 1A1A10 through 1A1A12, 2A1A1, 2A1A2, and 2A1A4, parts location and printed wiring diagram (part 2 of 2).

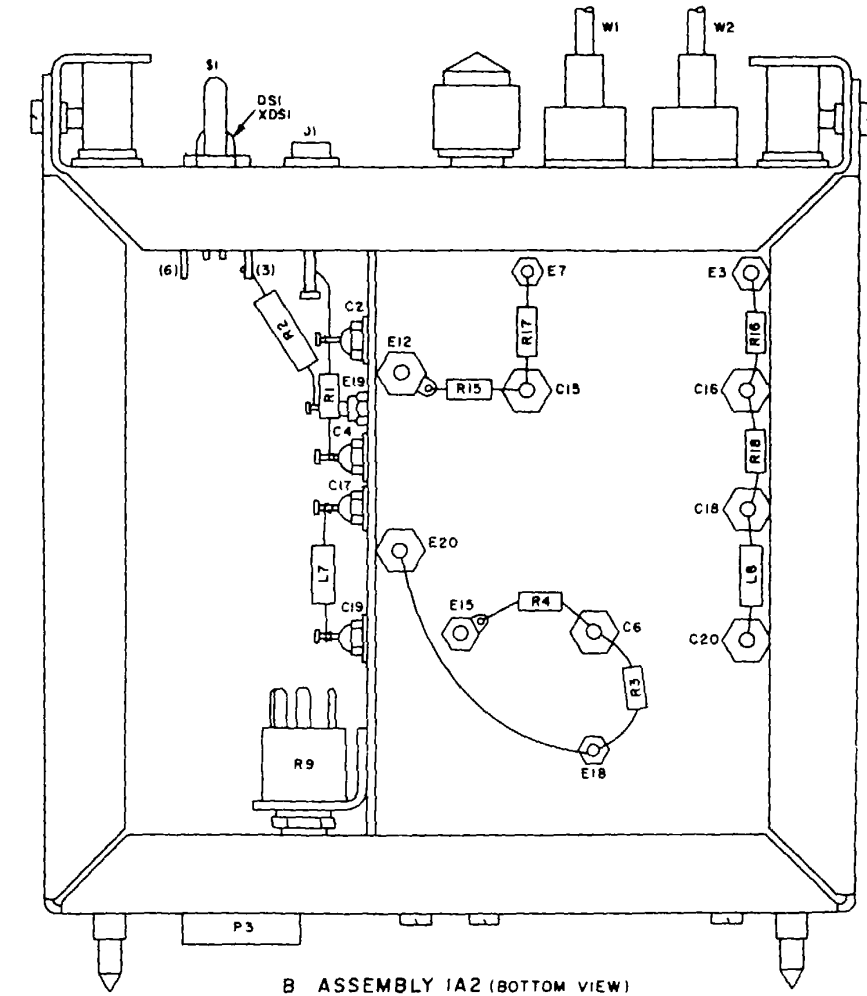
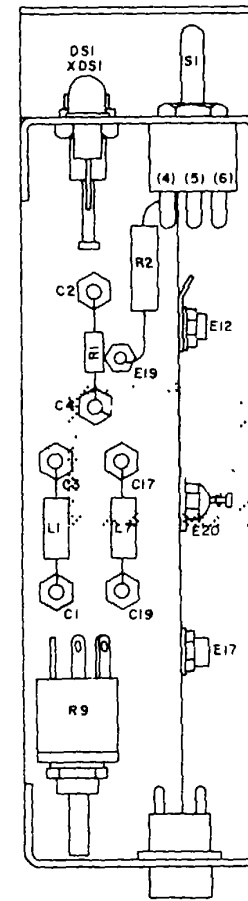
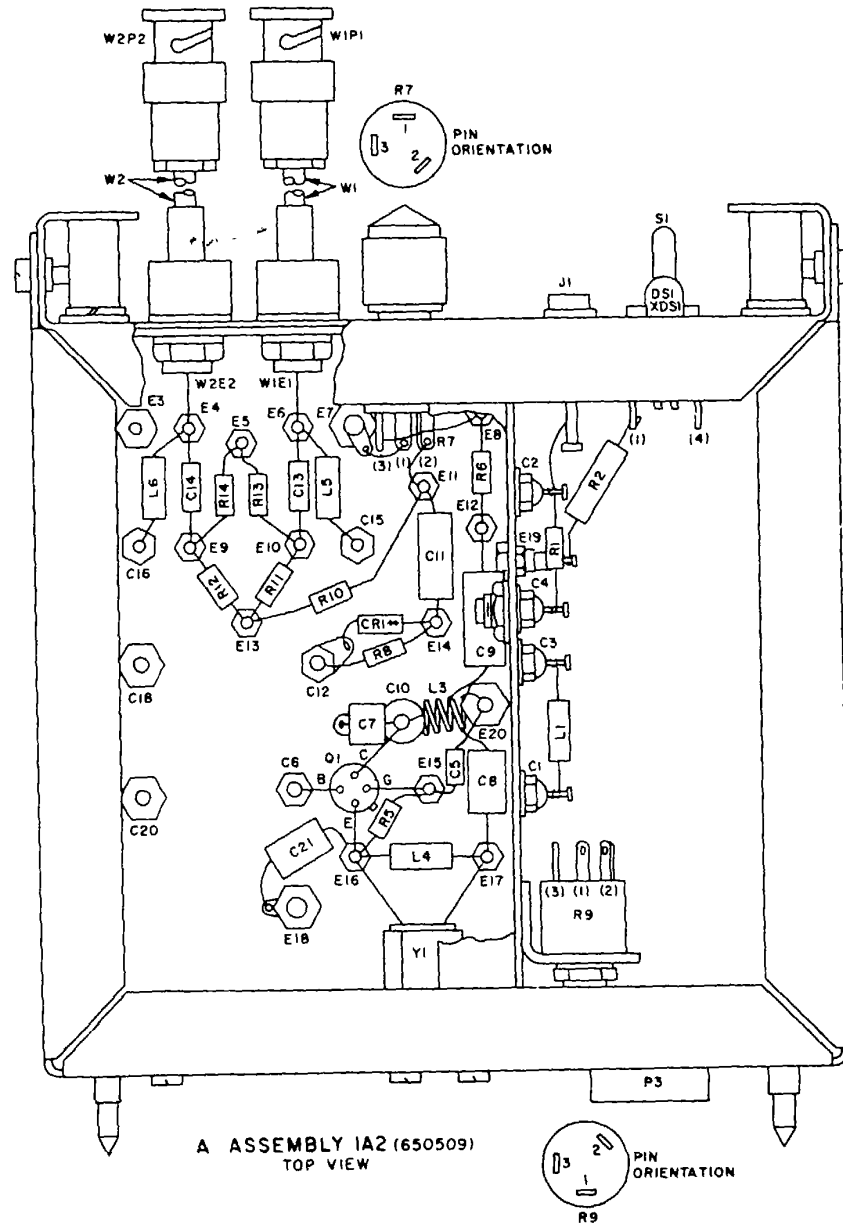
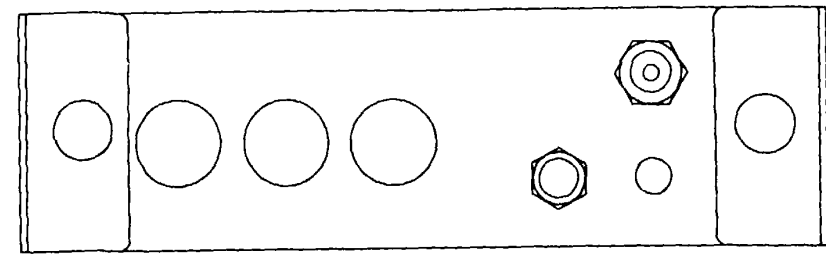
- NOTE
- 1 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH 1A2
  - 2 ALL WIRE IS NO 22 AWG STRANDED TEFLON INSULATED



E LOFB013

Figure 5-62. 100 MHz radio frequency oscillator 1A2, wiring diagram.

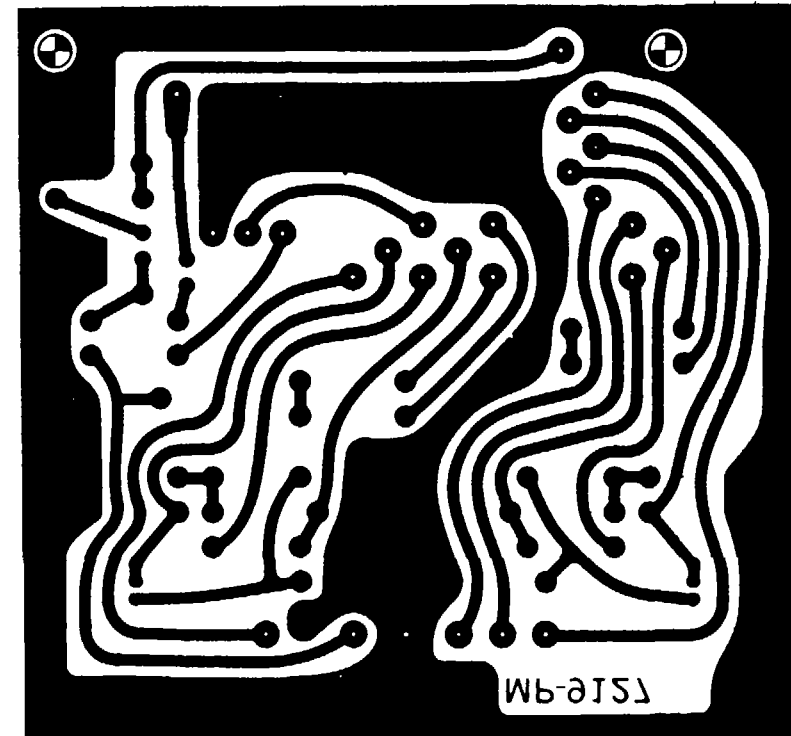
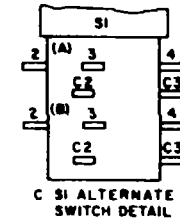
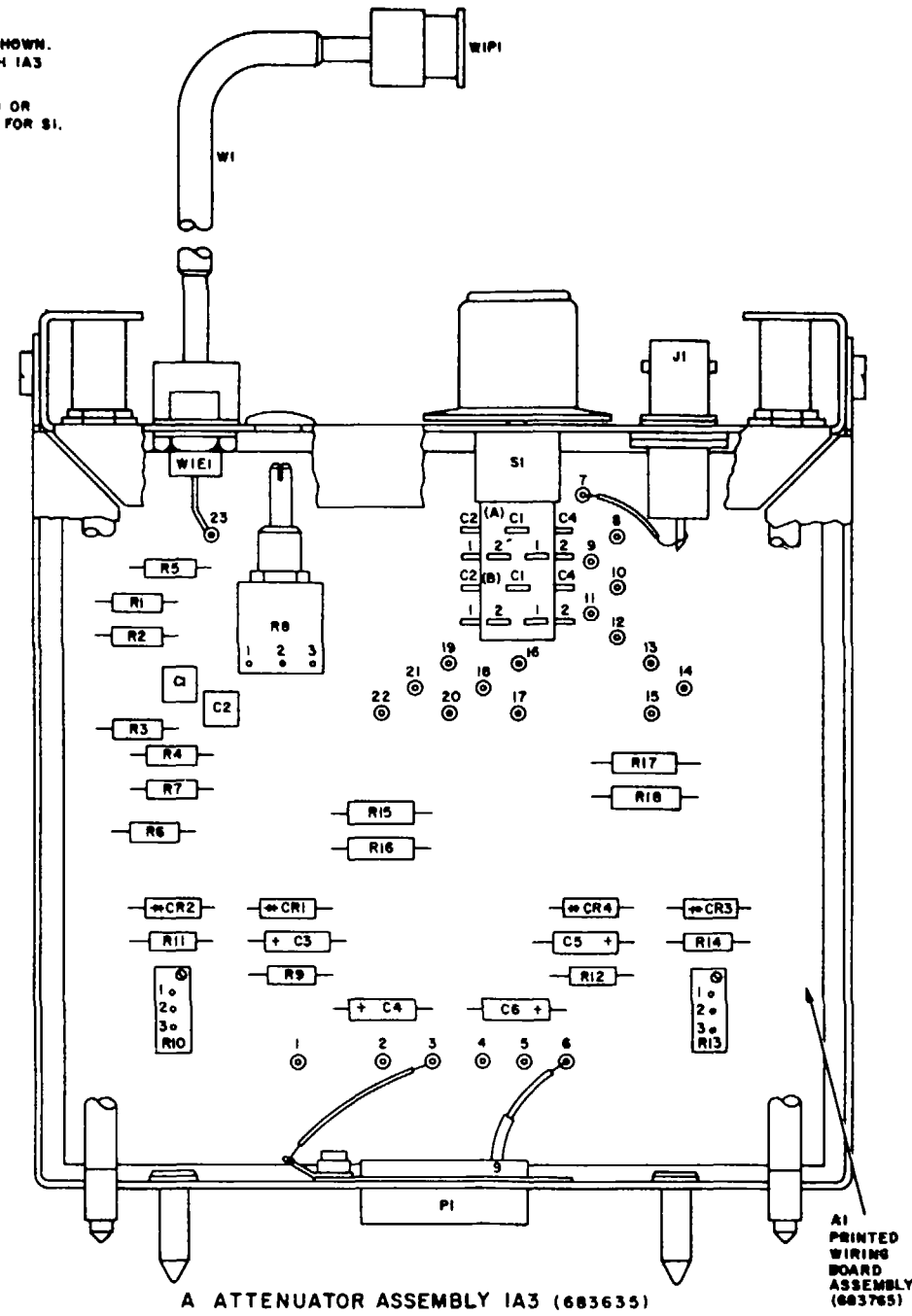
NOTE  
PARTIAL REFERENCE  
DESIGNATIONS ARE SHOWN  
FOR COMPLETE DESIGNATION.  
PREFIX WITH 1A2



FLOFB014

Figure 5-63. 100 MHz radio frequency oscillator 1A2, parts location.

NOTES  
 1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.  
 FOR COMPLETE DESIGNATION PREFIX WITH IA3  
 AND SUBASSEMBLY DESIGNATION  
 2. SWITCH PART NO. SM-B-684390 (DETAIL A) OR  
 PART NO SM-B-684783 (DETAIL C) IS USED FOR S1.

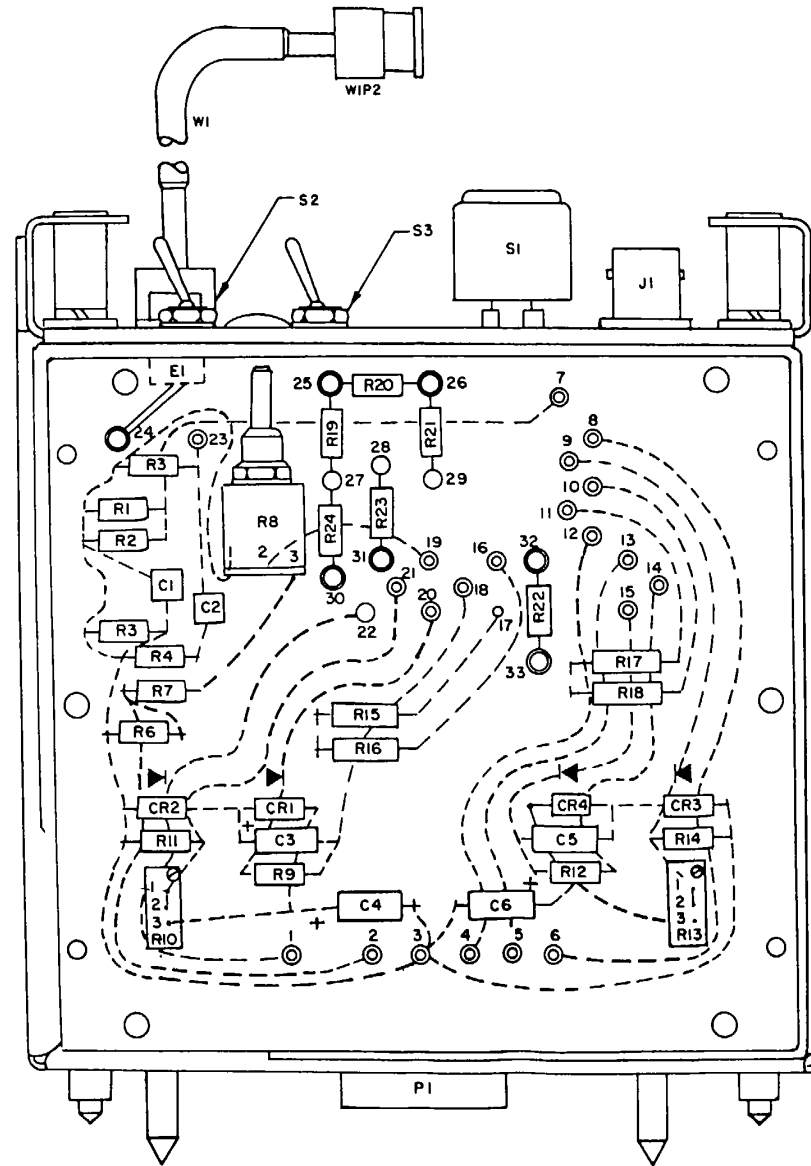
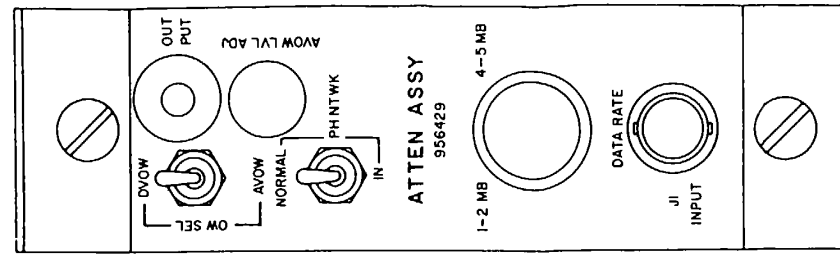


B. WIRING ON BACK OF BOARD A1 (VIEWED THROUGH FRONT)  
 EL5820-695-35-TM-C1-38

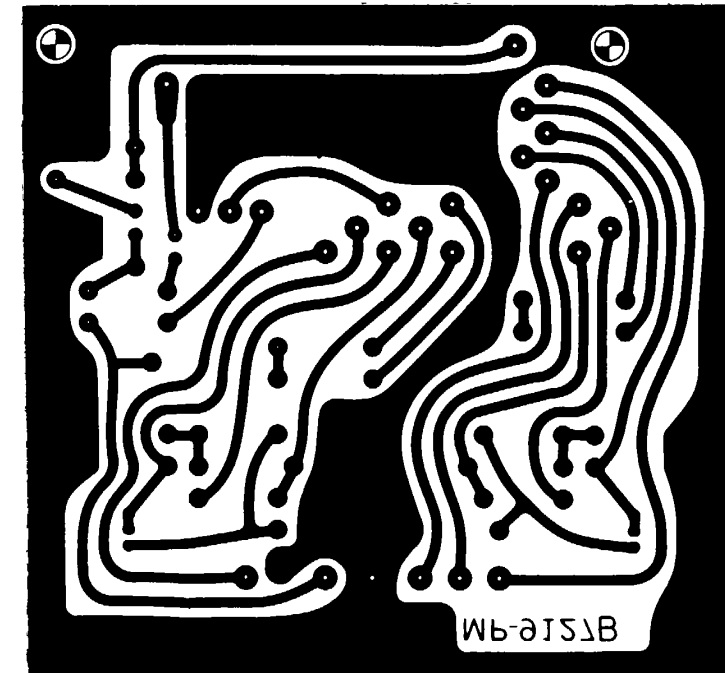
Figure 5-64. Attenuator assembly 1A3, parts location and printed wiring diagram.

NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.
2. ----- INDICATES WIRING ON REAR OF BOARD



A. ATTENUATOR ASSEMBLY (956429)

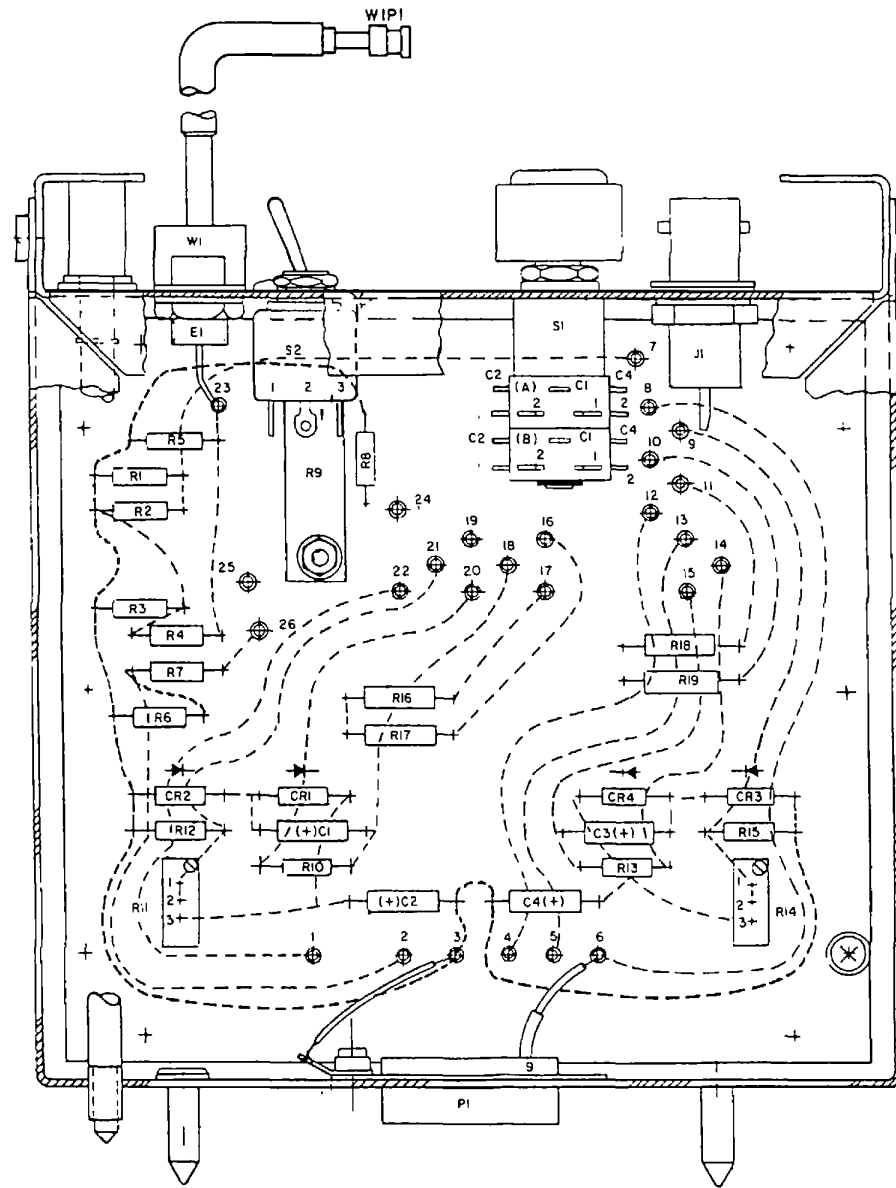
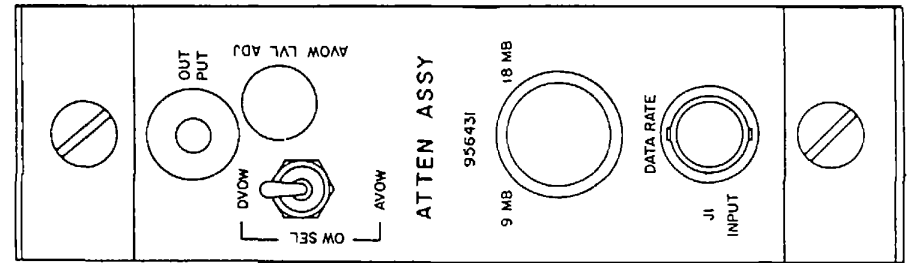


B WIRING ON BACK OF BOARD A1 (VIEWED THROUGH FRONT)

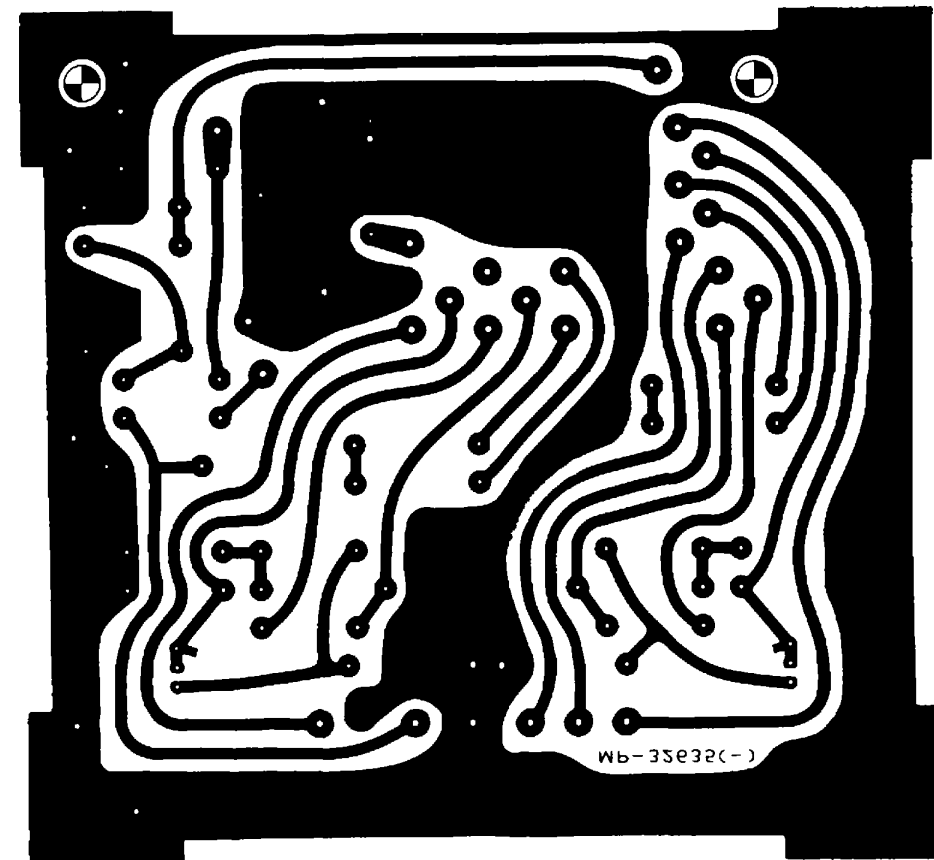
Figure 5-64.1. Attenuator assembly 1A3 (956429), parts location and printed wiring diagram.

NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.
2. ----- INDICATES WIRING ON REAR OF BOARD



A. ATTENUATOR ASSEMBLY 1A3 (956431)



B. WIRING ON BACK OF BOARD AS (VIEWED THROUGH FRONT)

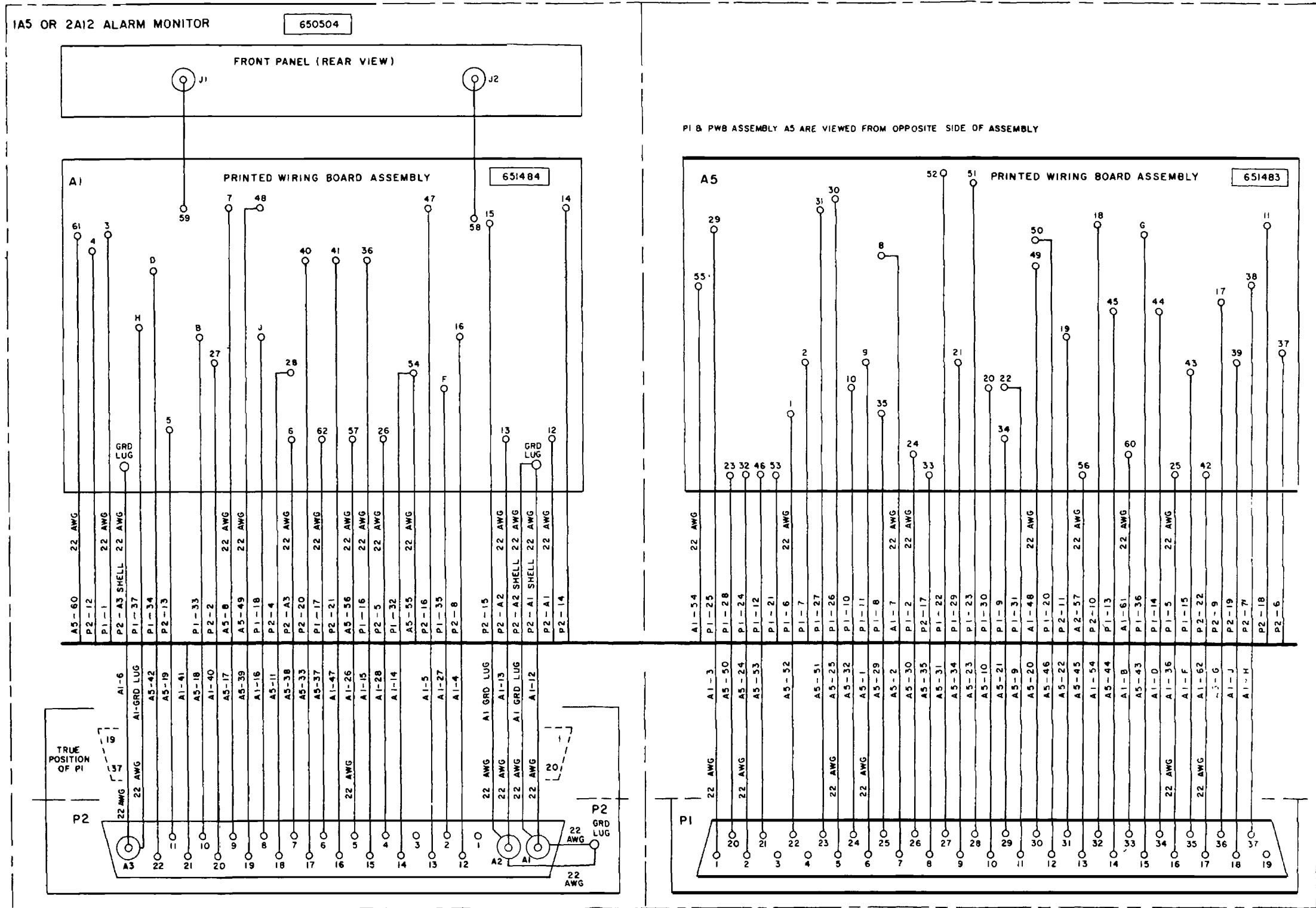
Figure 5-64.2. Attenuator assembly 1A3 (956431) parts location and printed wiring diagram.

Change 6 5-143.3

NOTES

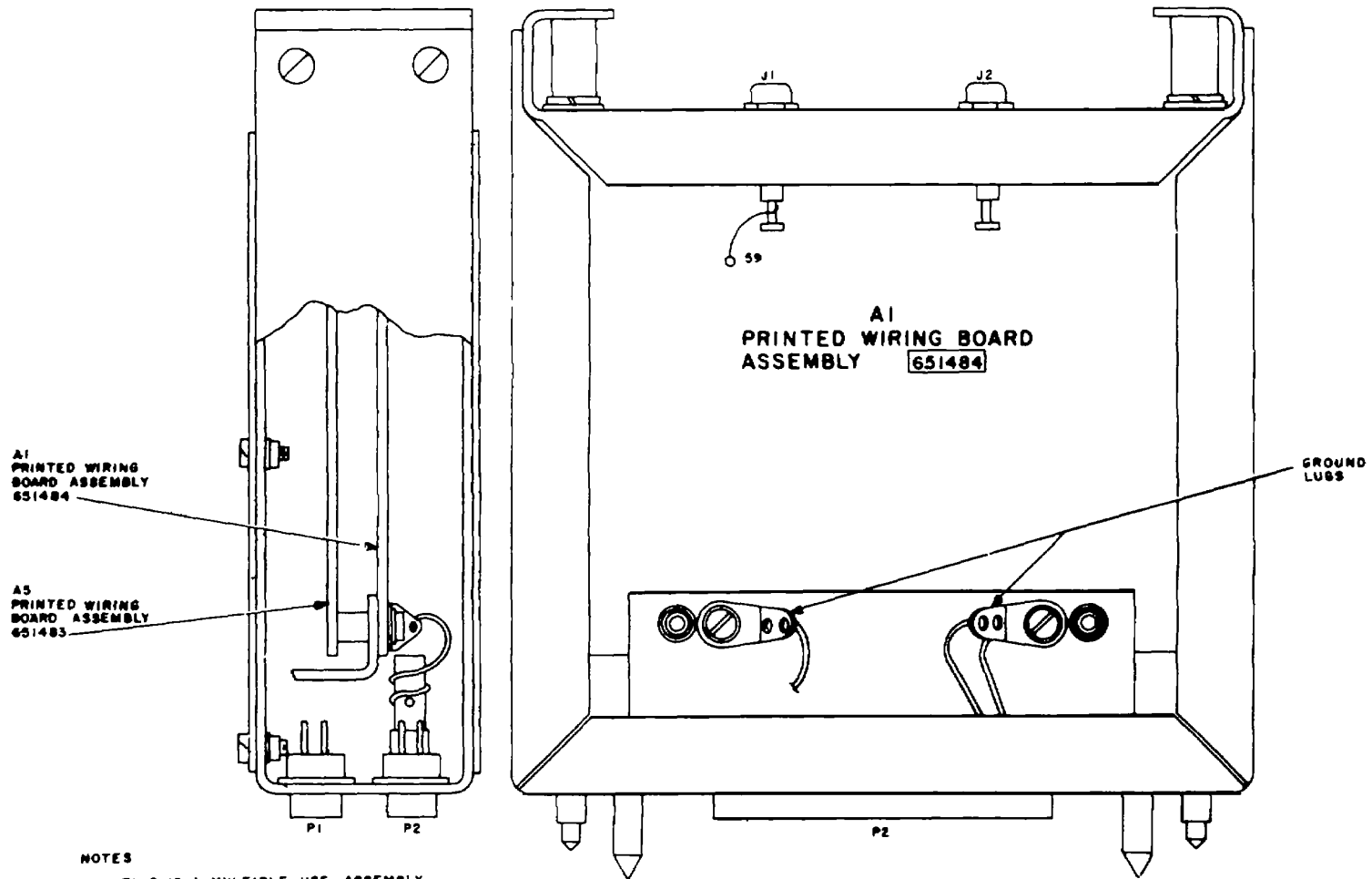
1. THIS IS A MULTIPLE USE ASSEMBLY PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION

2. ALL WIRE IS NO 26 AWG STRANDED TEFLON INSULATED, UNLESS SPECIFIED AS NO 22 AWG



EL 5020-695-35-TM-168

Figure 5-65. Alarm monitor 1A5/2A12, wiring diagram.



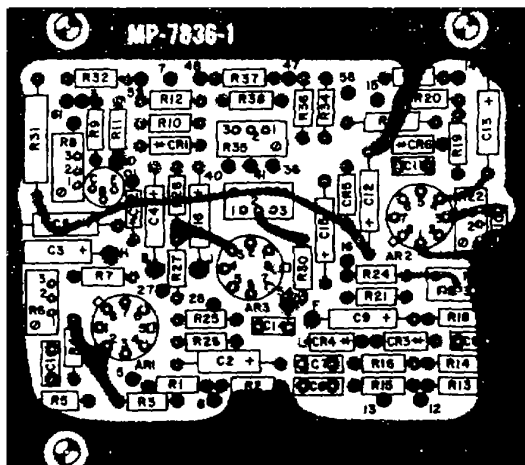
NOTES

- 1 THIS IS A MULTIPLE USE ASSEMBLY PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH 1A5 (T-1054/GRC-144) OR 2A12 (R-1467/GRC-144)
- 2 COMPONENT SIDES OF BOARDS FACE OUTWARD

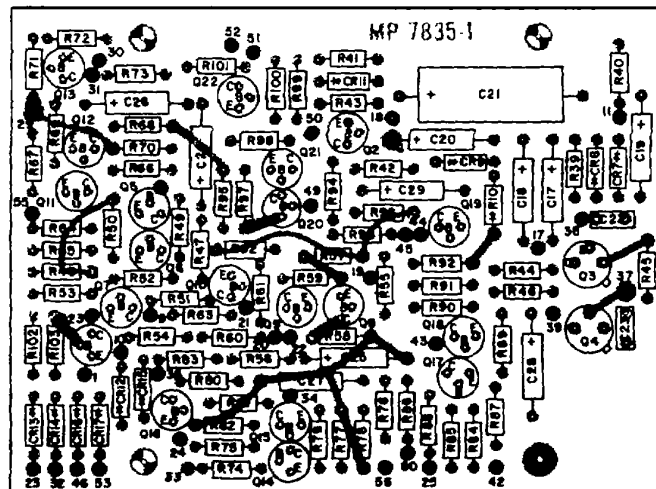
EL5820-695-35-TM-169 ①

Figure 5-66(1). Alarm monitor 1A5/2A12, parts location and printed wiring diagram (part 1 of 2).

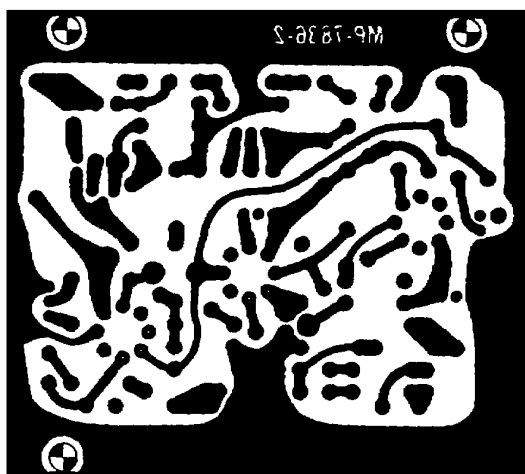




A. PARTS AND WIRING ON FRONT OF BOARD A1



C. PARTS AND WIRING ON FRONT OF BOARD A5.



B. WIRING ON BACK OF BOARD A1  
(VIEWED THROUGH FRONT)

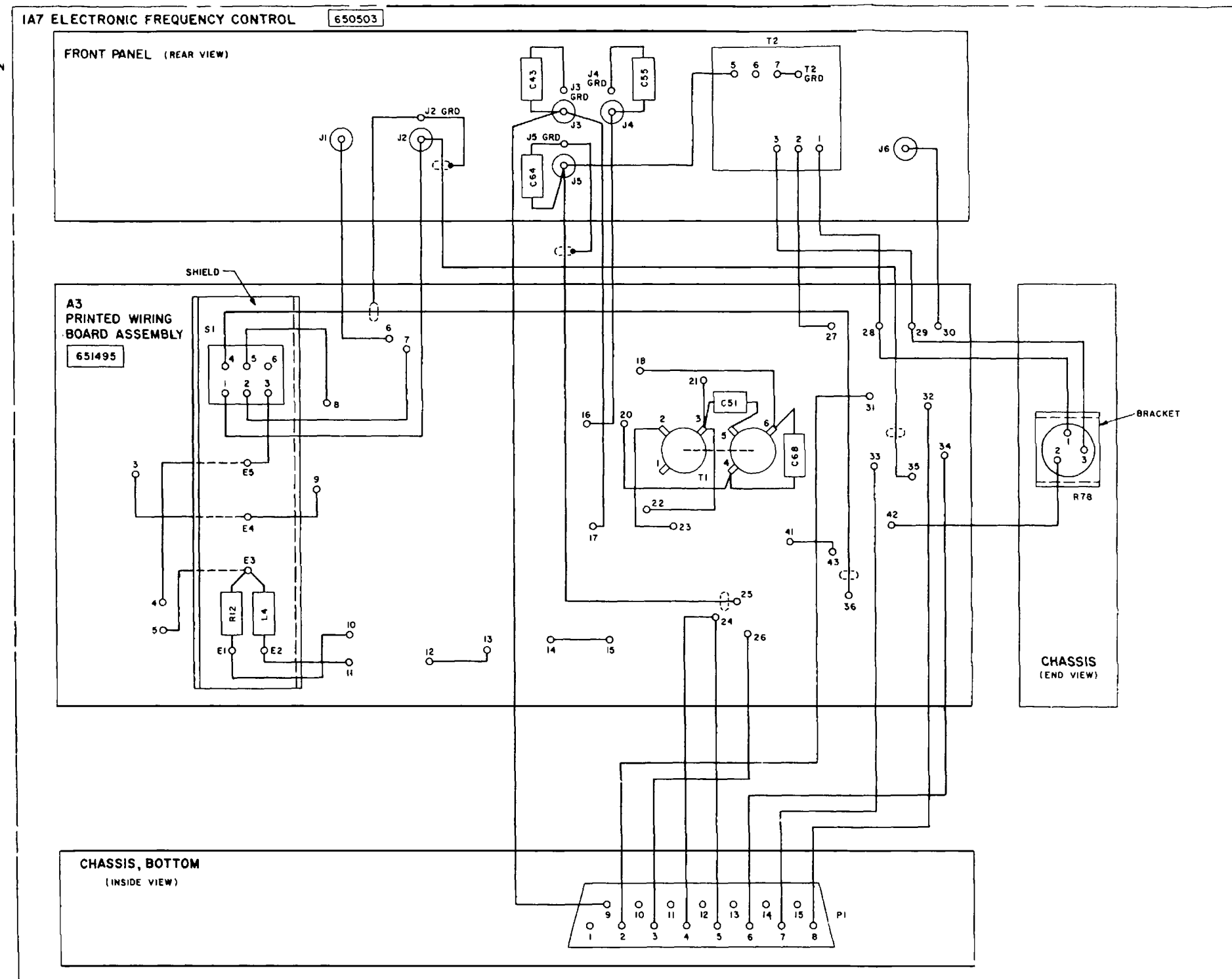


D WIRING ON BACK OF BOARD A5  
(VIEWED THROUGH FRONT)

EL210023

Figure 5-66(2). Alarm monitor 1A5/2A12, parts location and printed wiring diagram (part 2 of 2).

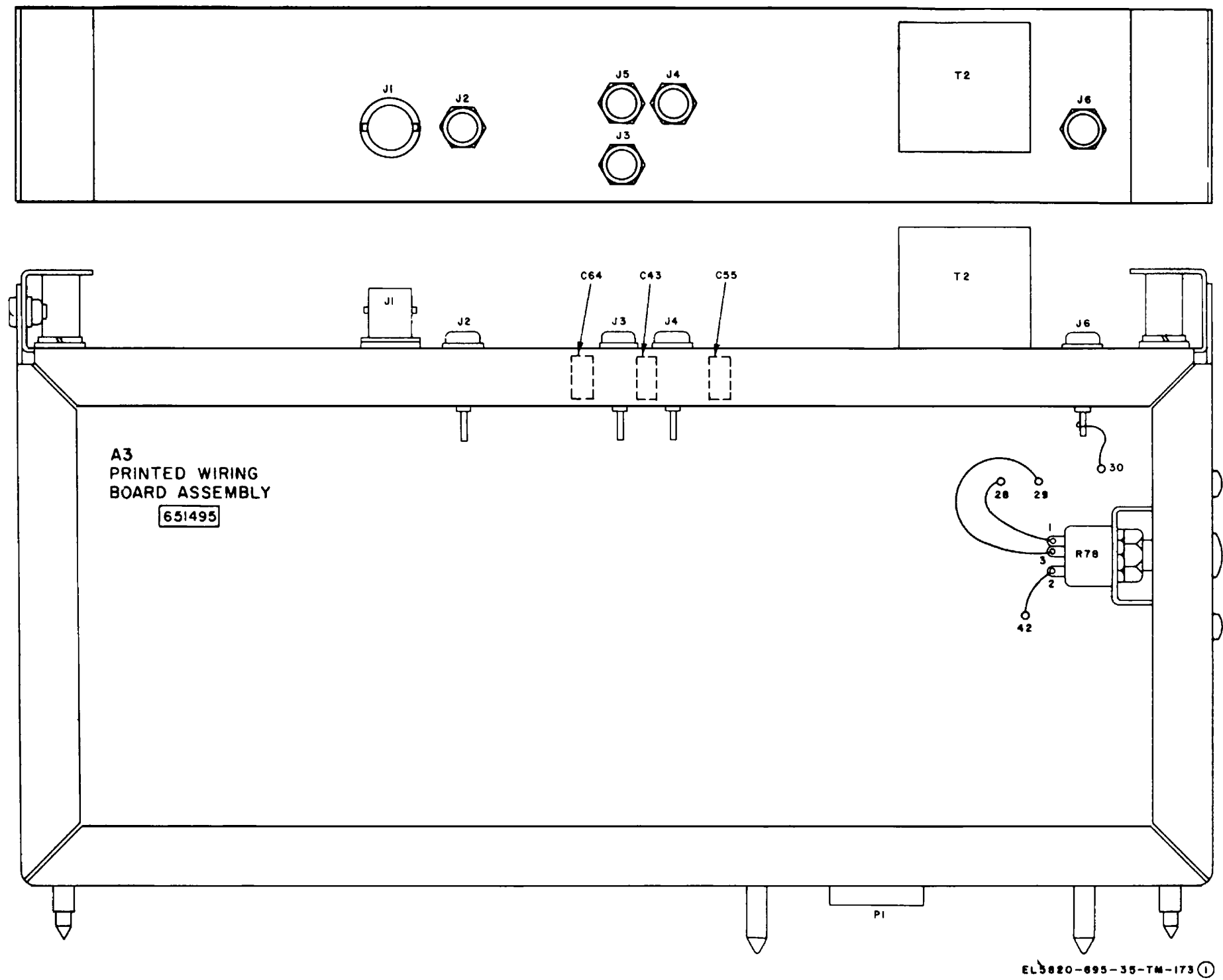
- NOTES
- 1 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION
  - 2 ALL WIRE IS NO 22 AWG STRANDED, TEFLON INSULATED



EI 5820-695-35-TM-172

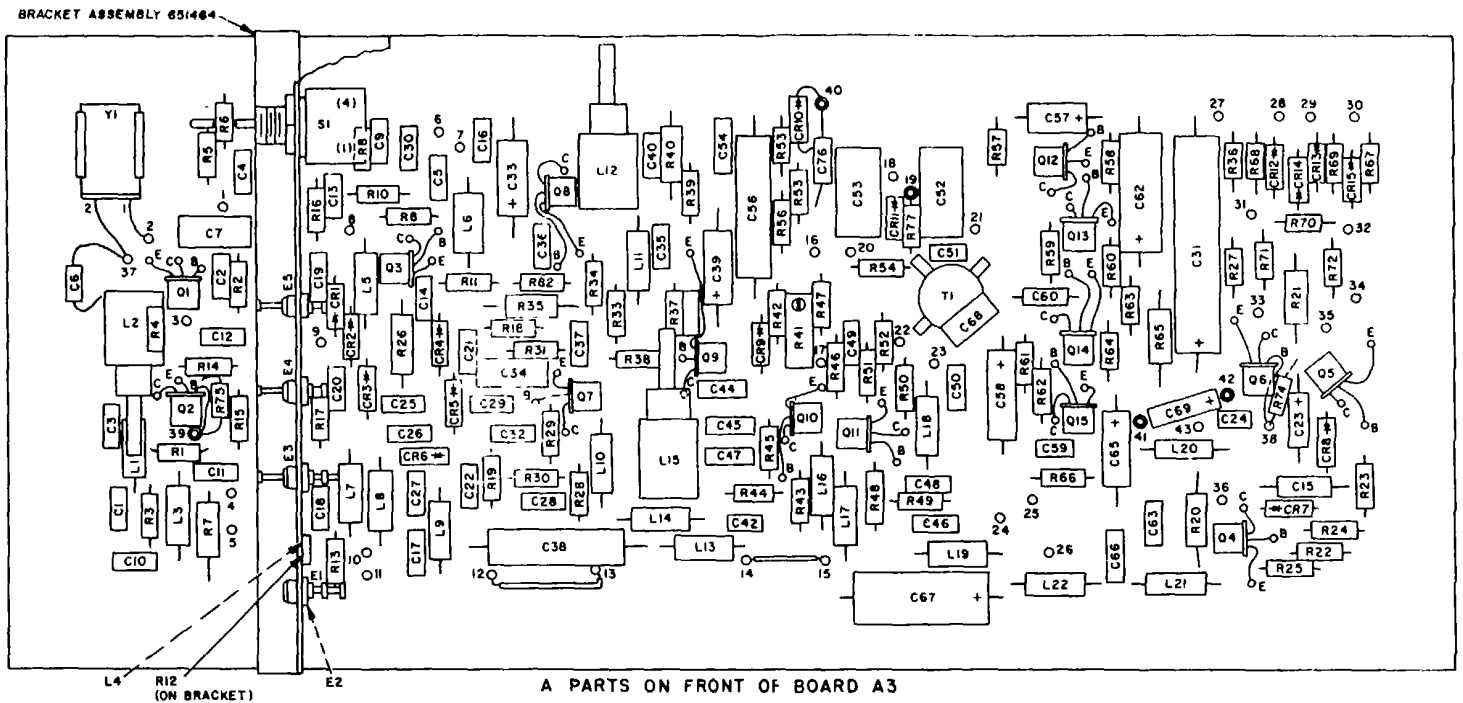
Figure 5-67. Electronic frequency control 1A7, wiring diagram.

NOTE:  
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.  
FOR COMPLETE DESIGNATION, PREFIX WITH 1A7.



EL 5820-695-35-TM-173 ①

Figure 5-68(1). Electronic frequency control 1A7, parts location and printed wiring diagram (part 1 of 2).



B WIRING ON BACK OF BOARD A3 (VIEWED THROUGH FRONT)

EL5820-695 35-TM-173(2)

Figure 5-68(2). Electronic frequency control 1A7, parts location and printed wiring diagram (part 2 of 2).

- NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH TAB.
  2. ALL WIRE IS NO 22 AWG STRANDED, TEFLON INSULATED.
  3. WIRING POINT TERMINAL NUMBERS (WT) ARE ASSIGNED FOR IDENTIFICATION PURPOSES ONLY. THEY ARE NOT MARKED ON EQUIPMENT.
  4. IN SOME COMPONENTS RESISTOR R18 IS ADDED AND SWITCH S1 IS SPST. IN THESE CASES RESISTOR R21 IS LOCATED ON THE ASSEMBLY BOTTOM.

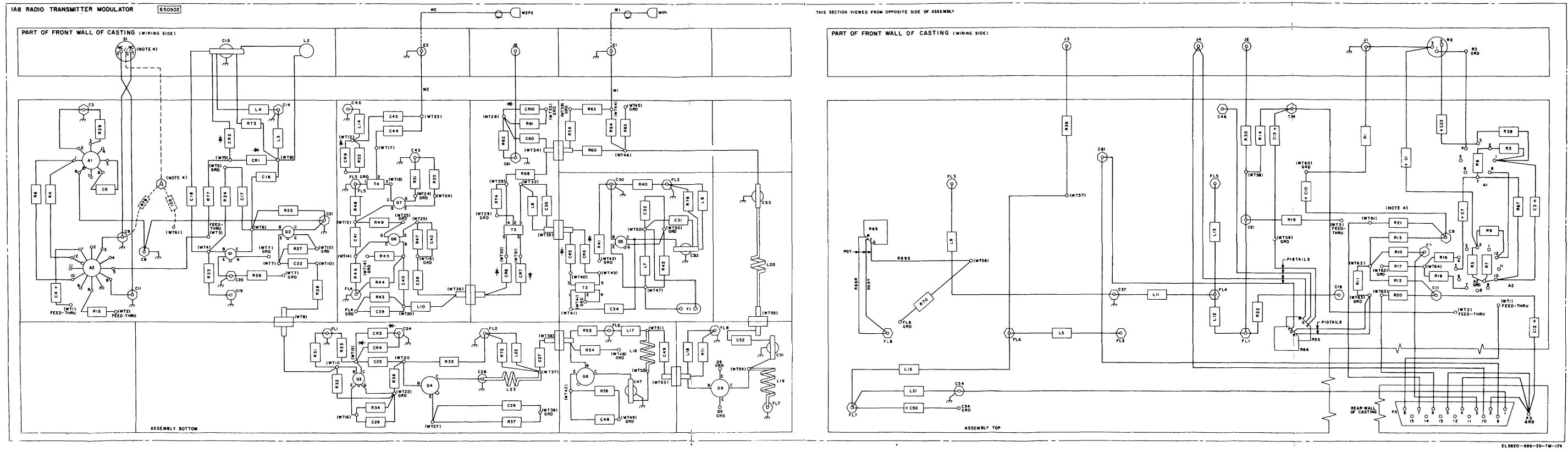


Figure 5-69. Radio transmitter modulator 1A8, wiring diagram.

NOTE  
 1 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH IAB  
 2 IN SOME COMPONENTS RESISTOR R78 IS ADDED AND SWITCH S1 IS SPDT IN THESE CASES RESISTOR R21 IS LOCATED ON THE ASSEMBLY BOTTOM

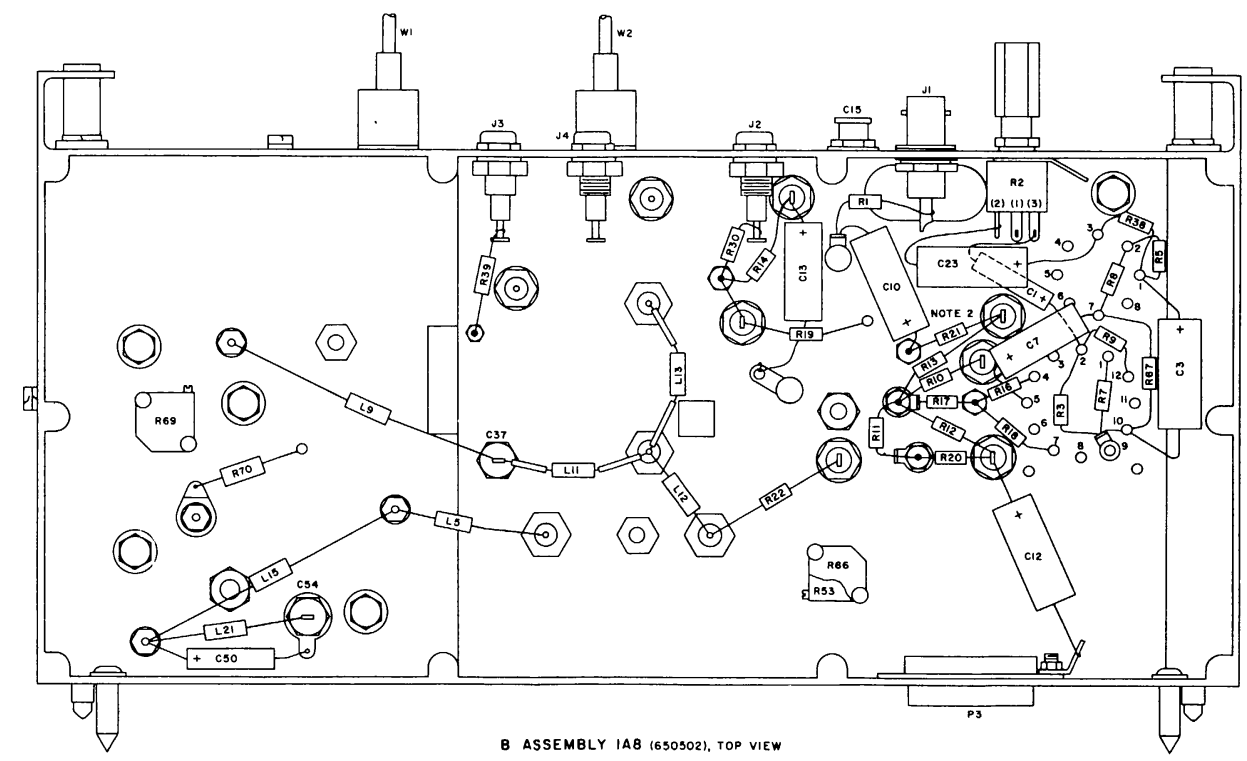
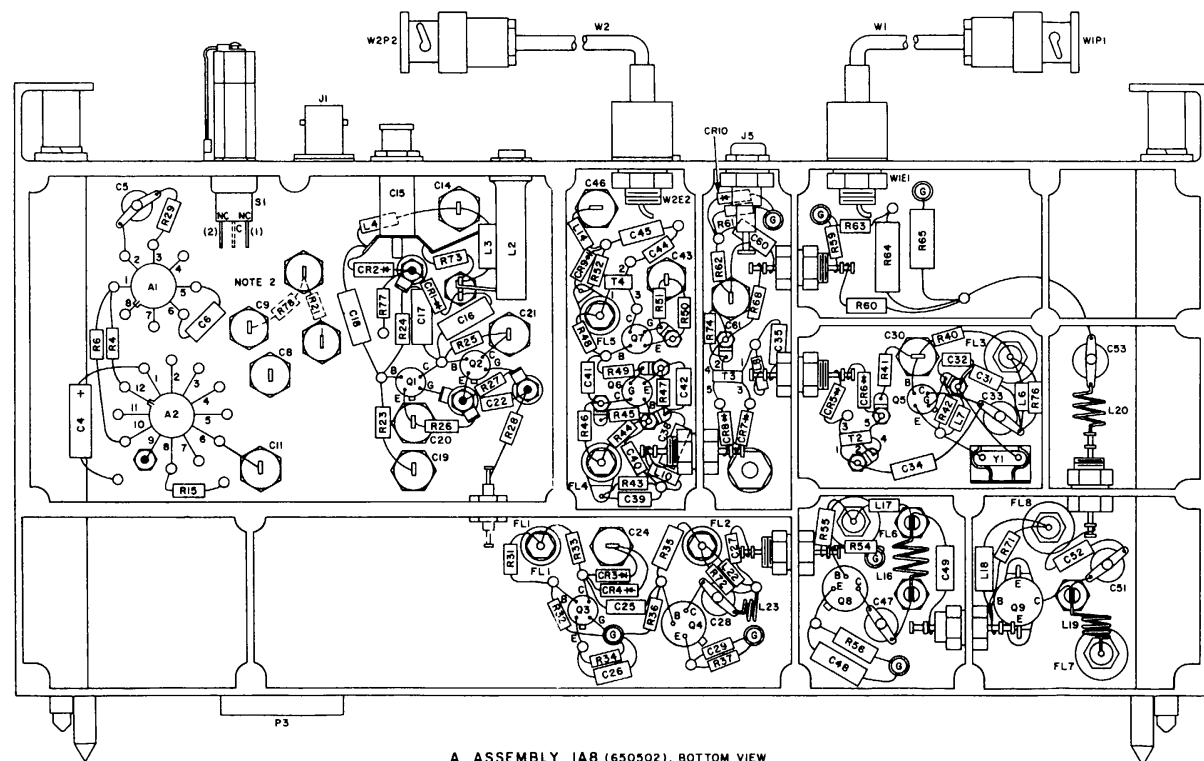
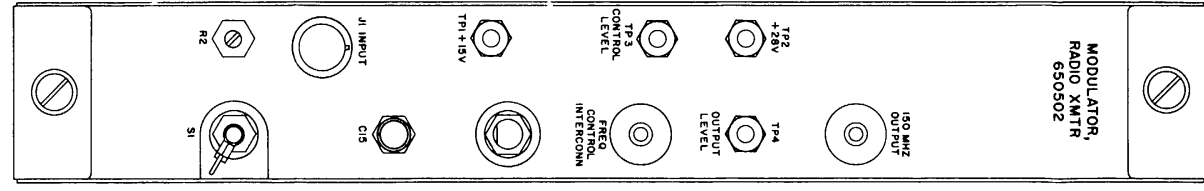
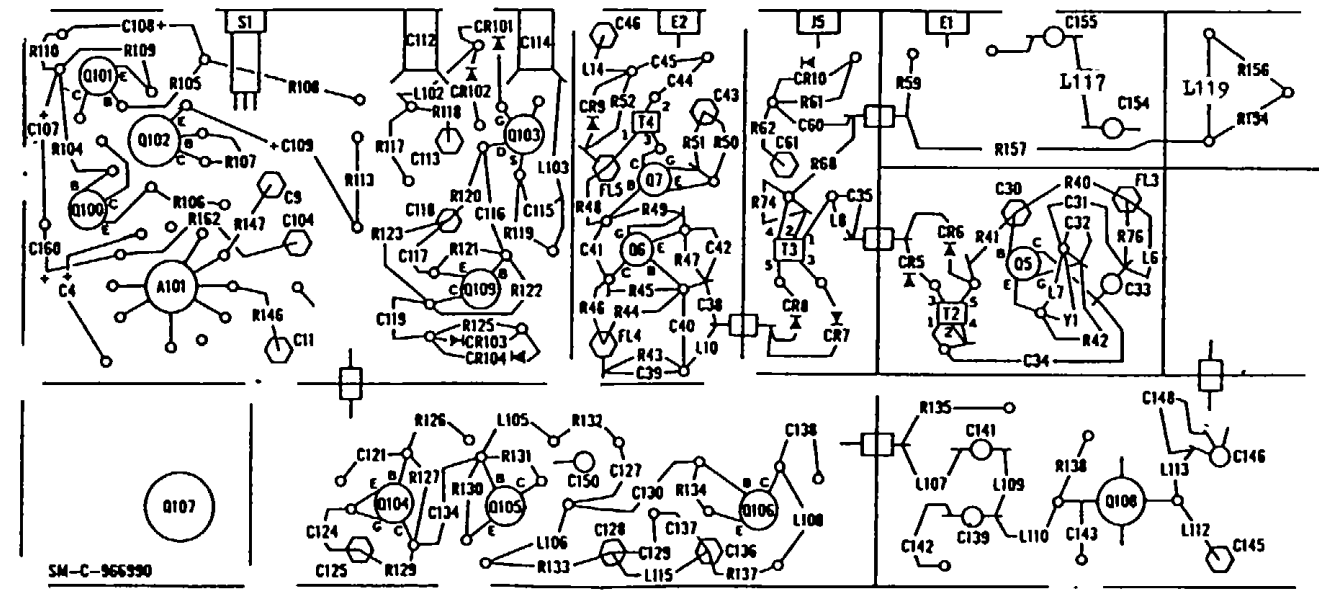
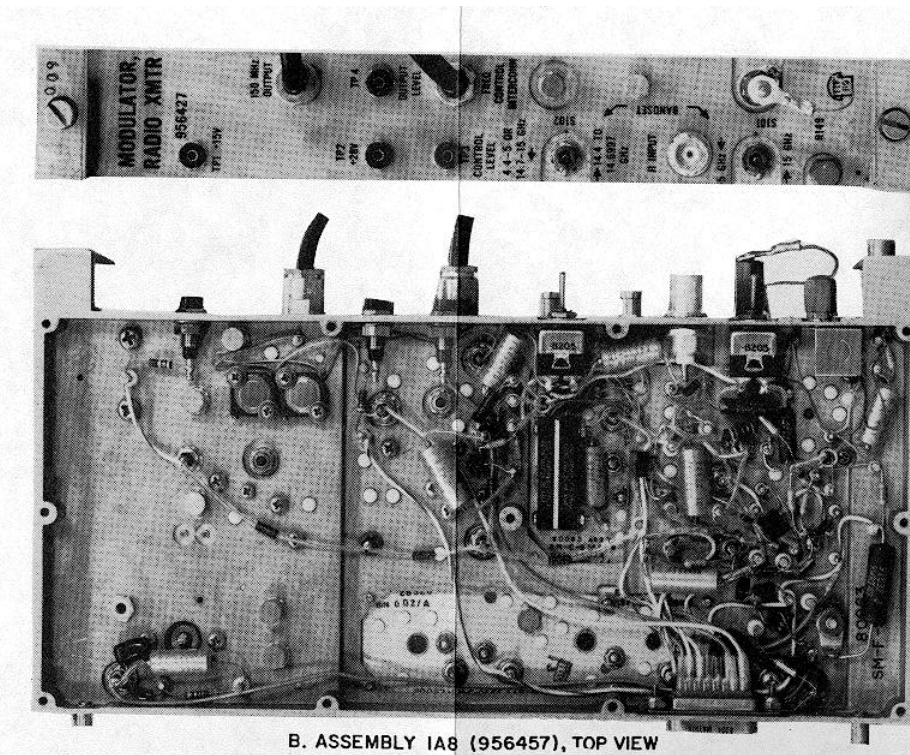
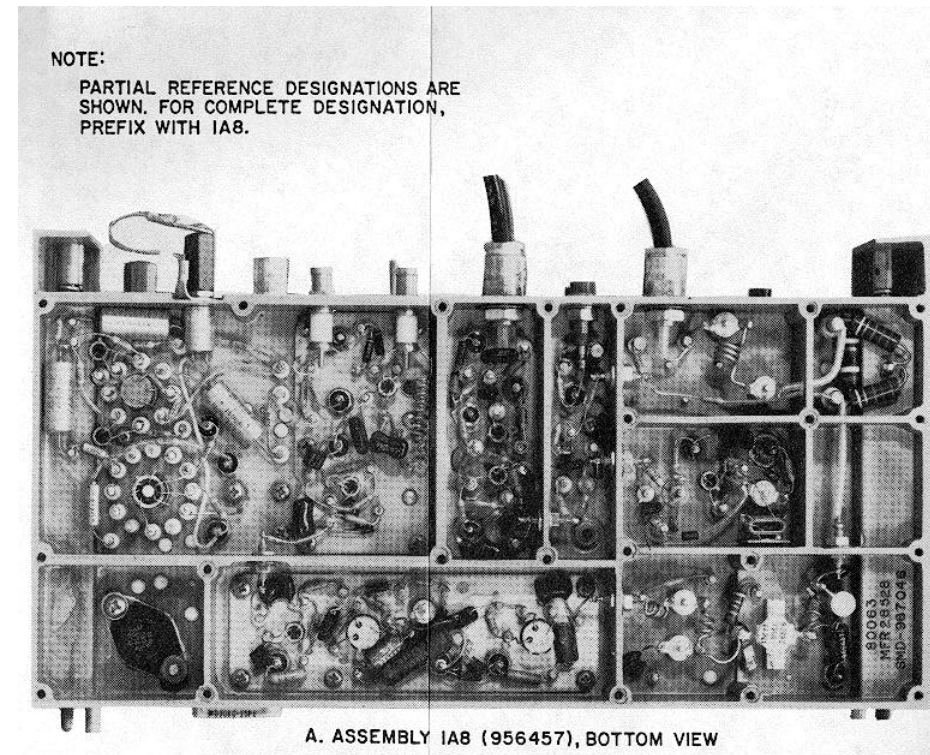
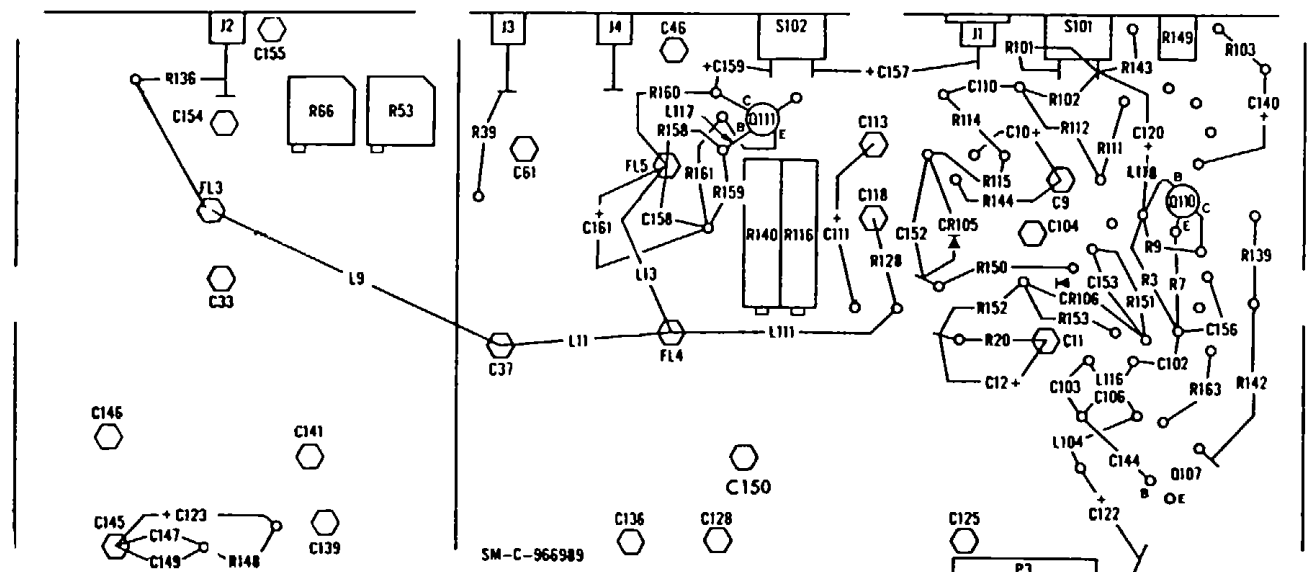


Figure 5-70. Radio transmitter modulator 1A8, parts location.

EL5820-695-35-TM-175



C. REFERENCE DESIGNATIONS OF PARTS ON BOTTOM OF ASSEMBLY IA8



D. REFERENCE DESIGNATIONS OF PARTS ON TOP OF ASSEMBLY IA8

EL2IB107

Figure 5-70.1. Radio transmitter modulator 1A8 (956427), parts location diagram.

NOTES  
 1 PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN FOR COMPLETE  
 DESIGNATION, PREFIX WITH IAS  
 2 FOR SRWBR MODIFICATIONS  
 AI MIXER, CRYSTAL 650527  
 IS LABELED 956891

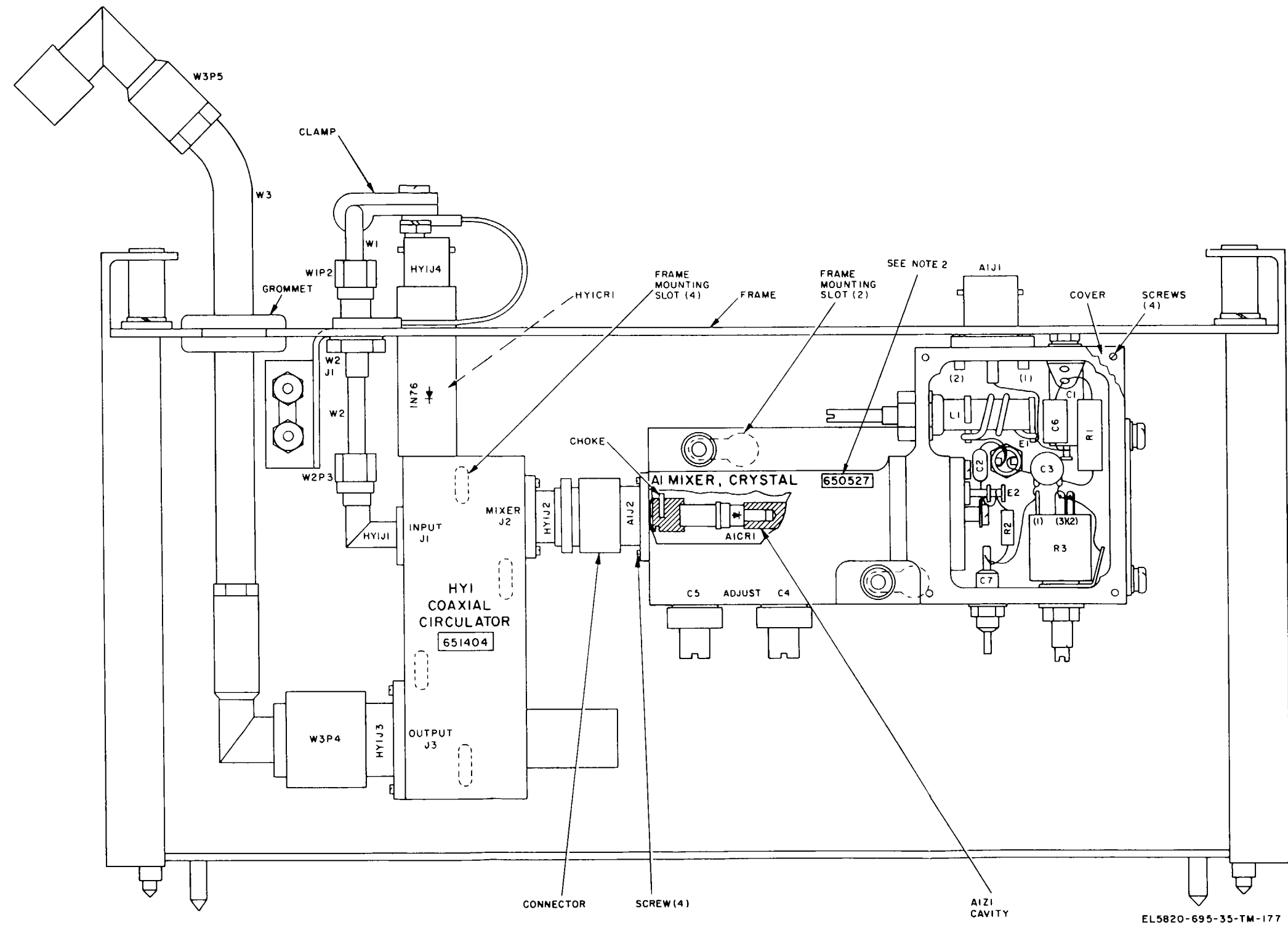
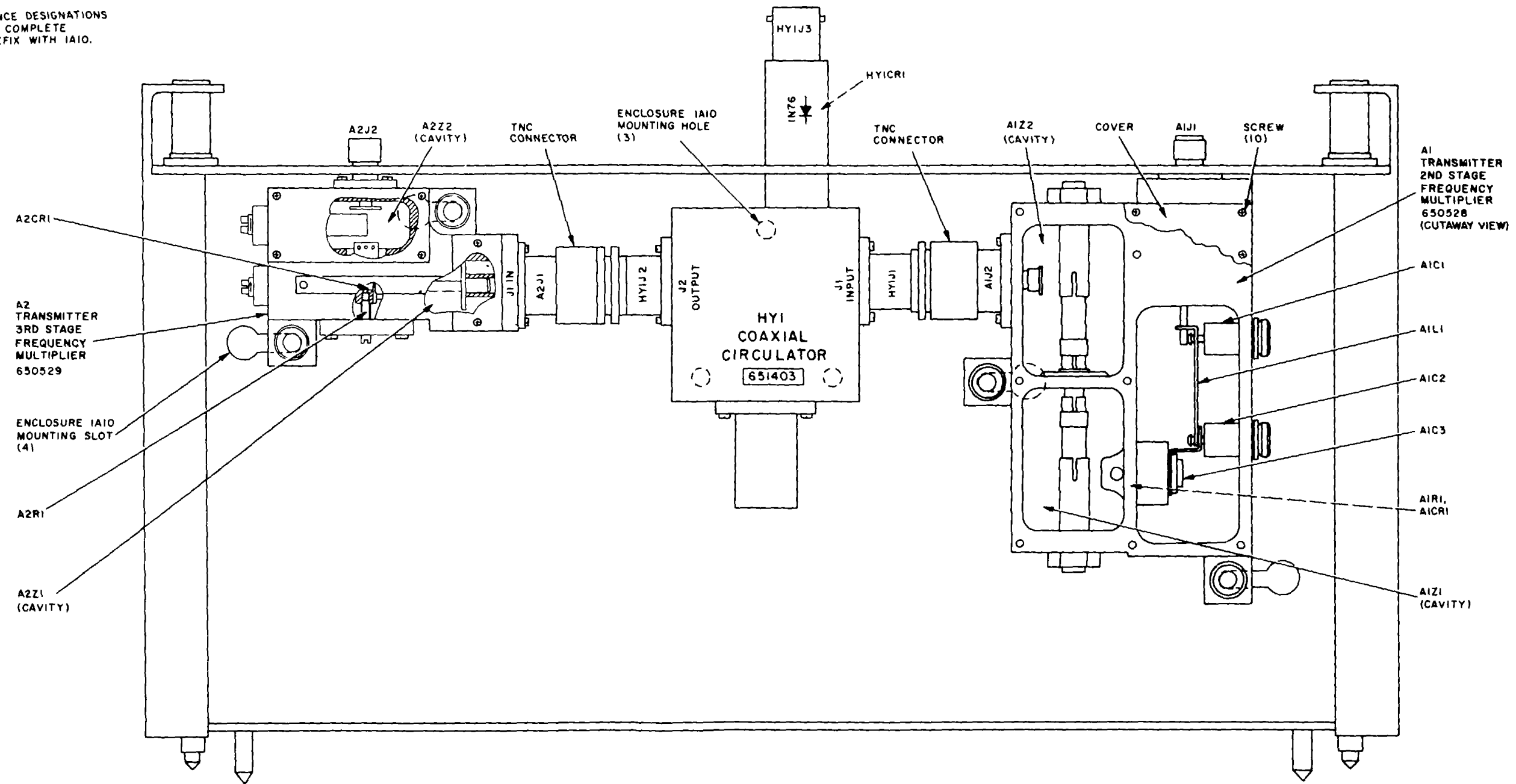


Figure 5-71. Transmitter frequency mixer stage 1A9, parts location.



NOTE  
 PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN FOR COMPLETE  
 DESIGNATION. PREFIX WITH 1A10.



EL5820-695-35-TM-178

Figure 5-72. Transmitter frequency multiplier group 1A10, parts location.

NOTES:  
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH IAI1.  
2. WIRING IS NO 22 AWG STRANDED WIRE TEFLON INSULATED.

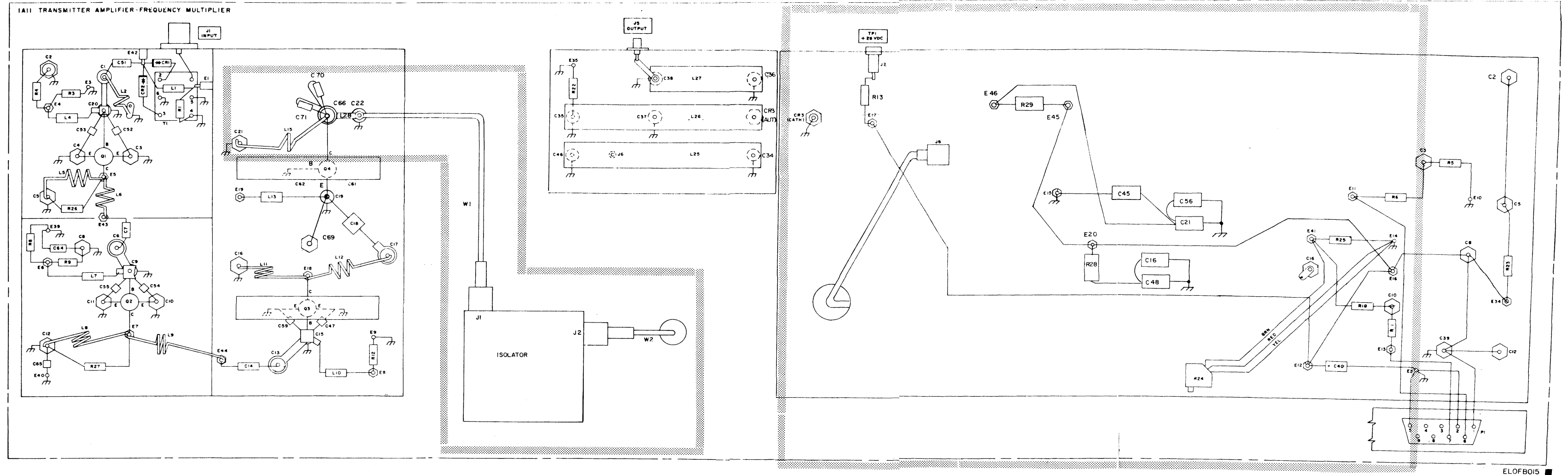


Figure 5-73. Transmitter Amplifier - Frequency Multiplier 1A11, wiring diagram.

Change 5 1-163

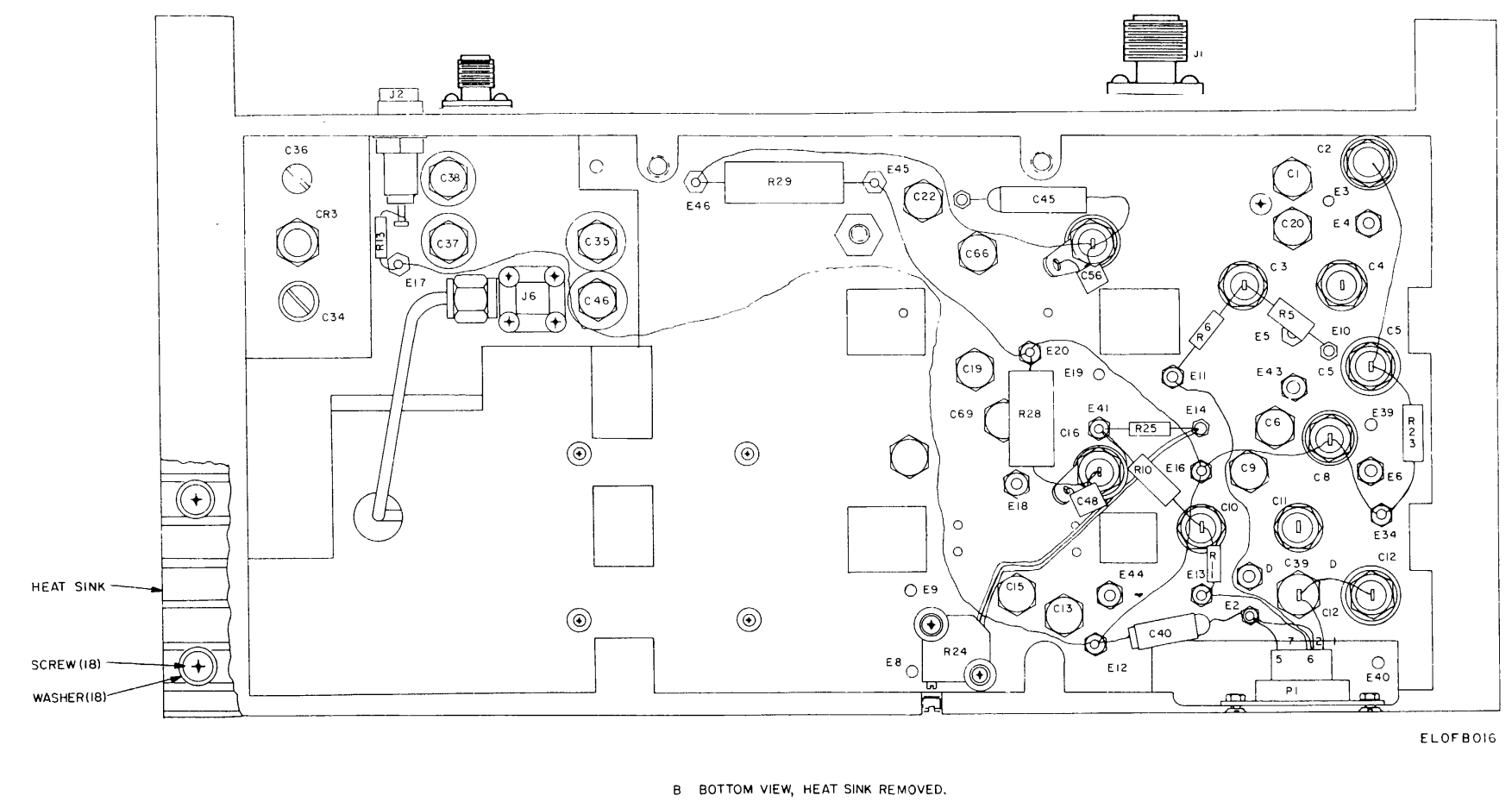
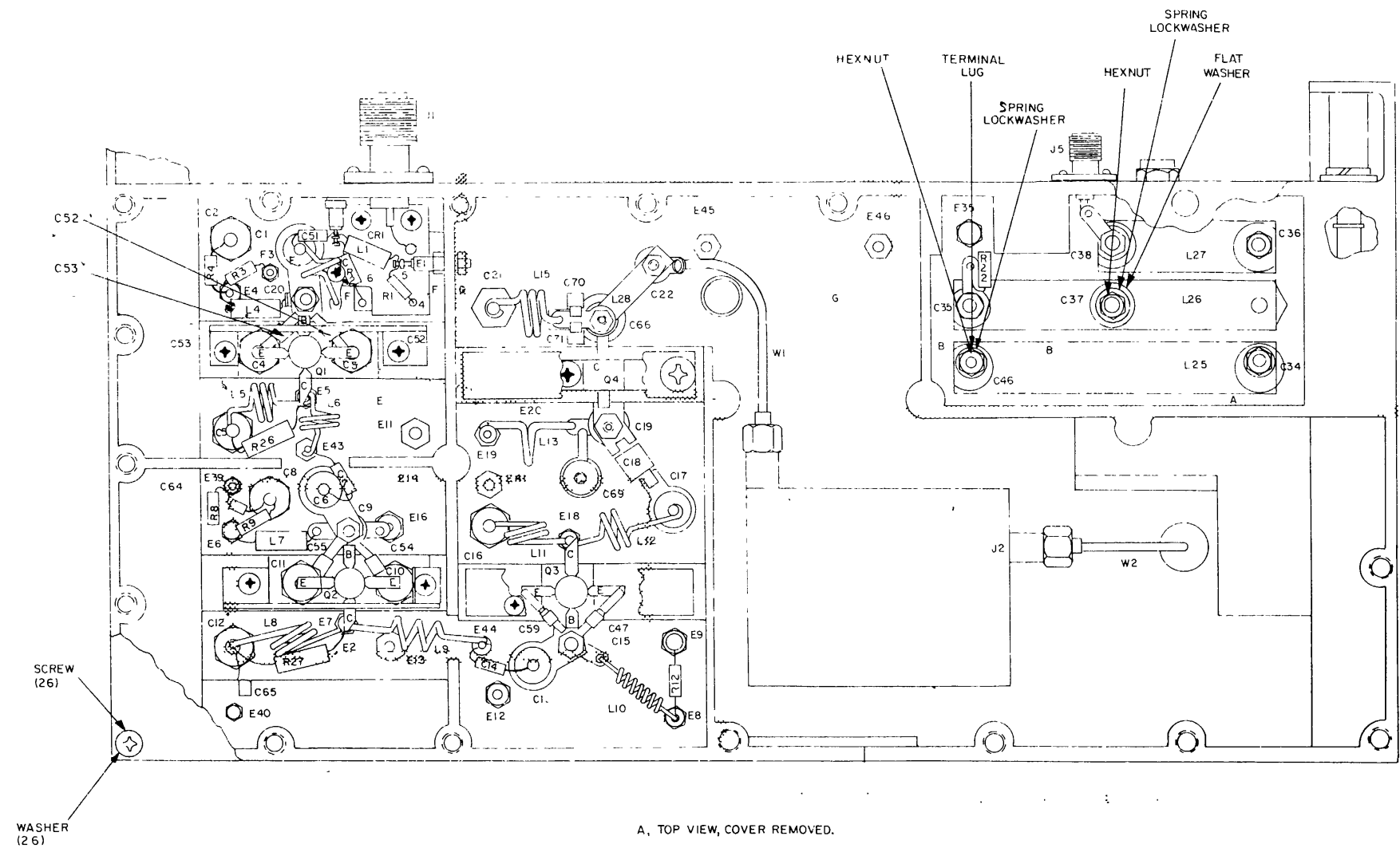
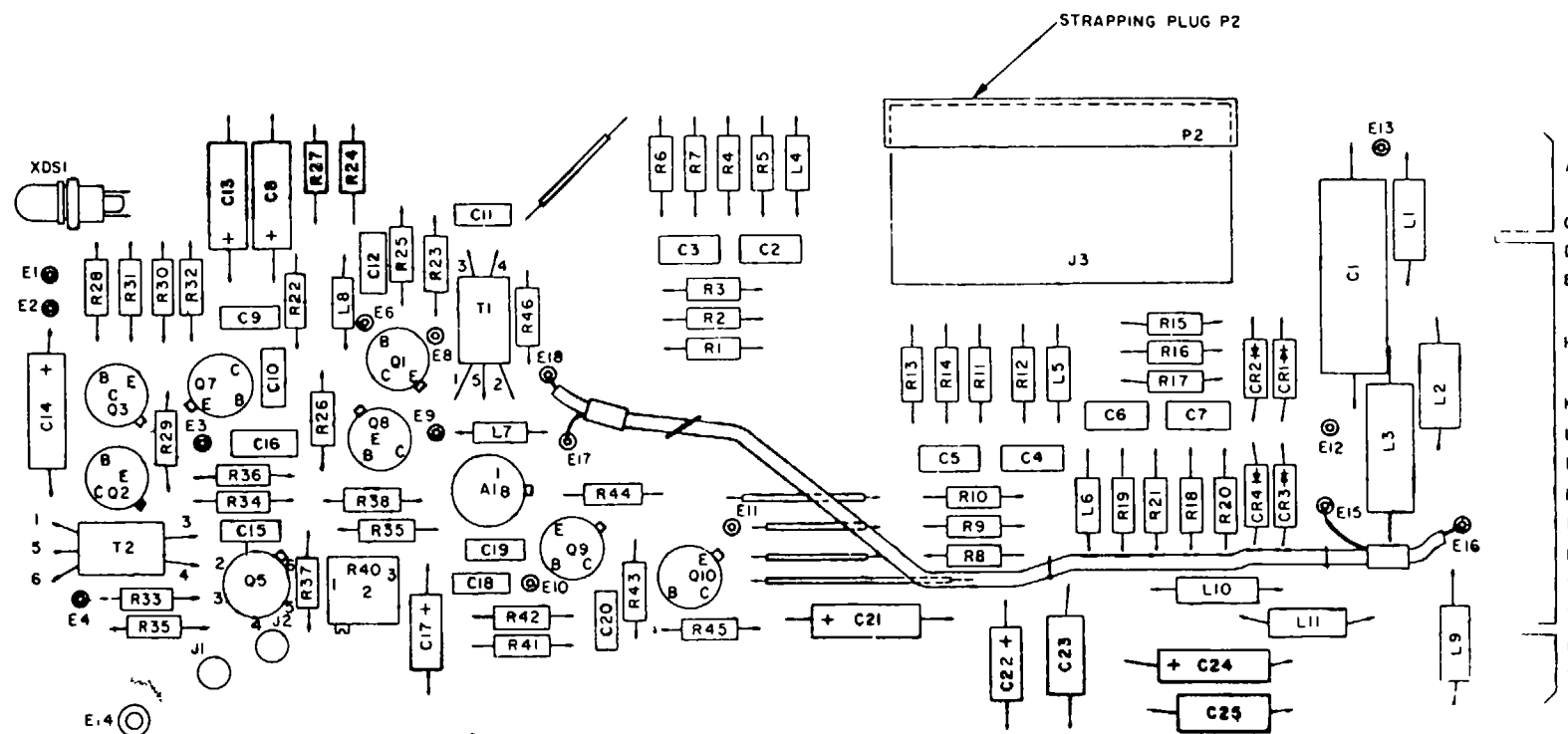


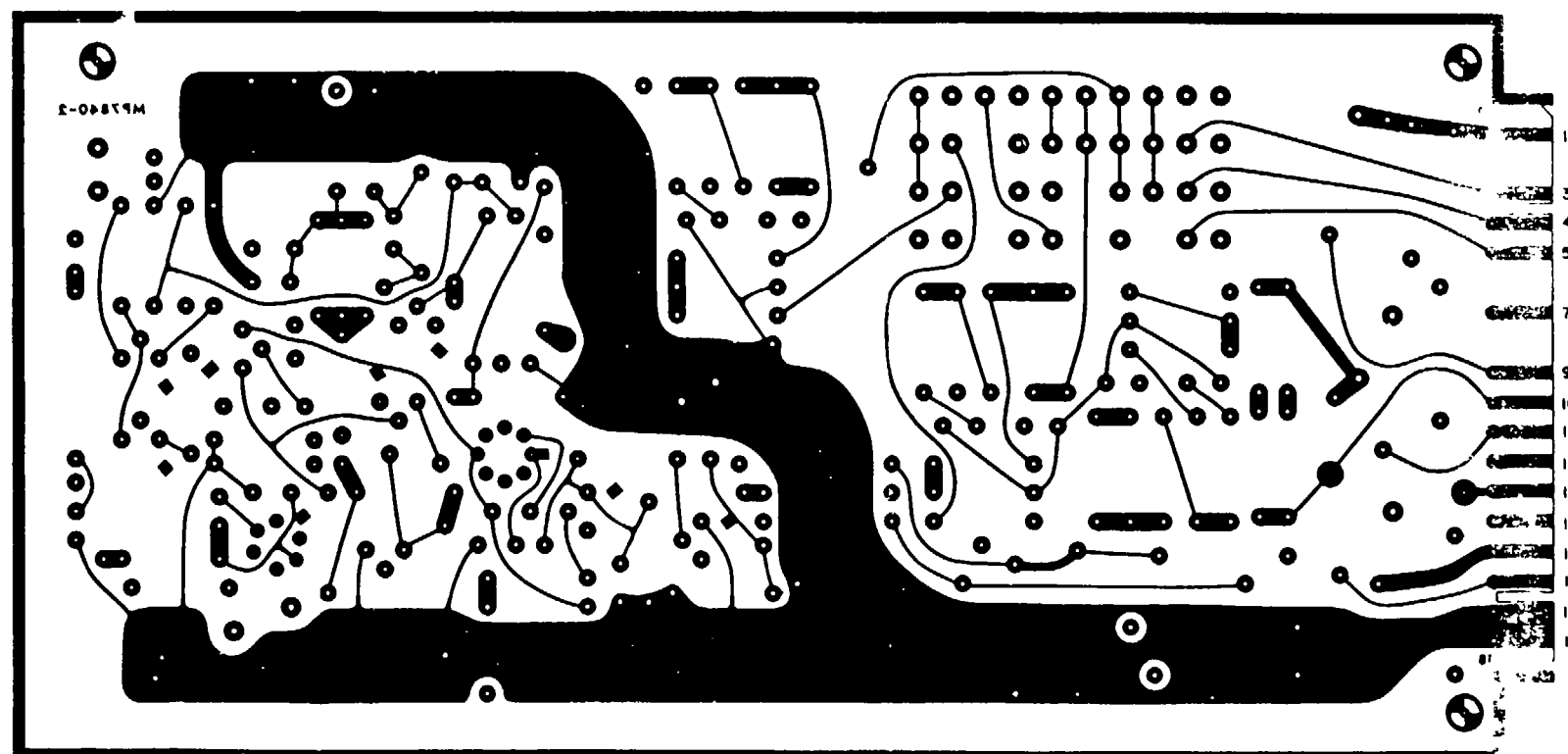
Figure 5-74. Transmitter amplifier-frequency multiplier 1A11, parts location.

Change 5 5-165

NOTE  
 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN  
 FOR COMPLETE DESIGNATION, PREFIX WITH 1A12A2



A. PARTS AND WIRING ON FRONT OF BOARD 1A12A2 (650539)

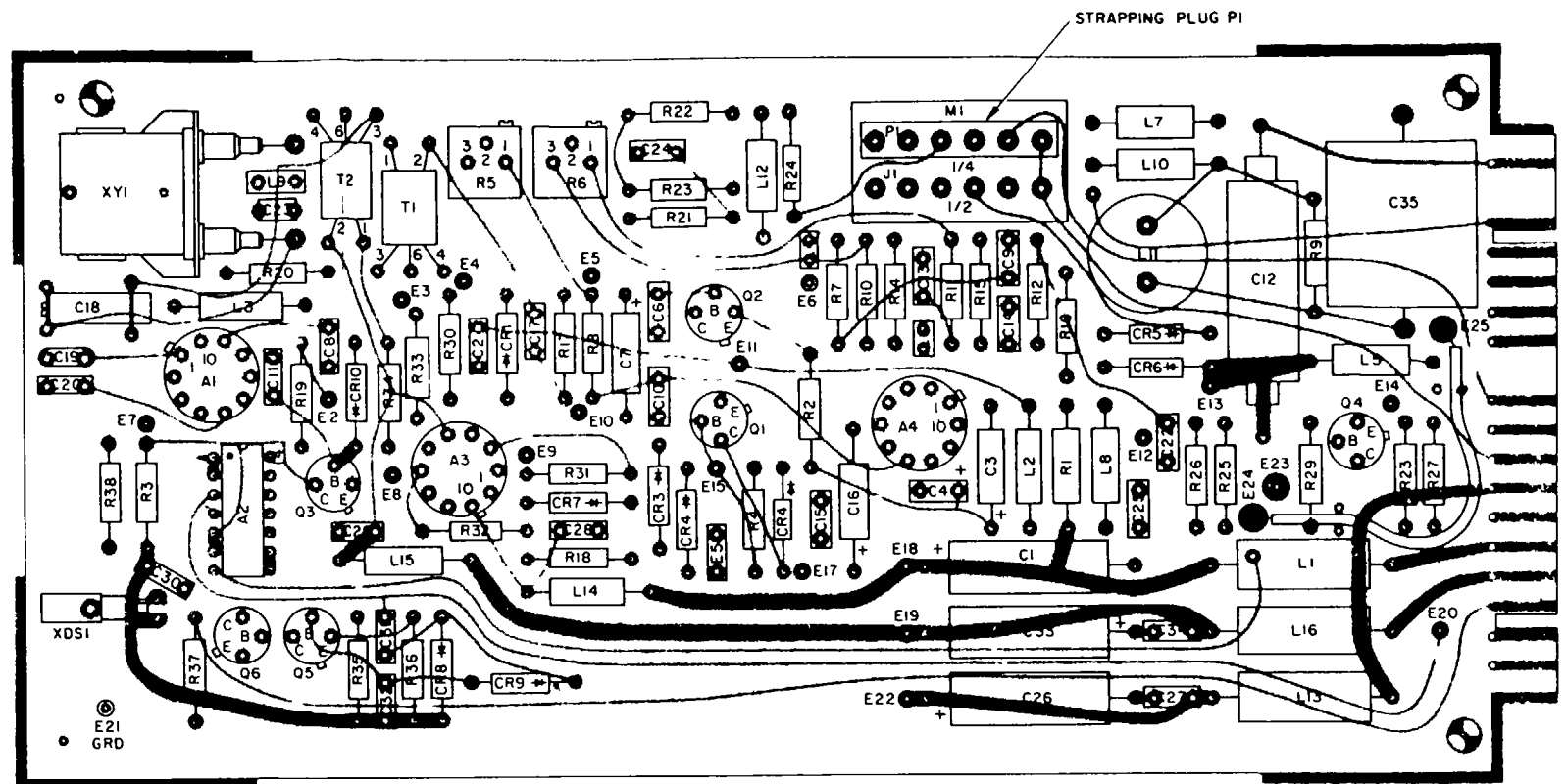


B. WIRING ON BACK OF BOARD 1A12A2 (VIEWED THROUGH FRONT).

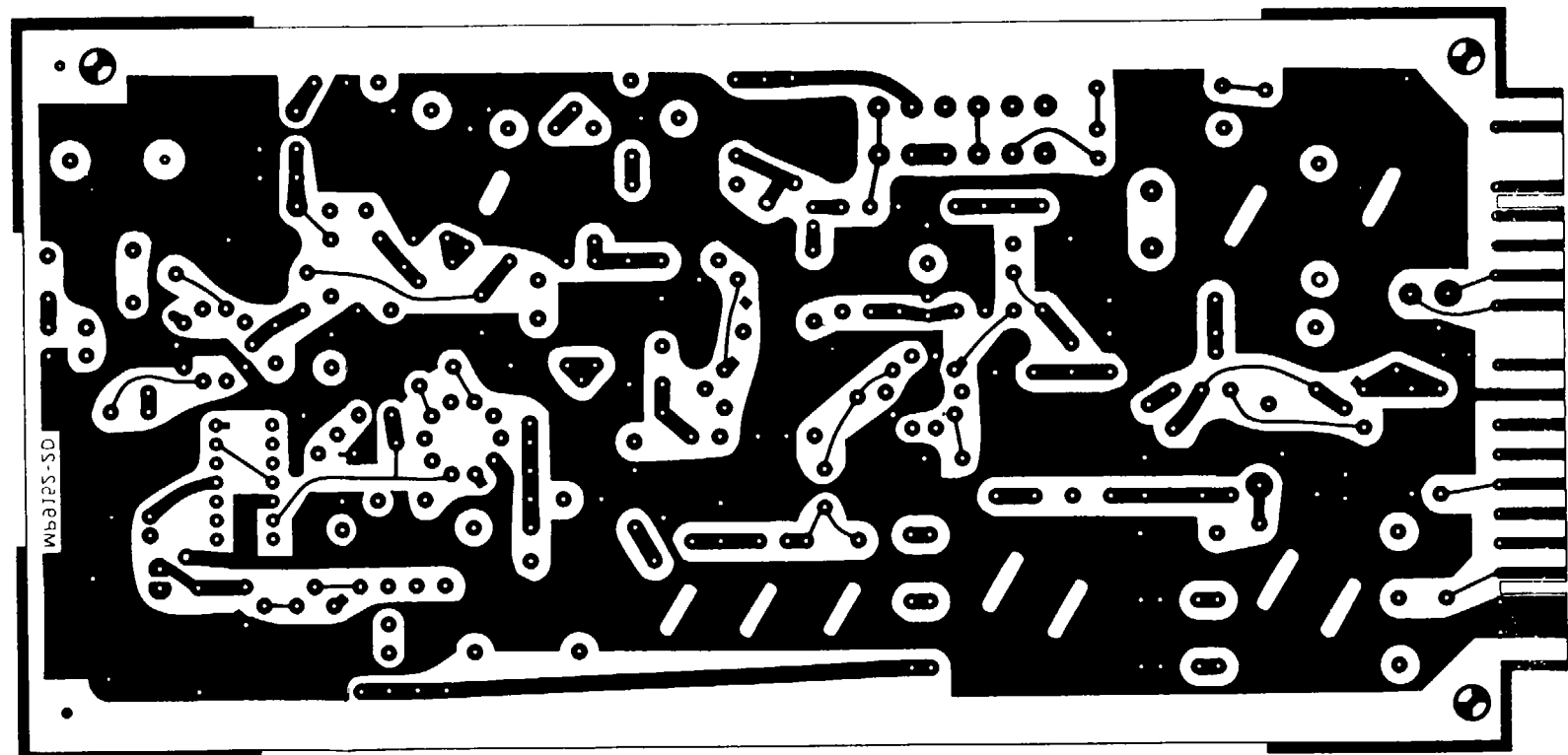
EL5820-695 35 186

Figure 5-75. Cable digital regenerator 1A12A2, parts location and printed wiring diagram, synchronous mode.  
 Change 2 5-167

NOTE  
 PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN FOR COMPLETE  
 DESIGNATION, PREFIX WITH 1A12A13



A PARTS AND WIRING ON FRONT OF BOARD AI3(684089)

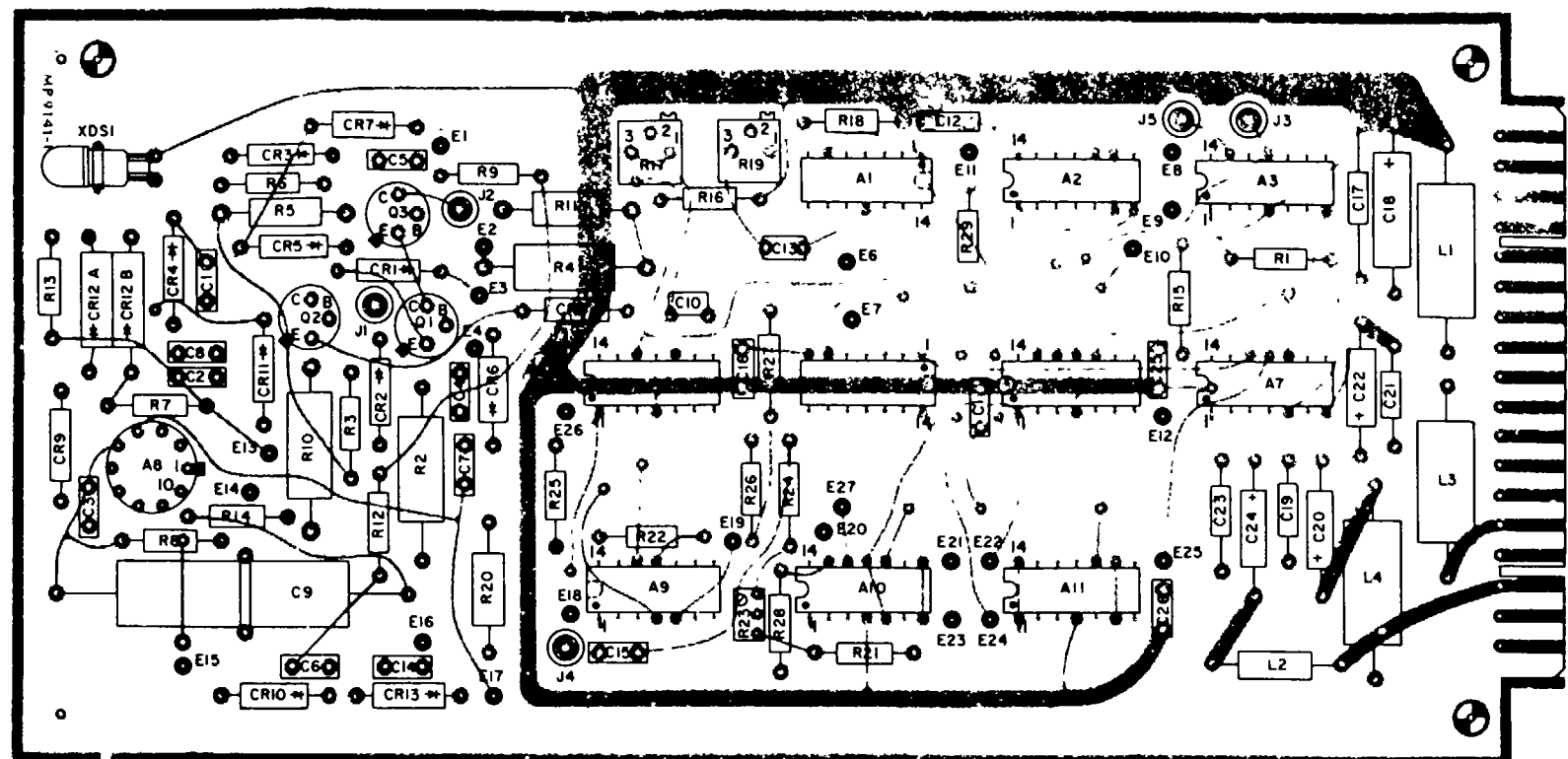


B WIRING ON BACK OF BOARD AI3 (VIEWED THROUGH FRONT)

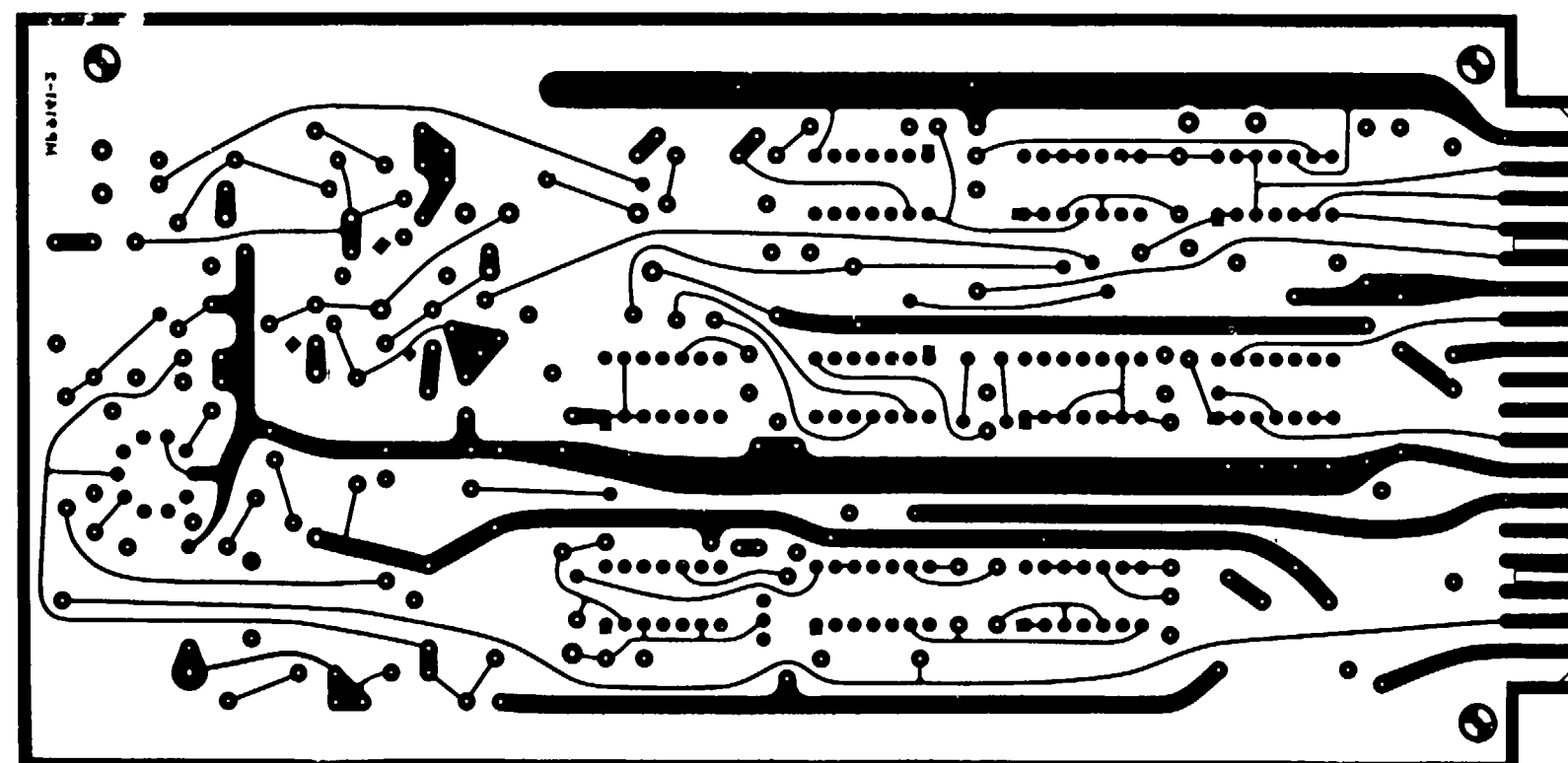
EL5820-695-35-C2-TM-9

Figure 5-75.1. Cable digital regenerator 1A12A13, parts location and printed wiring diagram, asynchronous mode.

NOTE  
 PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN FOR COMPLETE  
 DESIGNATION, PREFIX WITH 1A12A3.



A PARTS AND WIRING ON FRONT OF BOARD 1A12A3 (683689)

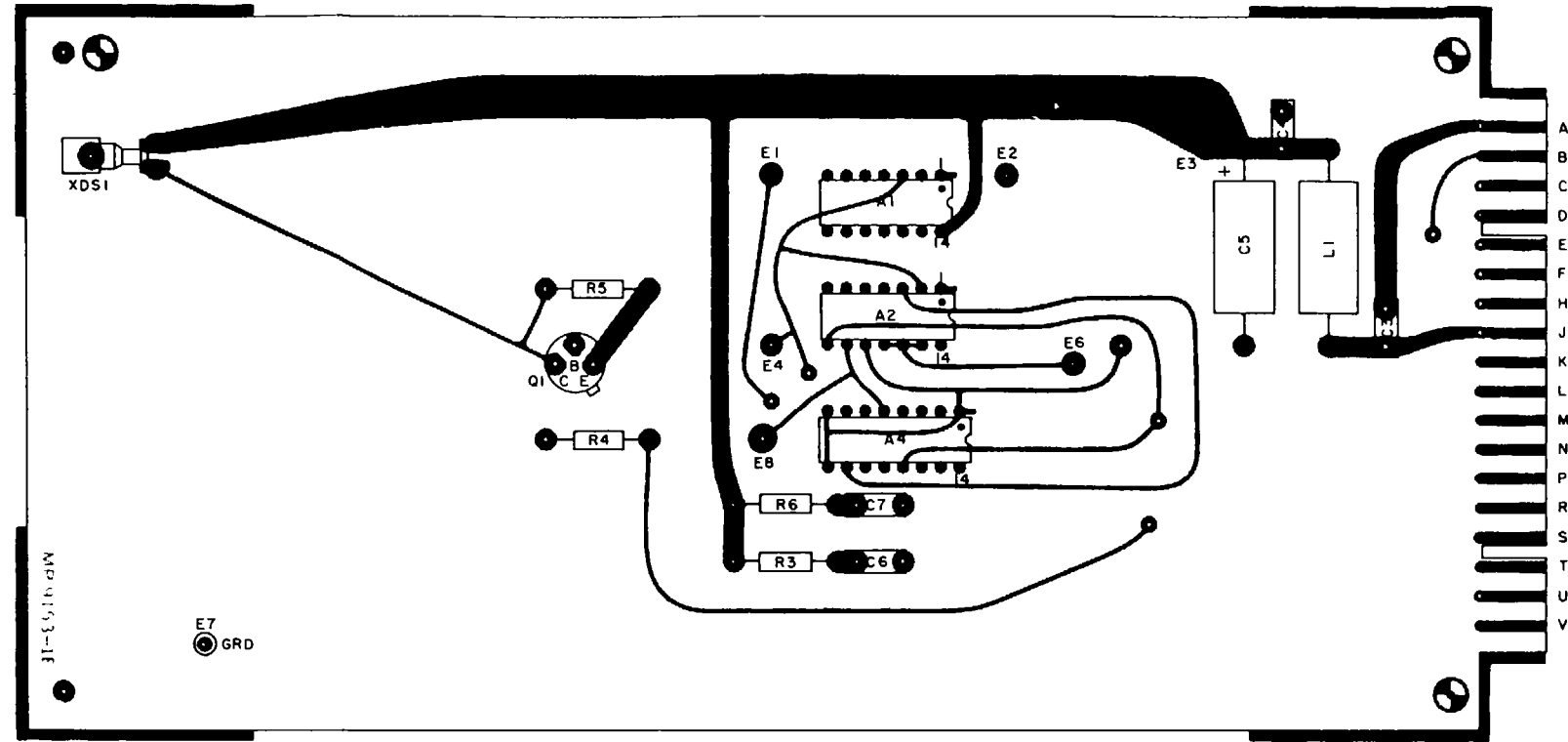


B. WIRING ON BACK OF BOARD 1A12A3 (VIEWED THROUGH FRONT).

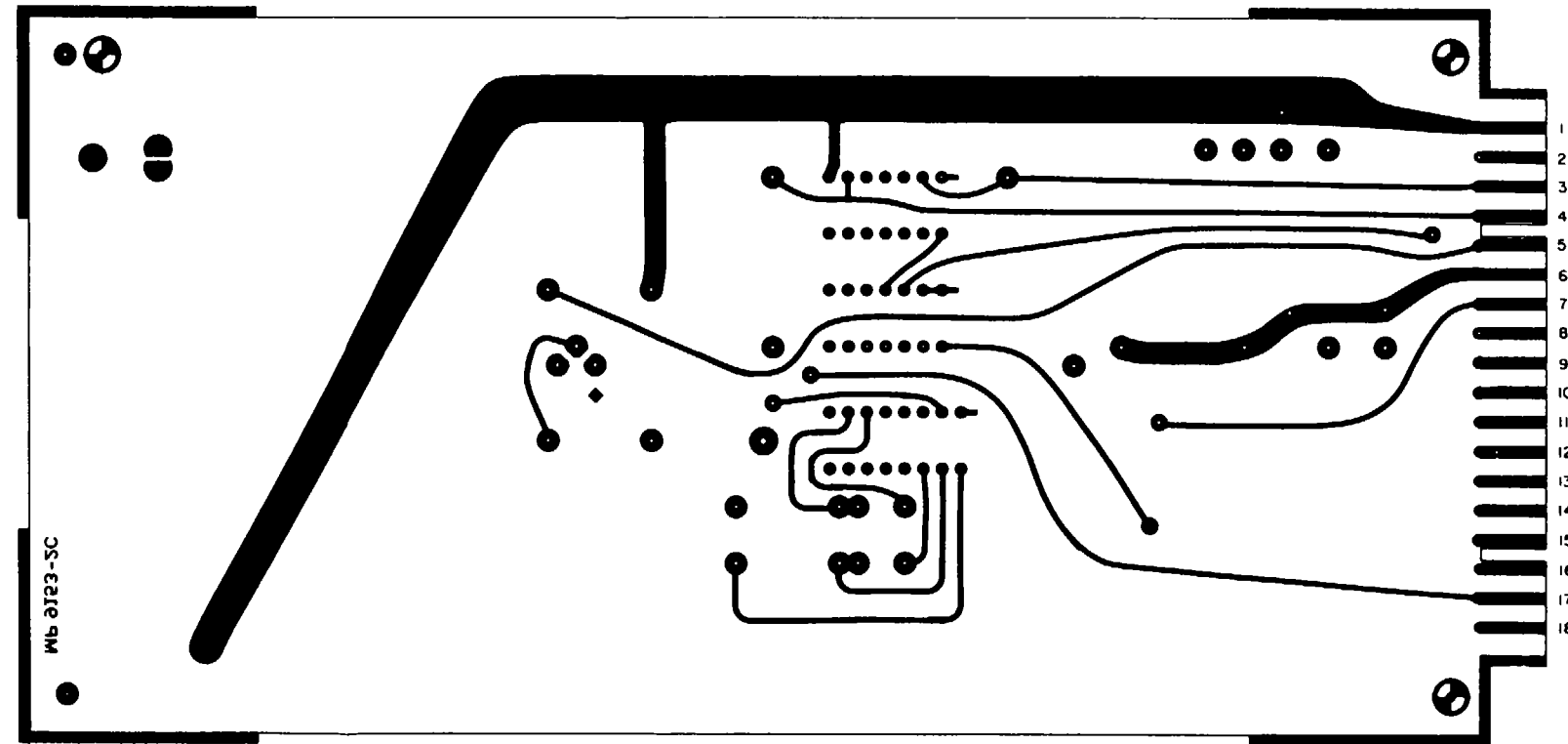
EL5820-695-35-TM-187

Figure 5-76. Cable control-comparator 1A12A3, parts location and printed wiring diagram, synchronous mode.

NOTE  
 PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN FOR COMPLETE  
 DESIGNATION, PREFIX WITH 1A12A14



A PARTS AND WIRING ON FRONT OF BOARD A14 (684090)

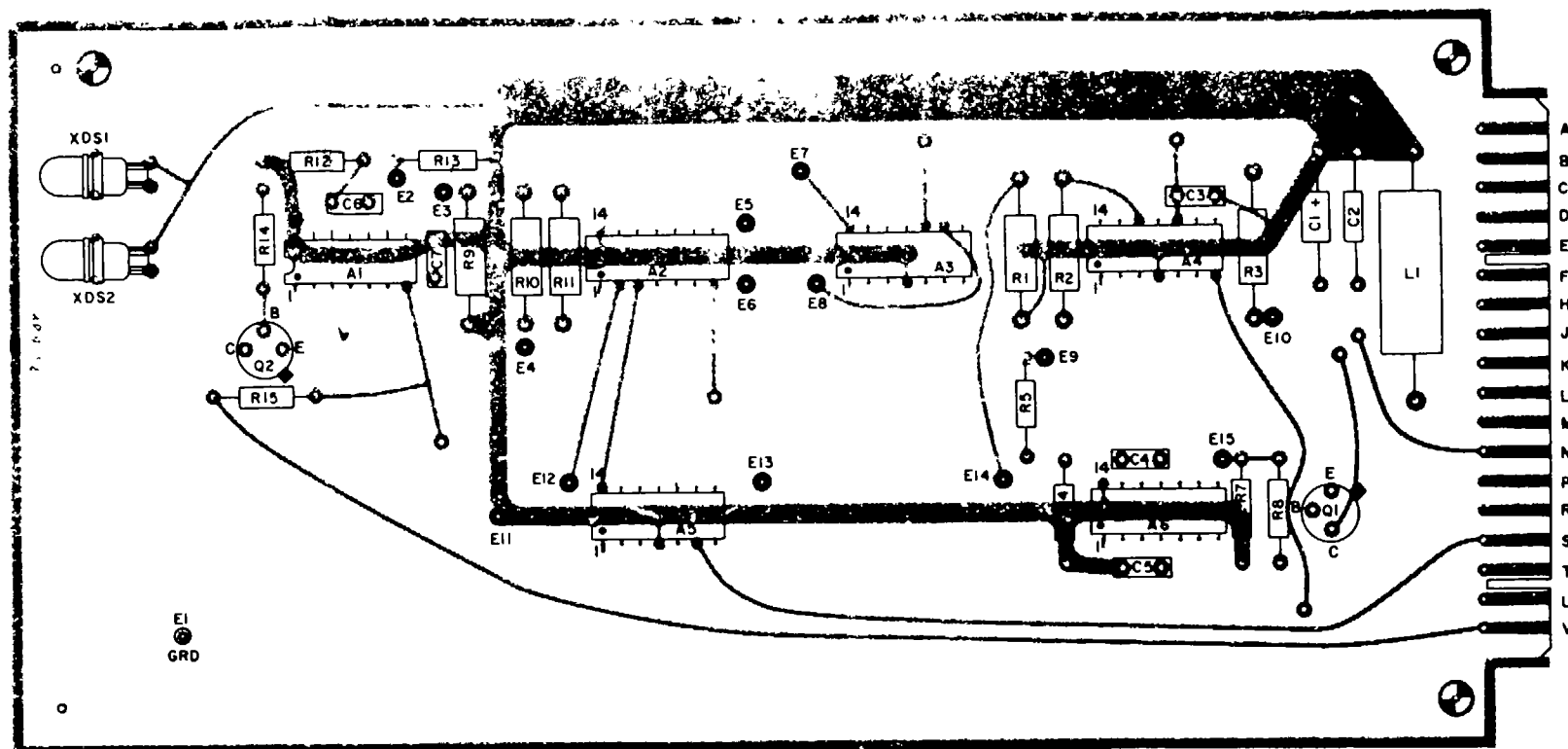


B WIRING ON BACK OF BOARD A14 (VIEWED THROUGH FRONT)

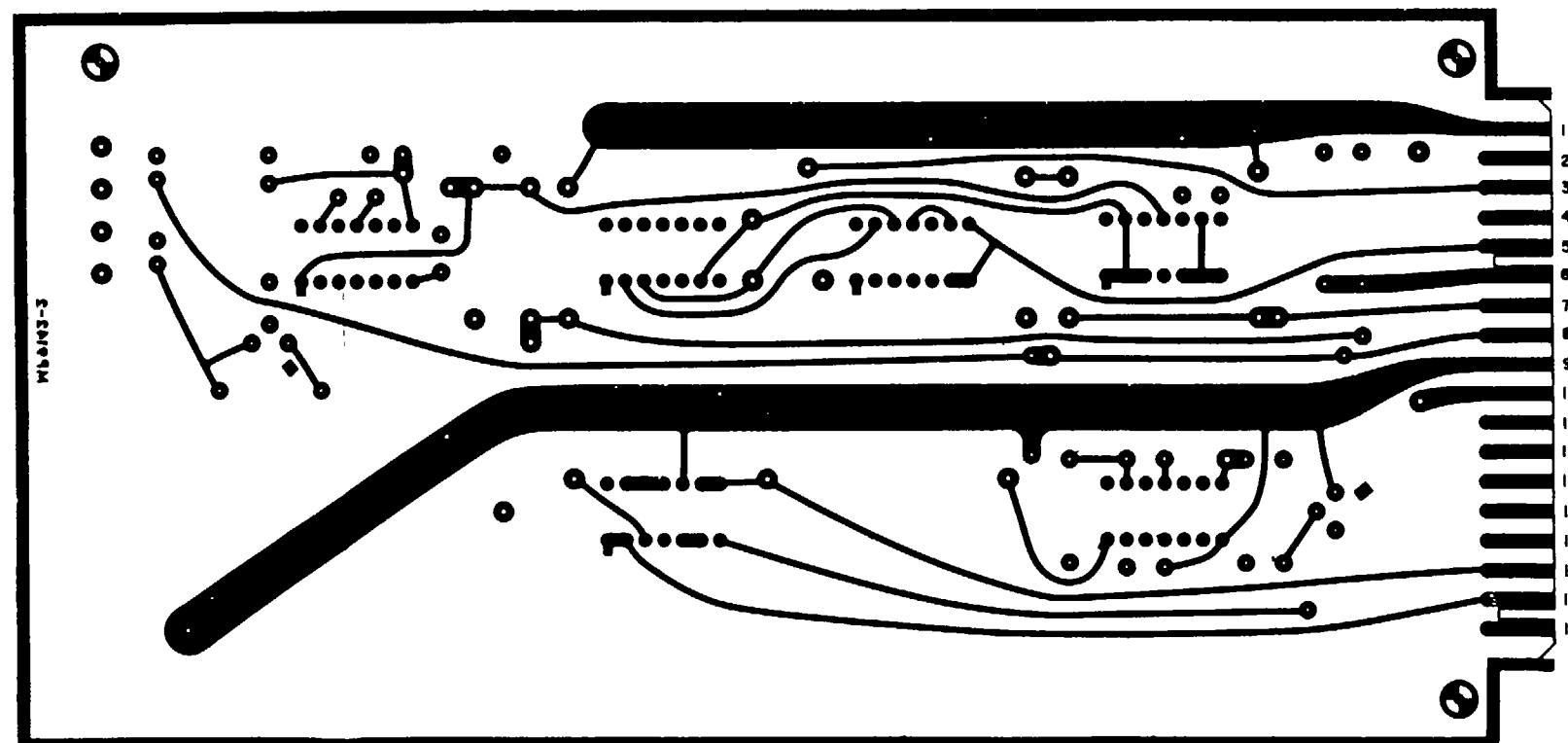
EL5820-695-35-C2-TM-10

Figure 5-76.1. Cable control comparator 1A12A14, parts location and printed wiring diagram, asynchronous mode.

NOTE  
 PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN FOR COMPLETE  
 DESIGNATION, PREFIX WITH 1A12A4



A PARTS AND WIRING ON FRONT OF BOARD 1A12A4 (683690)



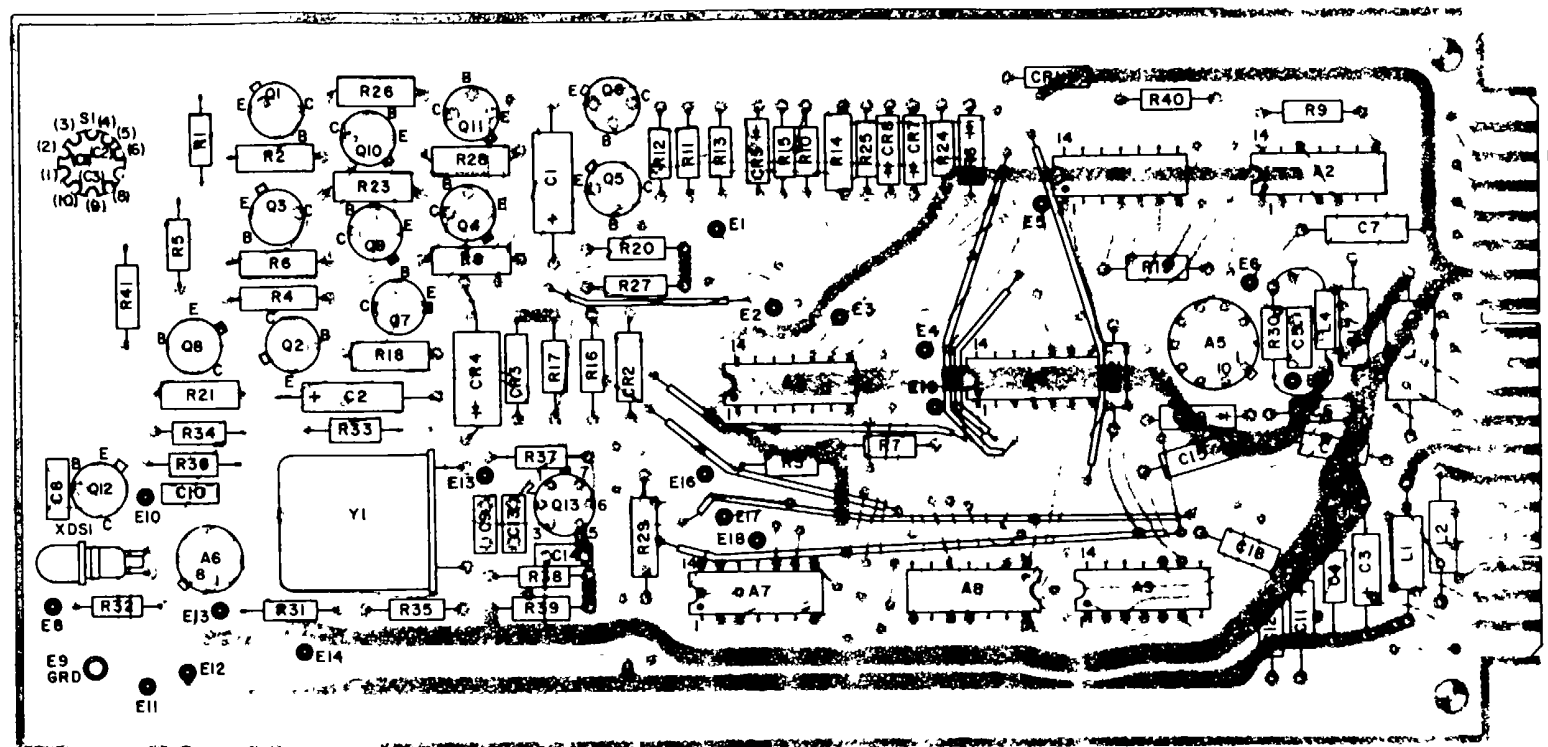
B. WIRING ON BACK OF BOARD 1A12A4 (VIEWED THROUGH FRONT).

EL5820-695-35-TM-188

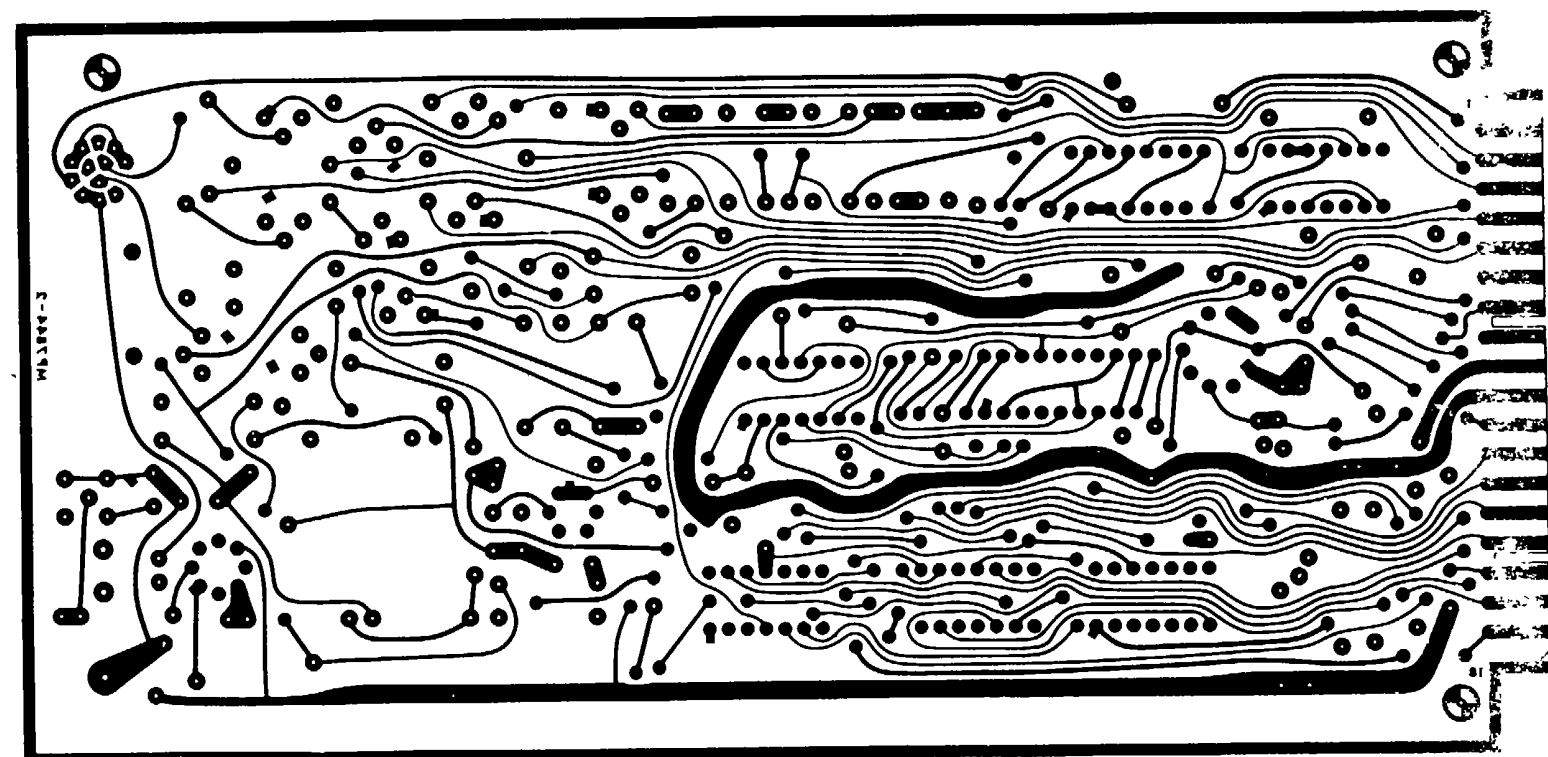
Figure 5-77. Cable digital processor 1A12A4 parts location and printed wiring diagram.



NOTE.  
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.  
FOR COMPLETE DESIGNATION, PREFIX WITH 1A12A5



A. PARTS AND WIRING ON FRONT OF BOARD 1A12A5 (650545)

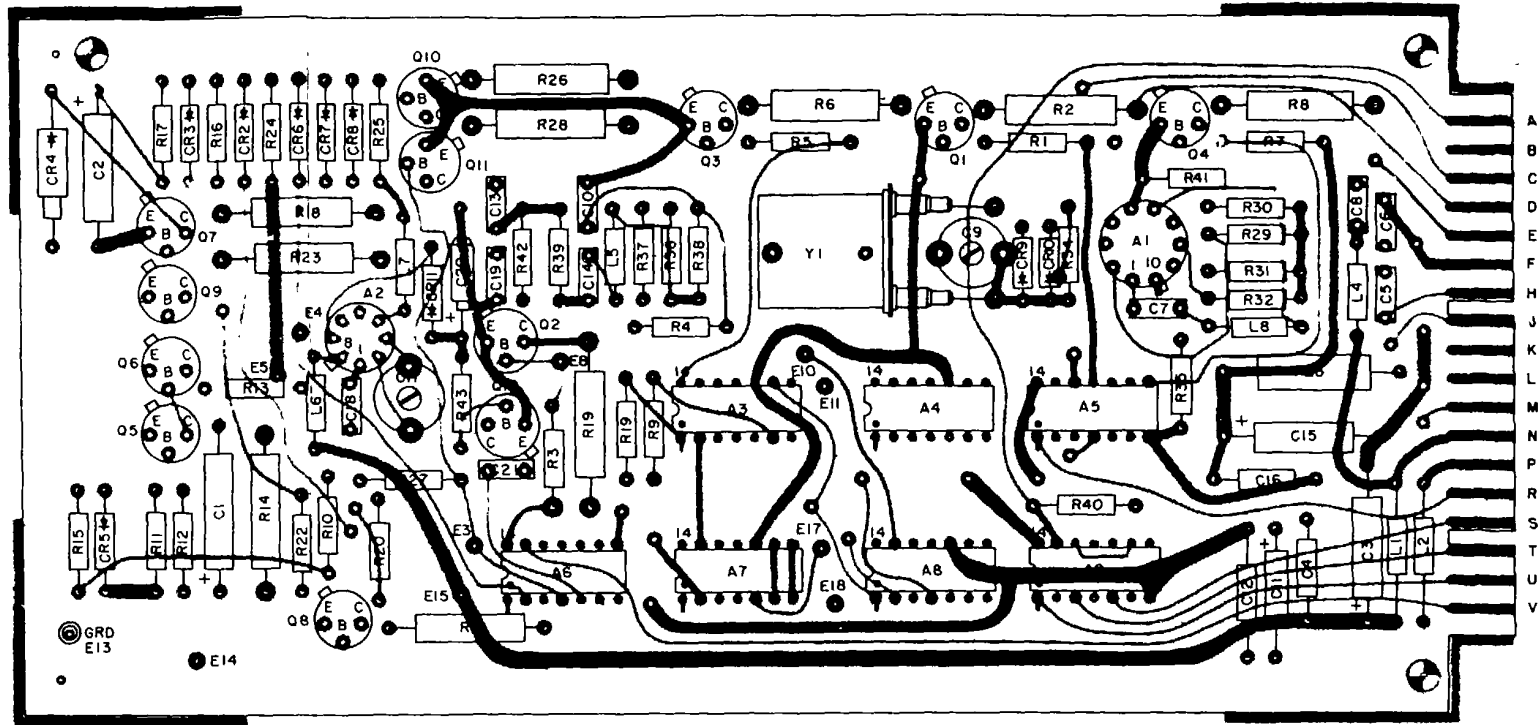


B. WIRING ON BACK OF BOARD 1A12A5 (VIEWED THROUGH FRONT)

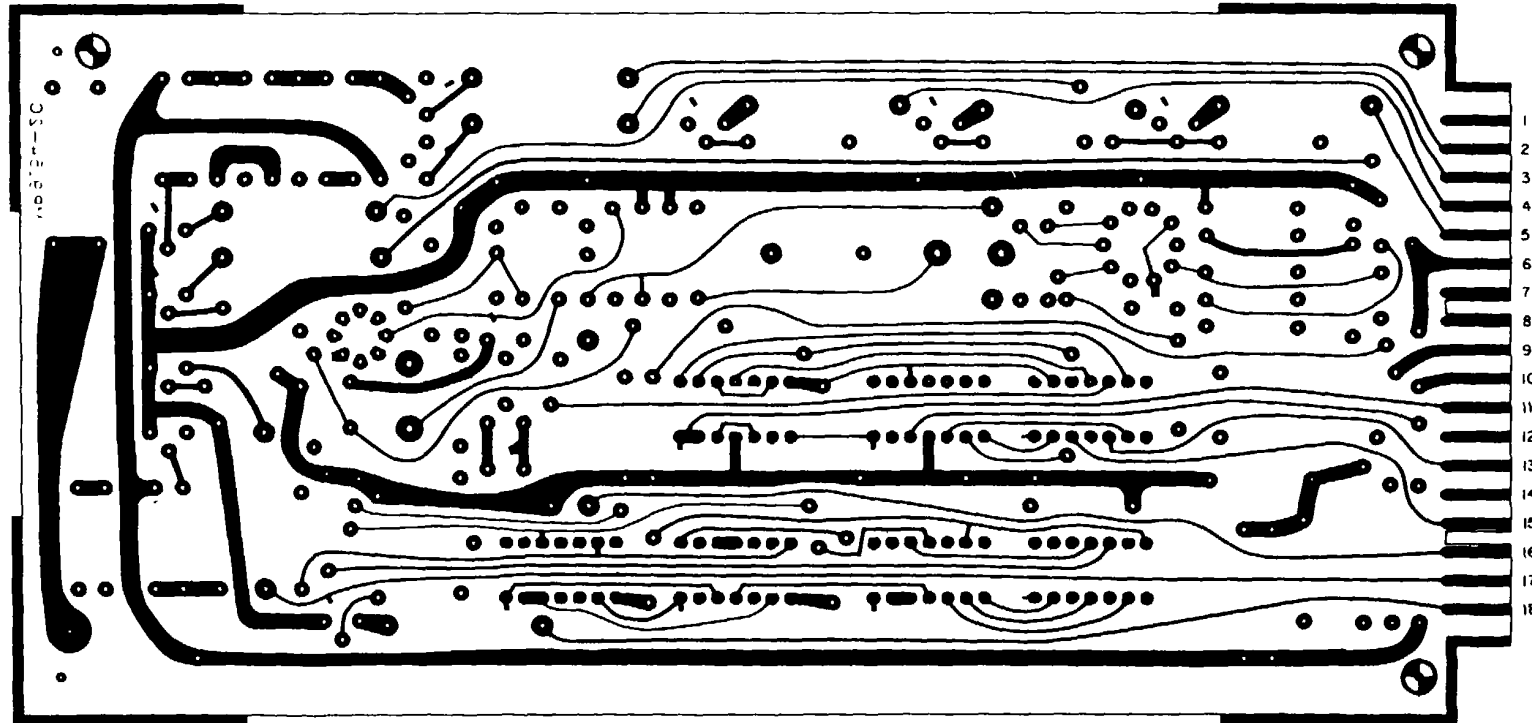
EL5820-695-35-41

Figure 5-78. Alarm monitor 1A12A5, parts location and printed wiring diagram, synchronous mode.

NOTE  
 PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN FOR COMPLETE  
 DESIGNATION, PREFIX WITH 1A12A15



A PARTS AND WIRING ON FRONT OF BOARD AI5 (684091)

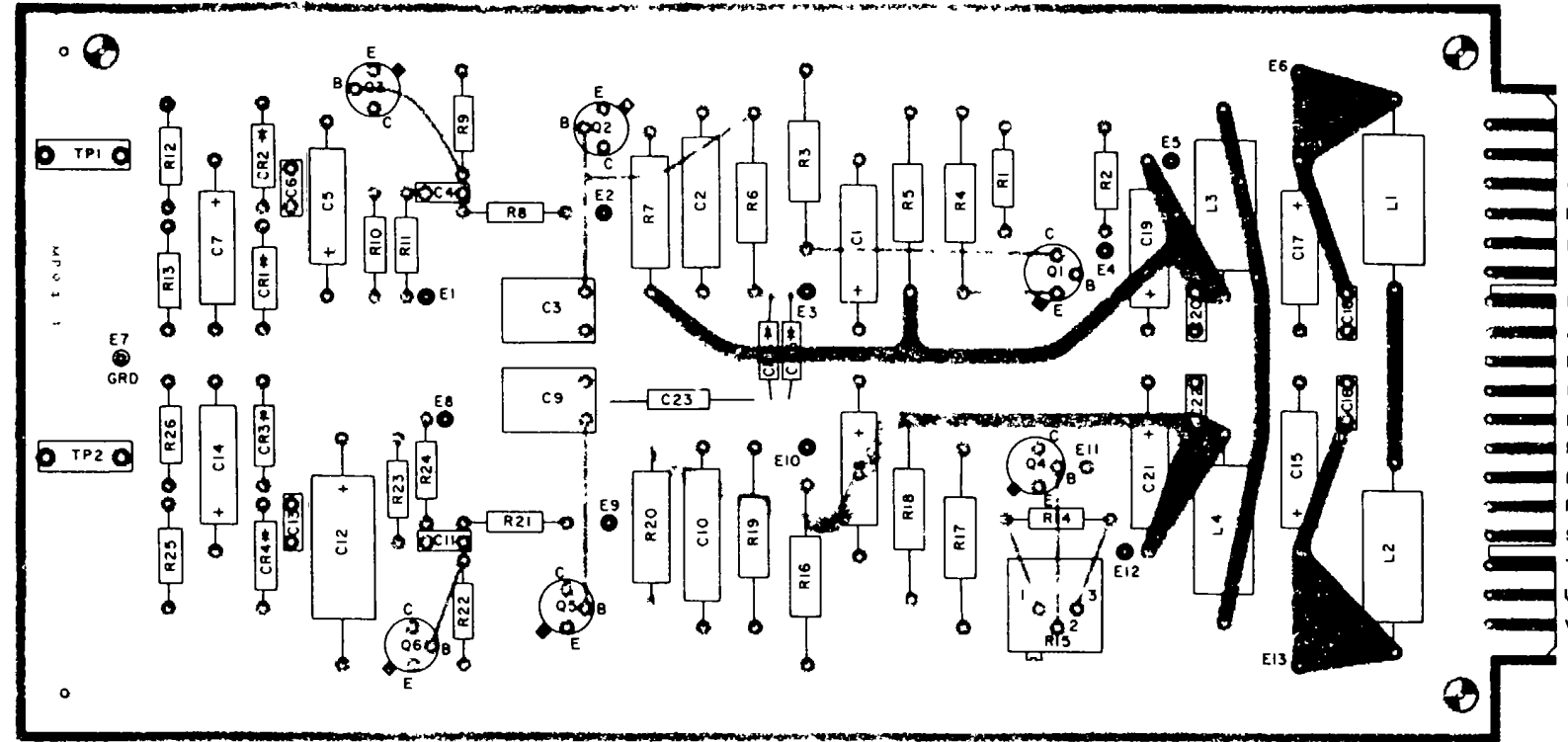


B WIRING ON BACK OF BOARD AI5 (VIEWED THROUGH FRONT)

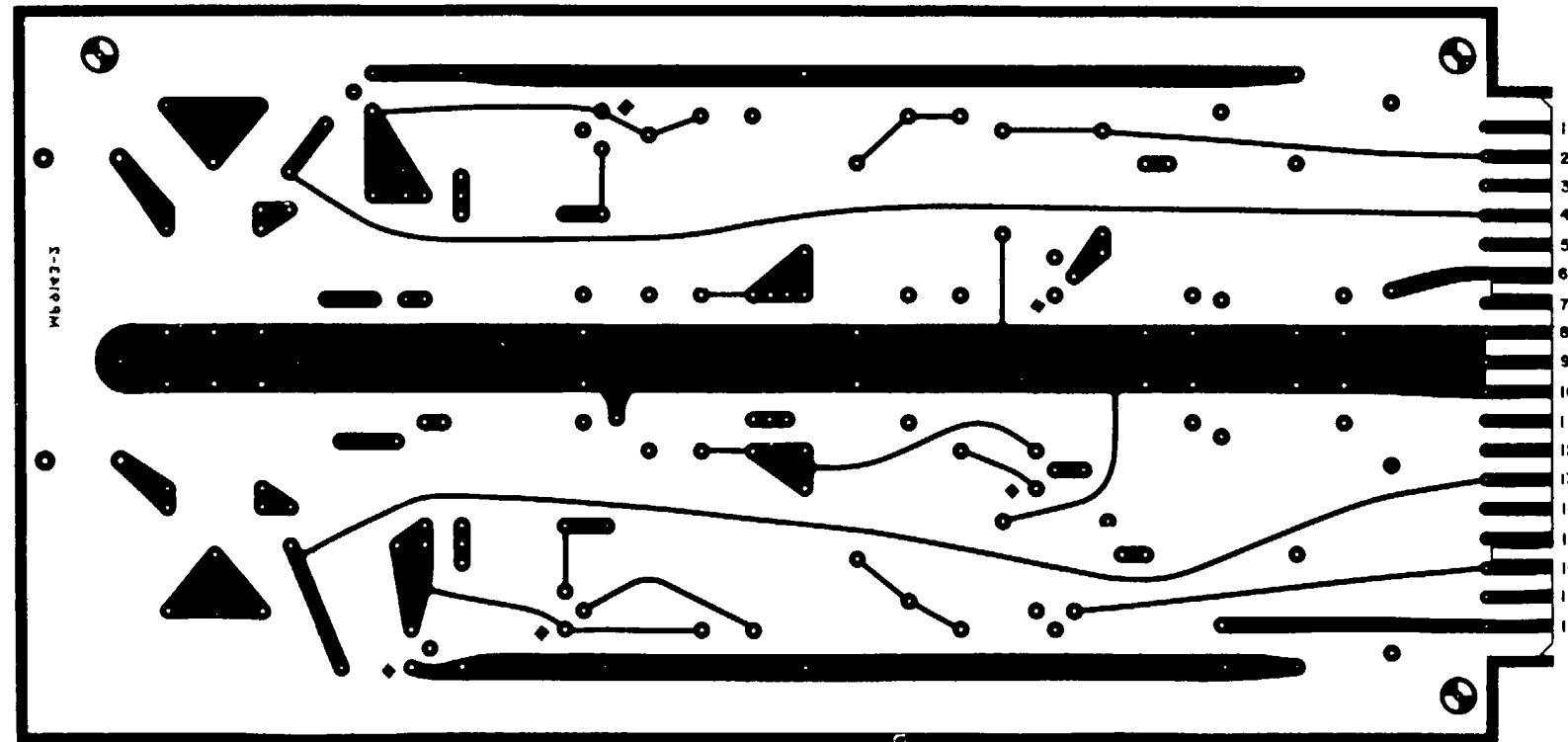
EL5820-695-35-C2-TM-11

Figure 5-78.1. Alarm monitor 1A12A5, parts location and printed wiring diagram, synchronous mode.

NOTE  
 PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN FOR COMPLETE  
 DESIGNATION, PREFIX WITH 1A12A6



A. PARTS AND WIRING ON FRONT OF BOARD 1A12A6 (683691)

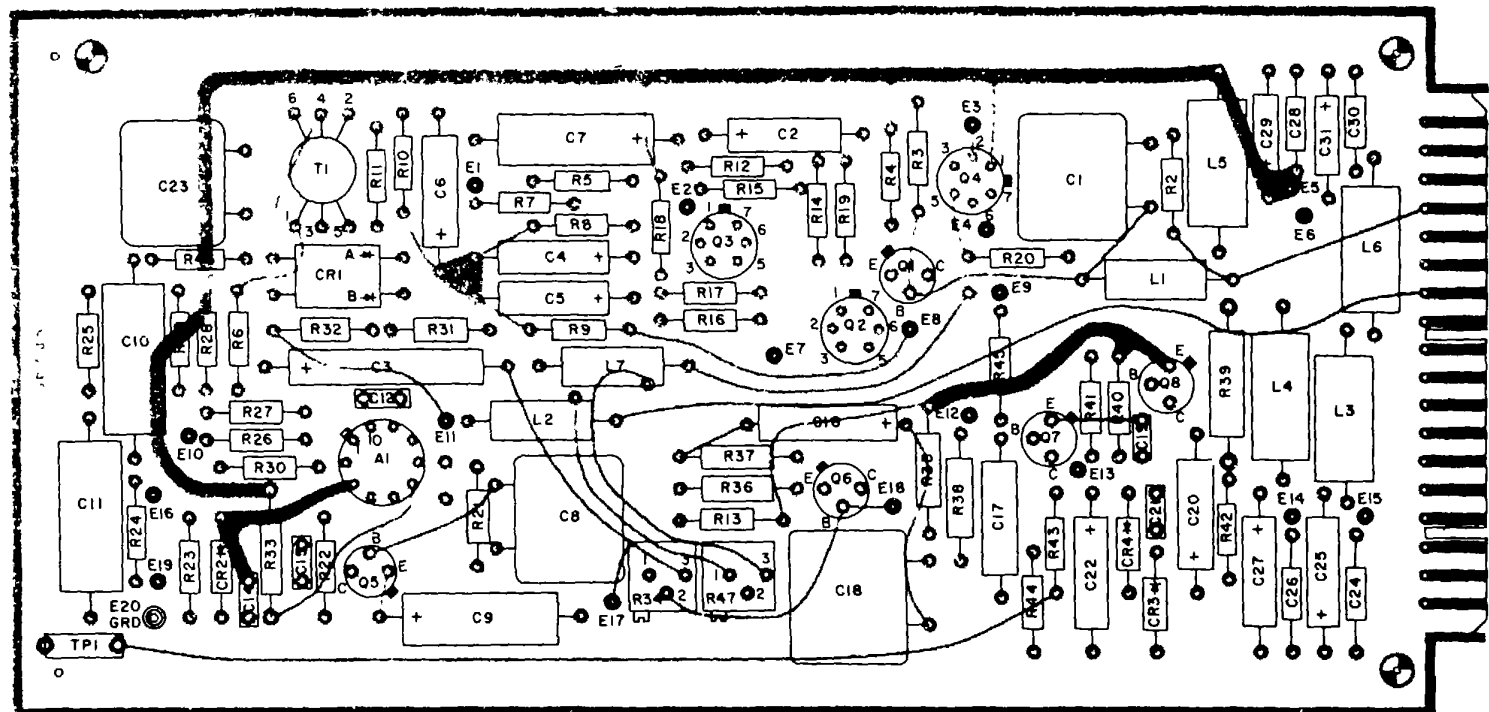


B. WIRING ON BACK OF BOARD 1A12A6 (VIEWED THROUGH FRONT)

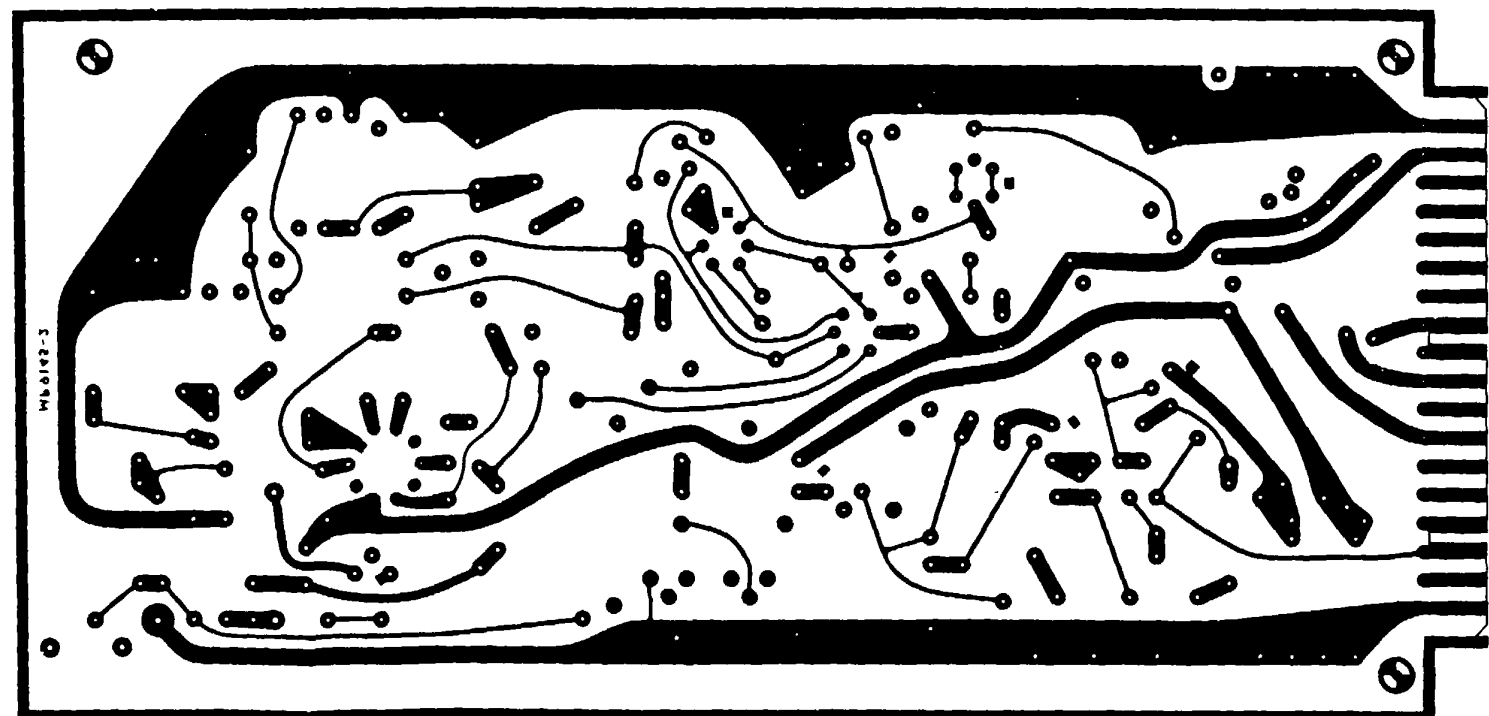
EL5820-695-35-TM-CI-42

Figure 5-79. Af amplifier 1A12A5, parts location and printed wiring diagram.

NOTE  
 PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN FOR COMPLETE  
 DESIGNATION, PREFIX WITH 1A12A7



A PARTS AND WIRING ON FRONT OF BOARD 1A12A7 (683693)

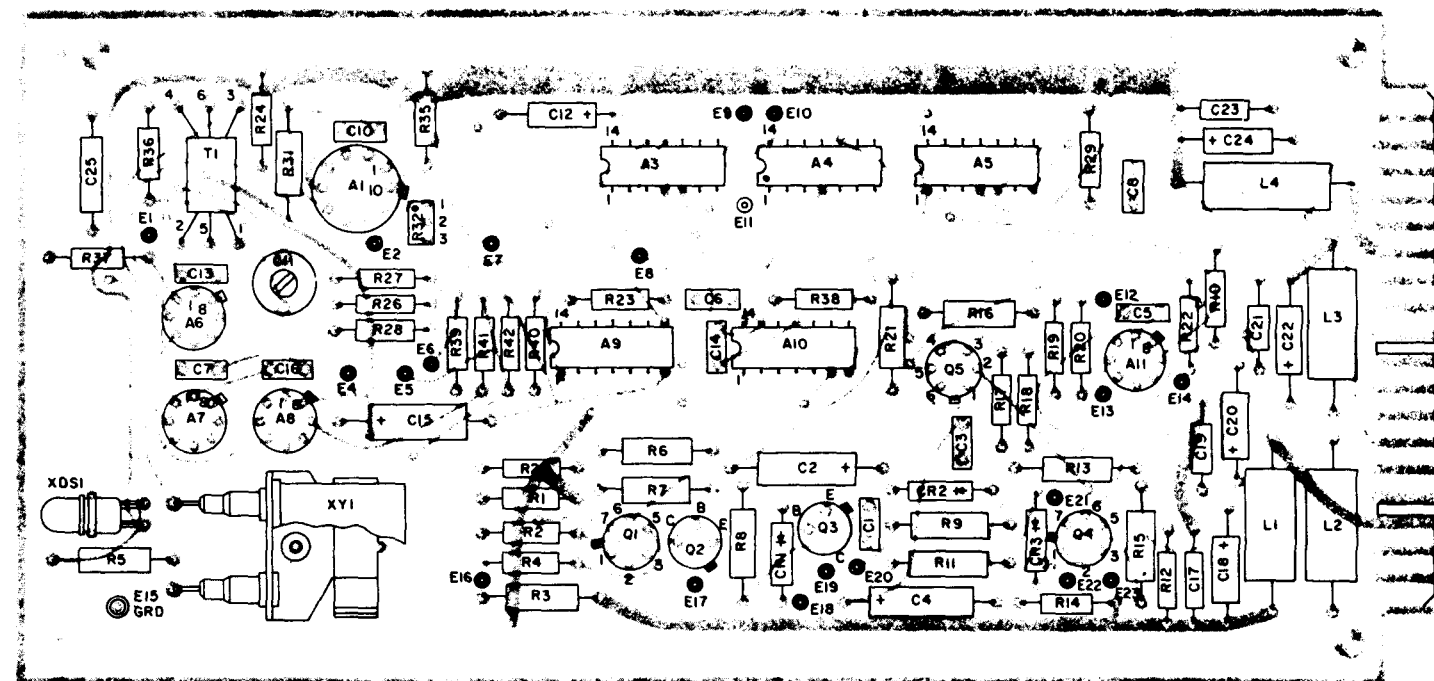


B WIRING ON BACK OF BOARD 1A12A7 (VIEWED THROUGH FRONT)

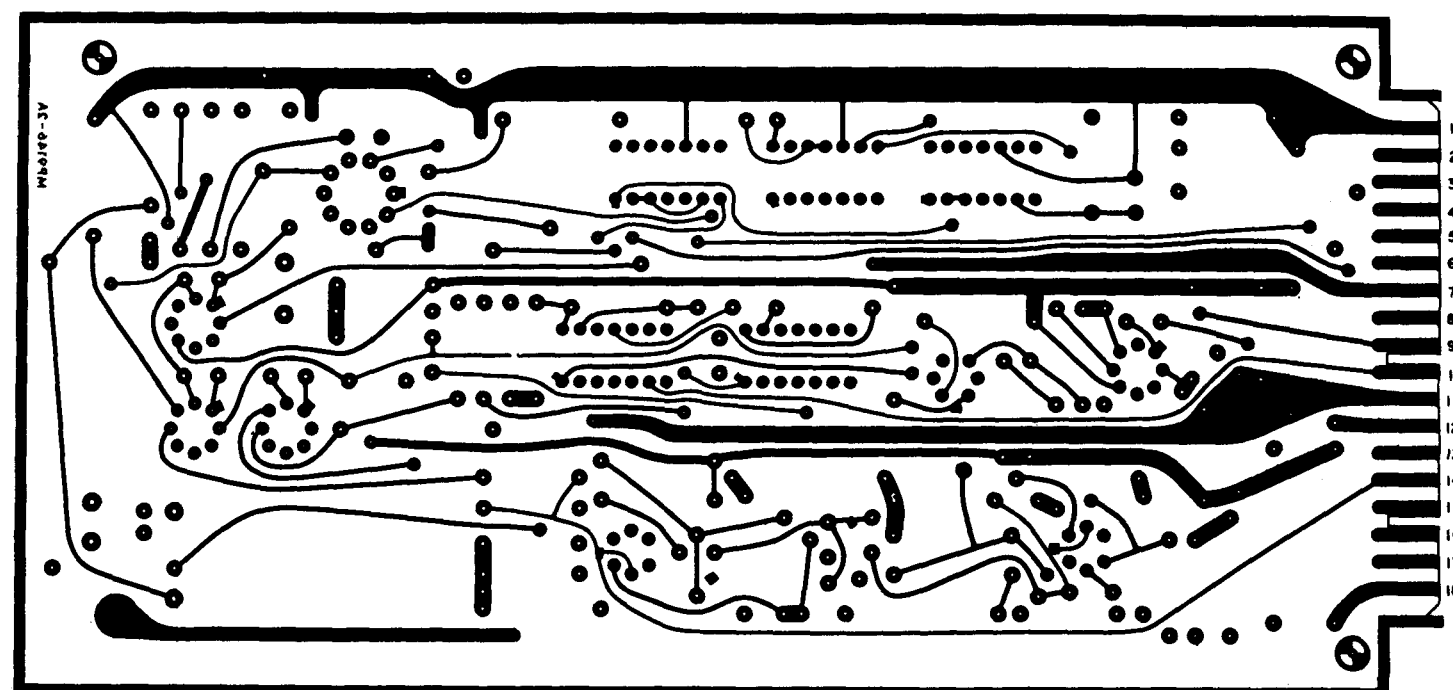
EL5820-695-35-TM-191

Figure 5-80. Radio amplifier-detector 1A12A7, parts location and printed wiring diagram.

NOTE:  
PARTIAL REFERENCE DESIGNATIONS  
ARE SHOWN, FOR COMPLETE  
DESIGNATION, PREFIX WITH 1A12A8.



A. PARTS AND WIRING ON FRONT OF BOARD 1A12A8 (683694)

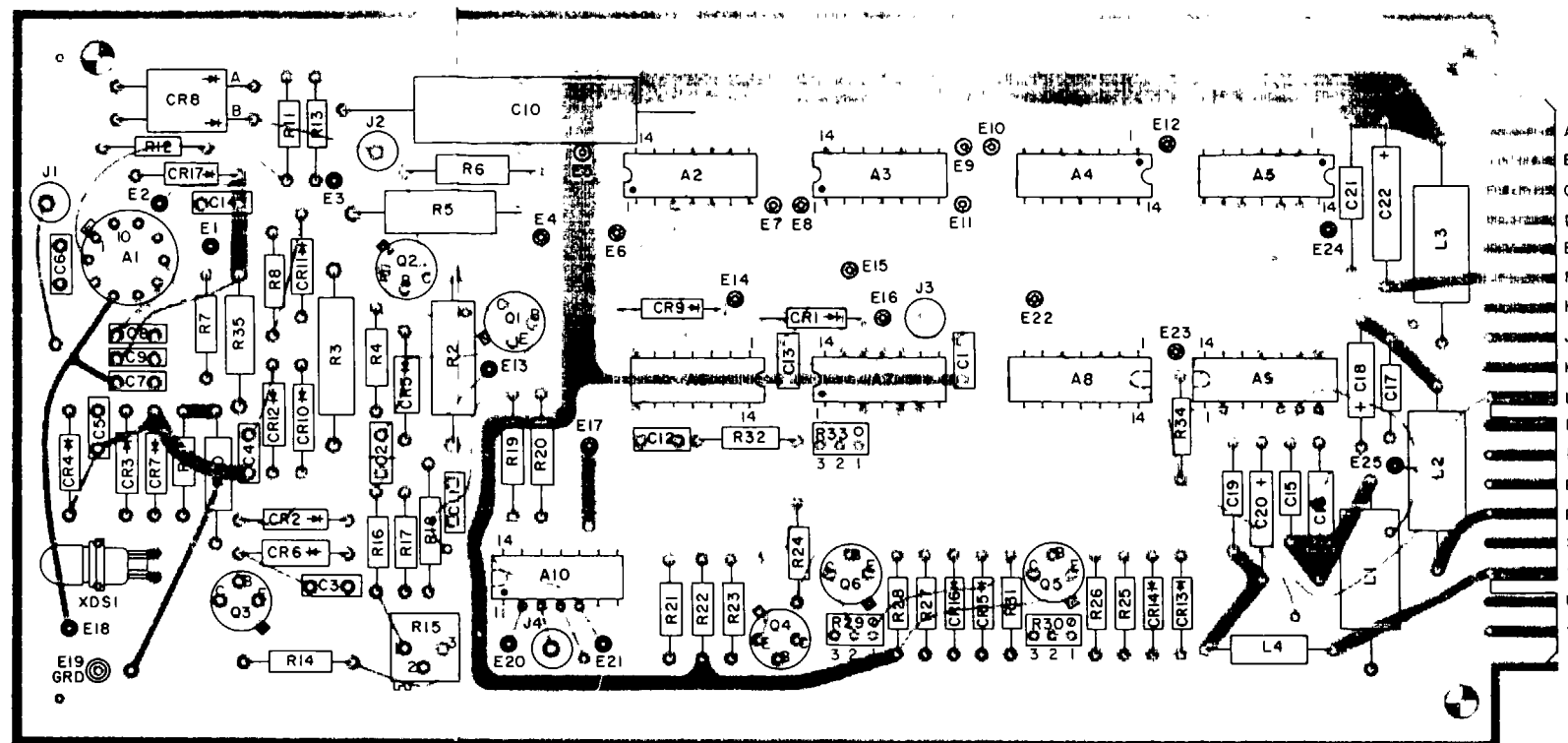


B. WIRING ON BACK OF BOARD 1A12A8 (VIEWED THROUGH FRONT).

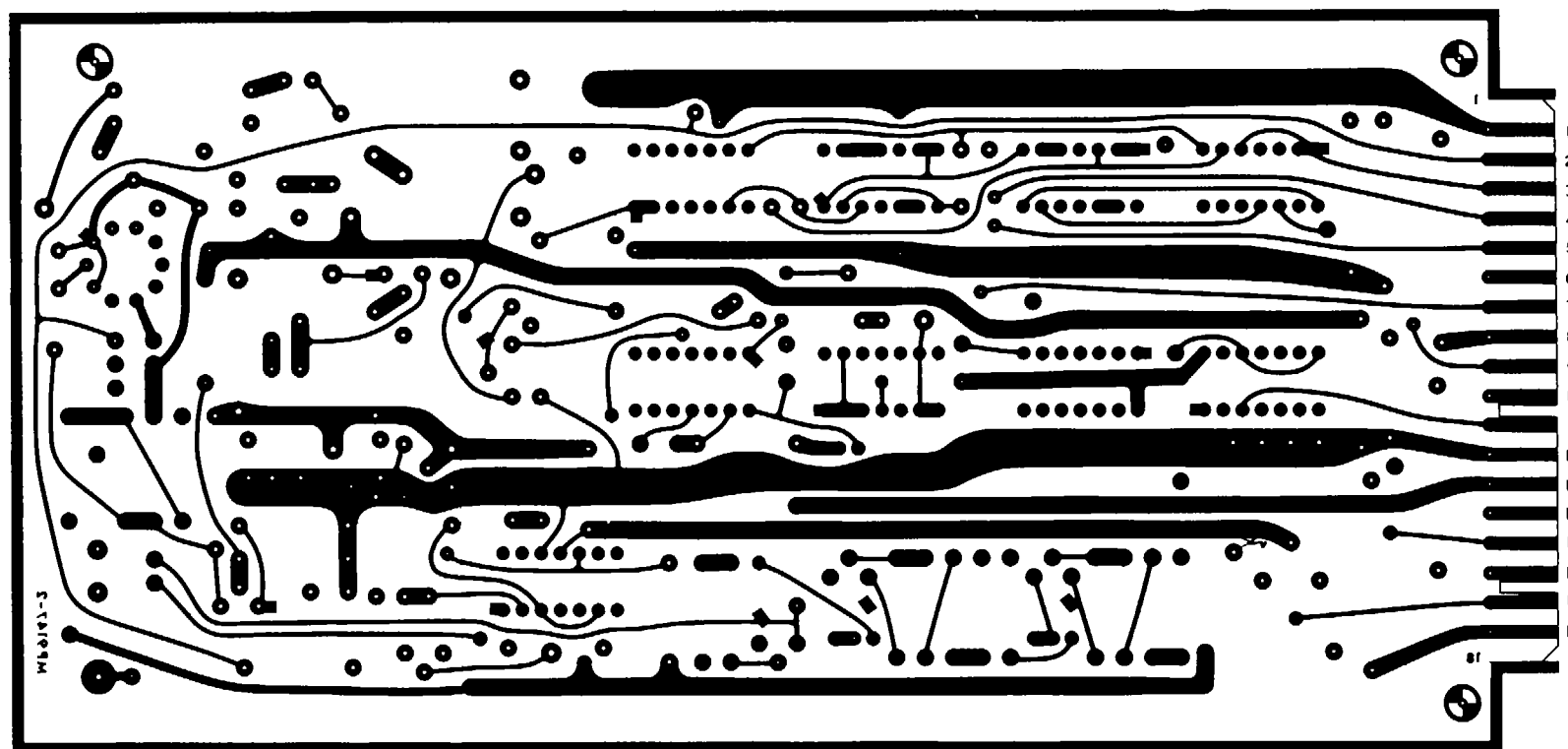
EL5820-695-35-TM-192

Figure 5-81. Radio digital regenerator 1A12A8, parts location and wiring diagram.

NOTE  
 PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN FOR COMPLETE  
 DESIGNATION, PREFIX WITH 1A12A9



A PARTS AND WIRING ON FRONT OF BOARD 1A12A9 (683695)

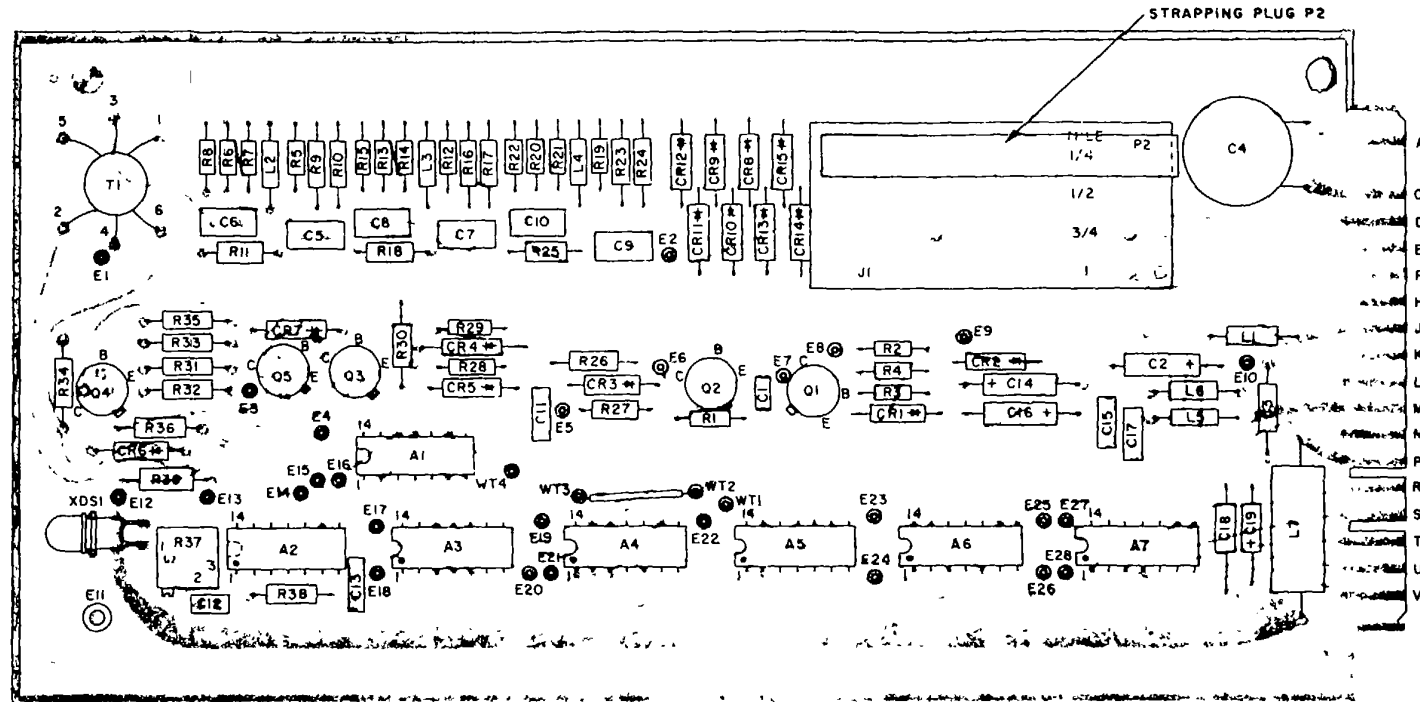


B WIRING ON BACK OF BOARD 1A12A9 (VIEWED THROUGH FRONT)

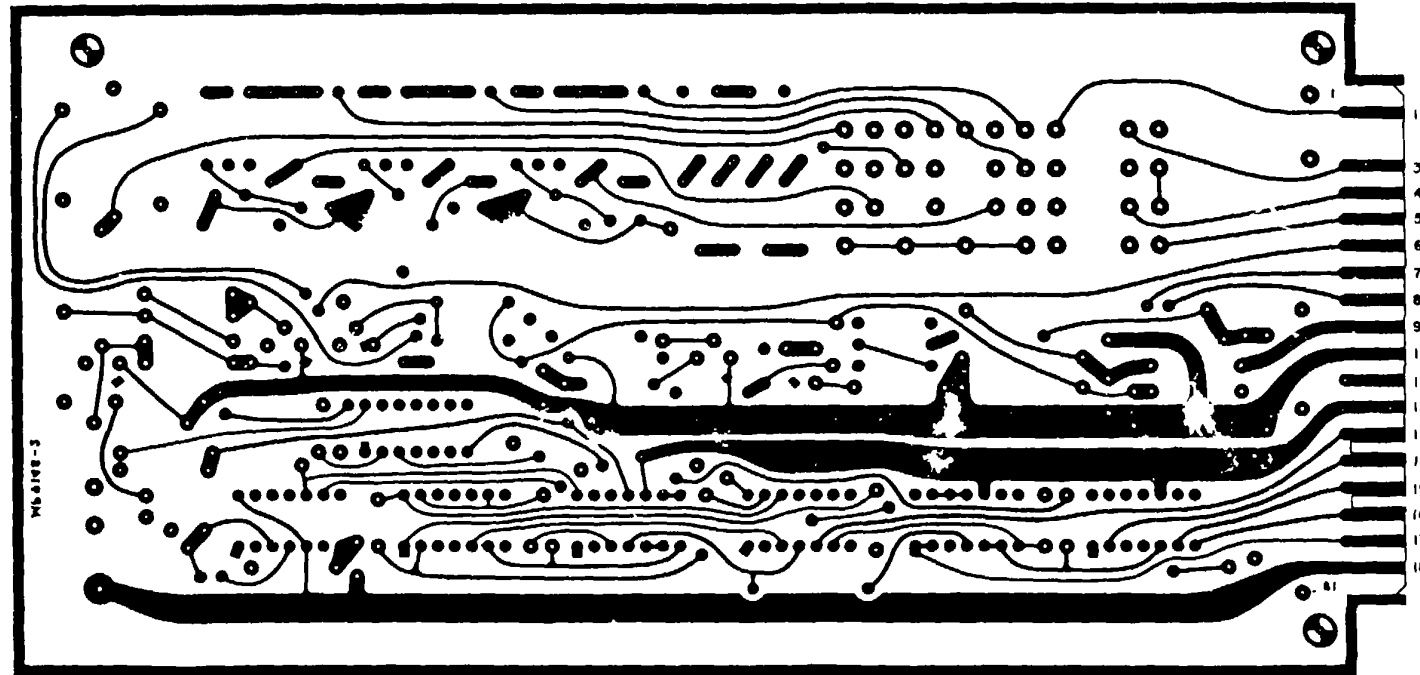
EL5820-695-35-TM-193

Figure 5-82. Radio control-comparator 1A12A9, parts location and printed wiring diagram

NOTE  
 PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN FOR COMPLETE  
 DESIGNATION, PREFIX WITH 1A12A10.



A. PARTS AND WIRING ON FRONT OF BOARD 1A12A10 (683696)



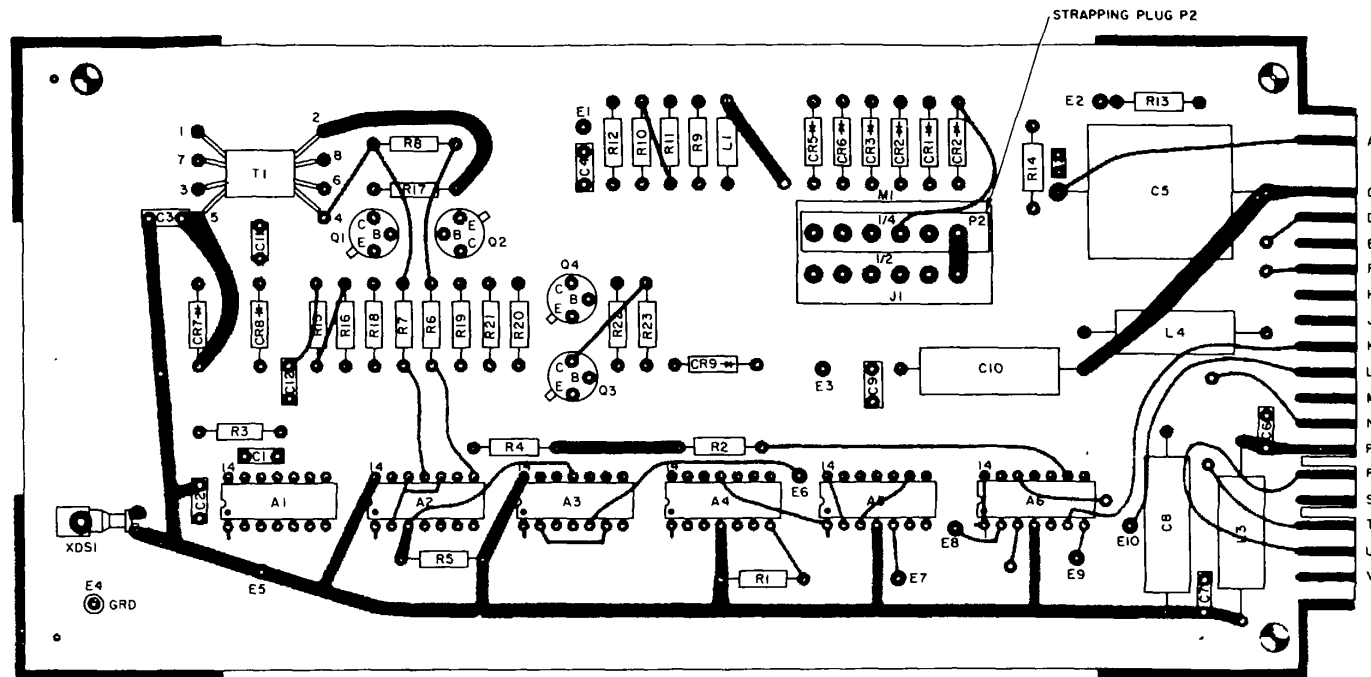
B. WIRING ON BACK OF BOARD 1A12A10 (VIEWED THROUGH FRONT)

EL5820-695-35-TM-194

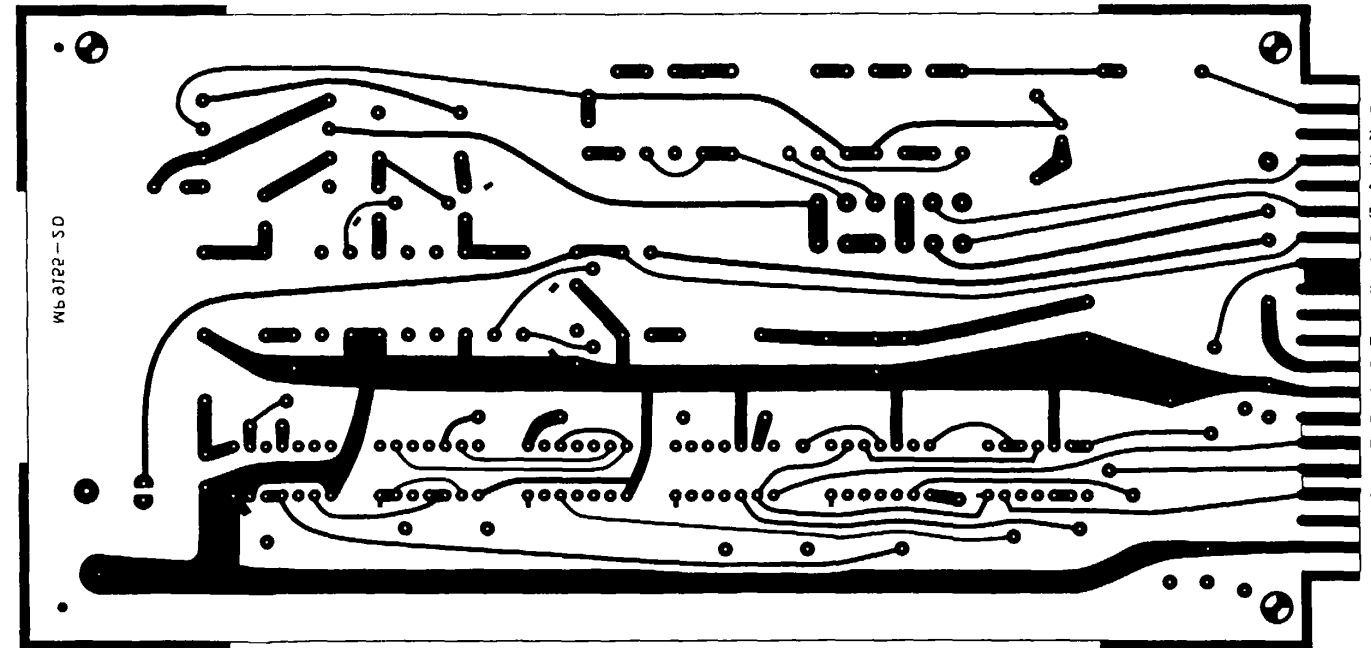
Figure 5-83. Radio digital processor 1A12A10, parts location and printed wiring diagram, synchronous mode.

Change 1 5-183

NOTE  
 PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN FOR COMPLETE  
 DESIGNATION, PREFIX WITH 1A12A16



A PARTS AND WIRING ON FRONT OF BOARD A16 (684092)



B WIRING ON BACK OF BOARD A16 (VIEWED THROUGH FRONT).

EL5820-695-35-C2-TM-12

Figure 5-83.1. Radio digital processor 1a12A16, parts location and printed wiring diagram, asynchronous mode.

Change 2 5-184.1



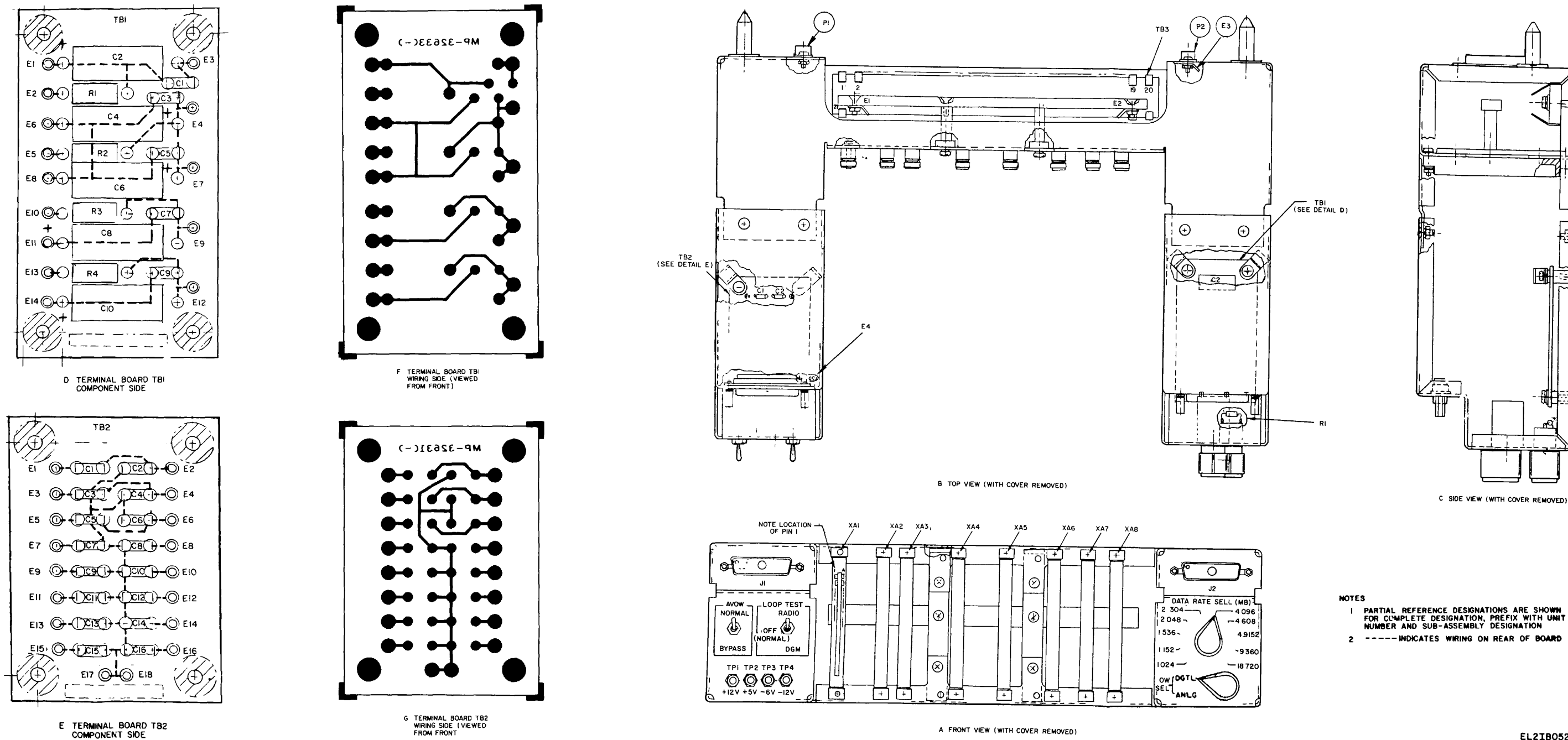
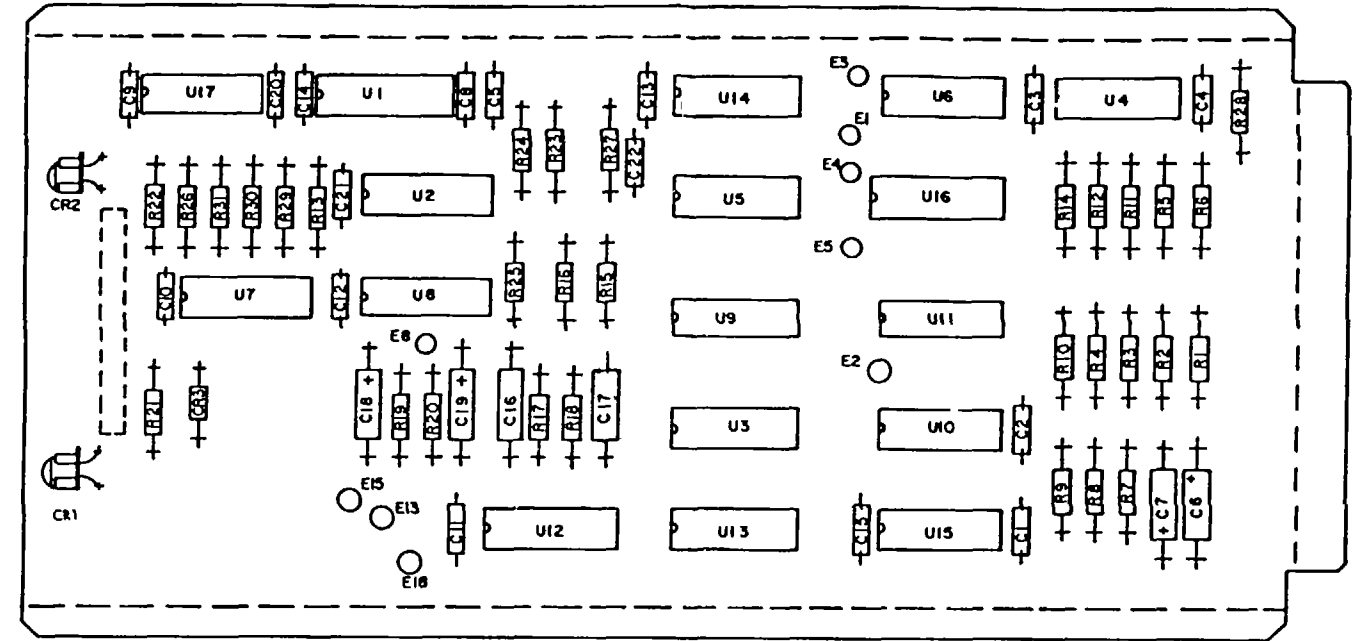


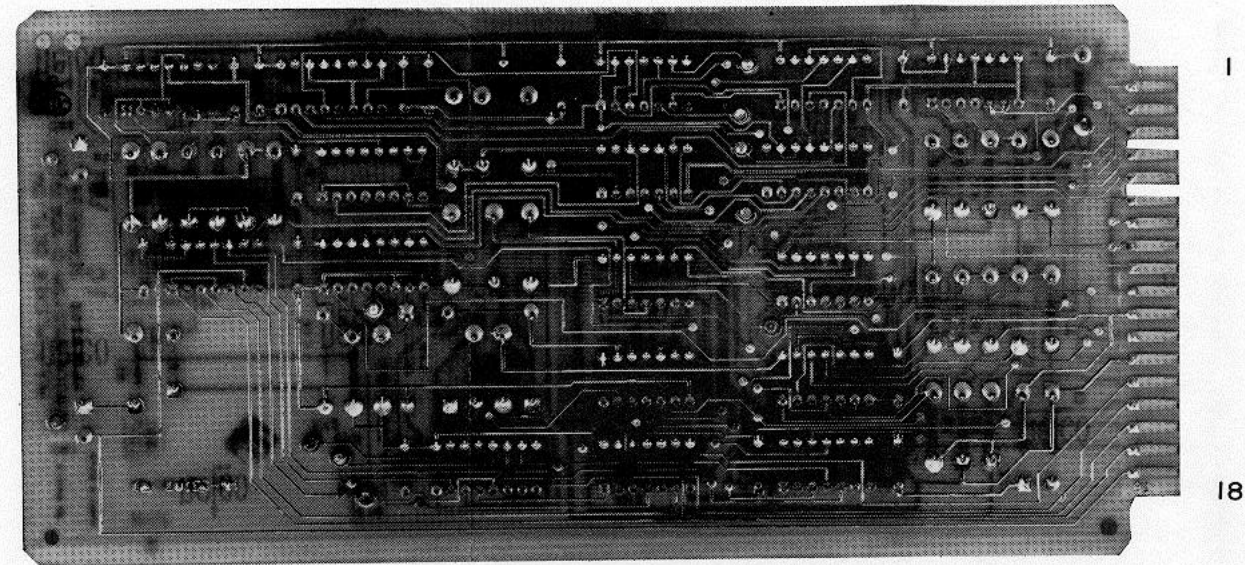
Figure 5-83.2. Digital data combiner 1A12, parts location and printed wiring diagram.

Change 6 5-184.3

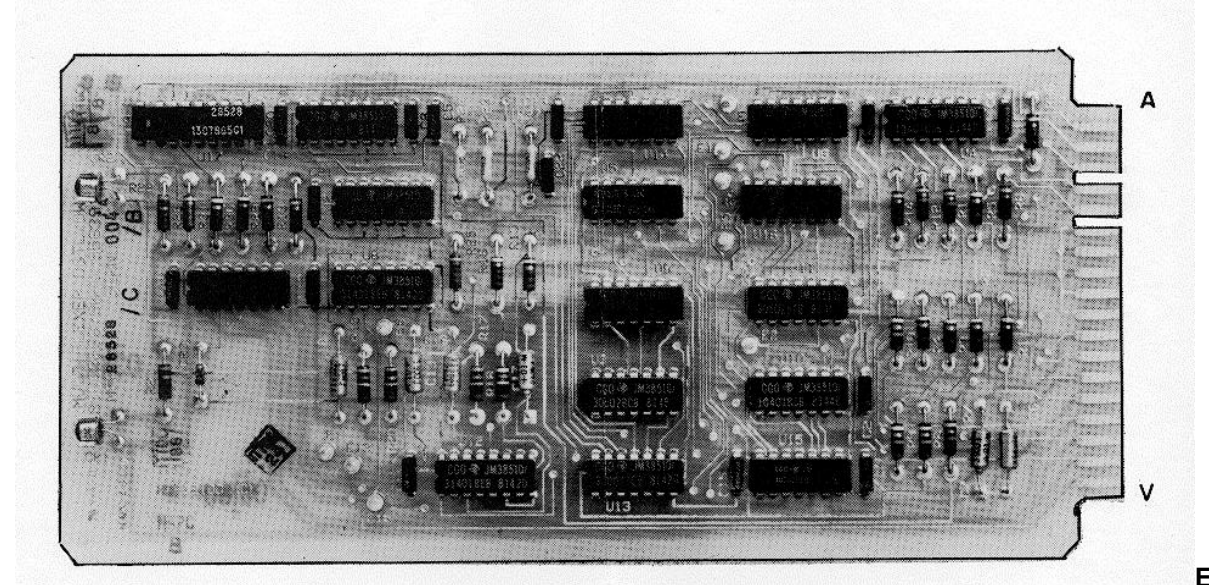
NOTE:  
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A12A1.



A. REFERENCE DESIGNATIONS OF PARTS ON FRONT OF BOARD A1 (956391)



C. WIRING ON BACK OF BOARD (VIEW THROUGH FRONT)



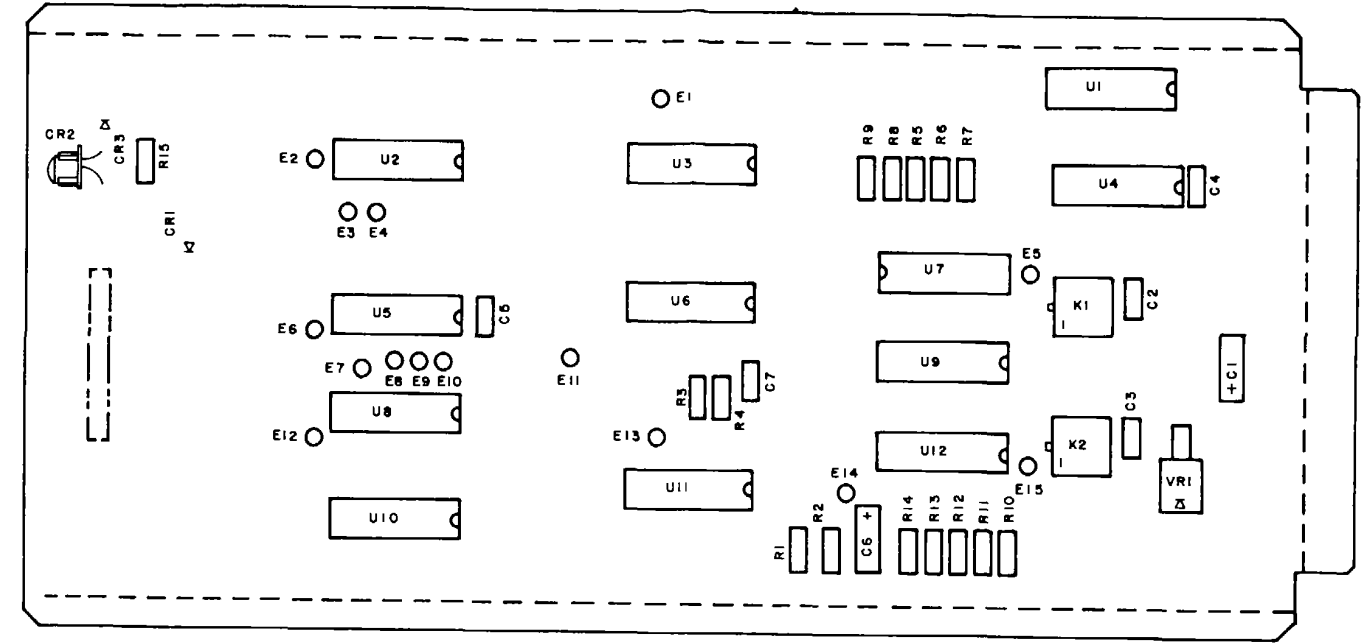
B. PARTS AND WIRING ON FRONT OF BOARD A1

EL2IB053

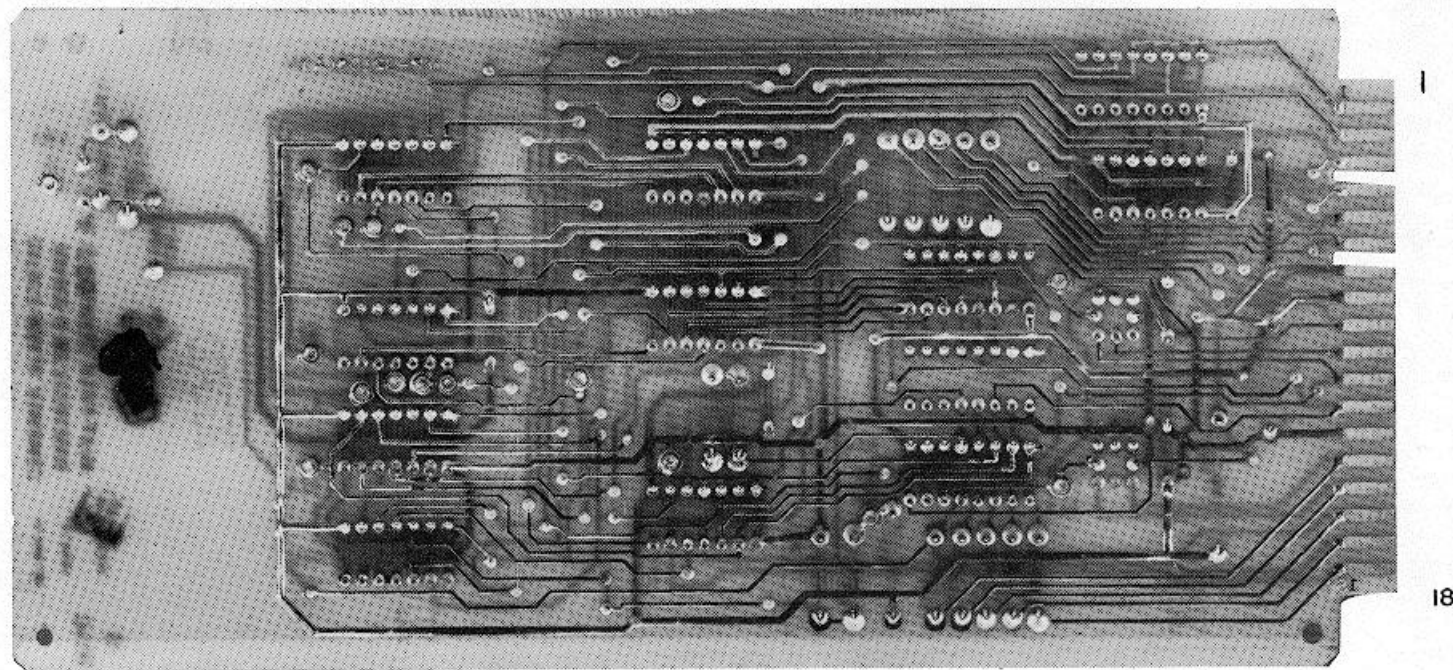
Figure 5-83.3. Multiplexer, digital orderwire 1A12A1, parts location diagram.

NOTE:

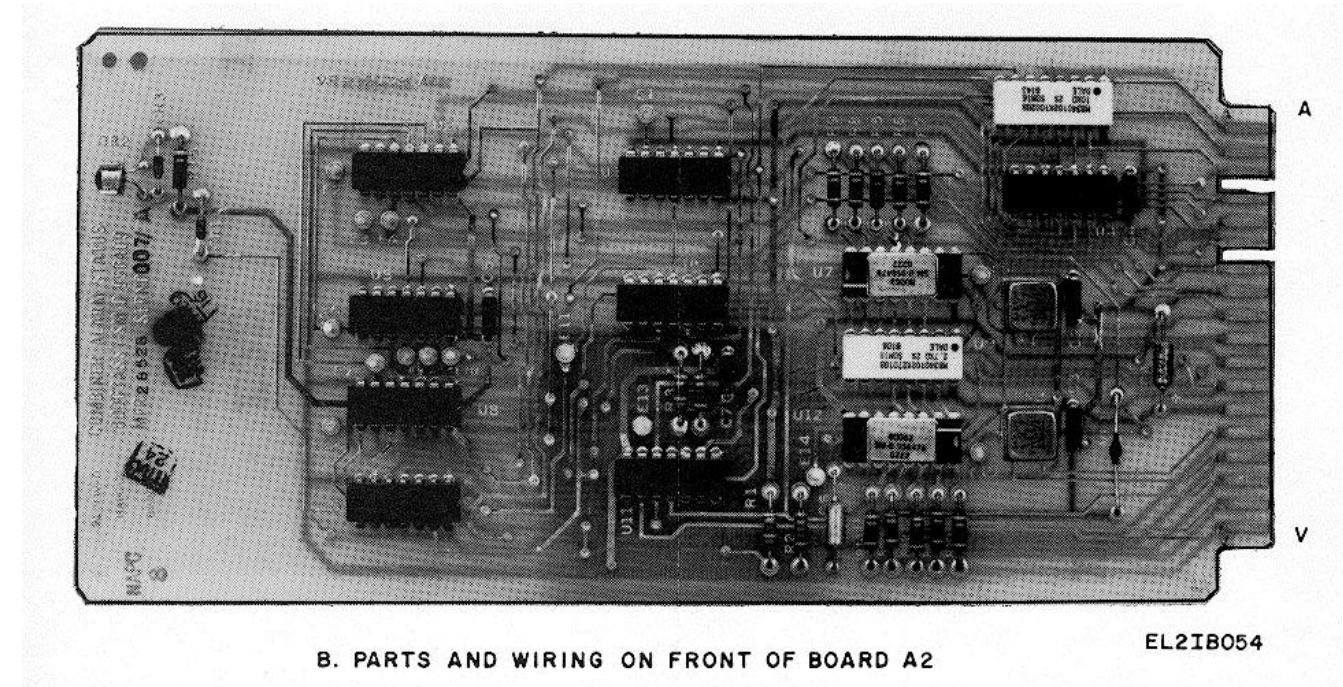
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A12A2.



A. REFERENCE DESIGNATIONS OF PARTS ON FRONT OF BOARD a2 (956409)



C. WIRING ON BACK OF BOARD (VIEW THROUGH FRONT)



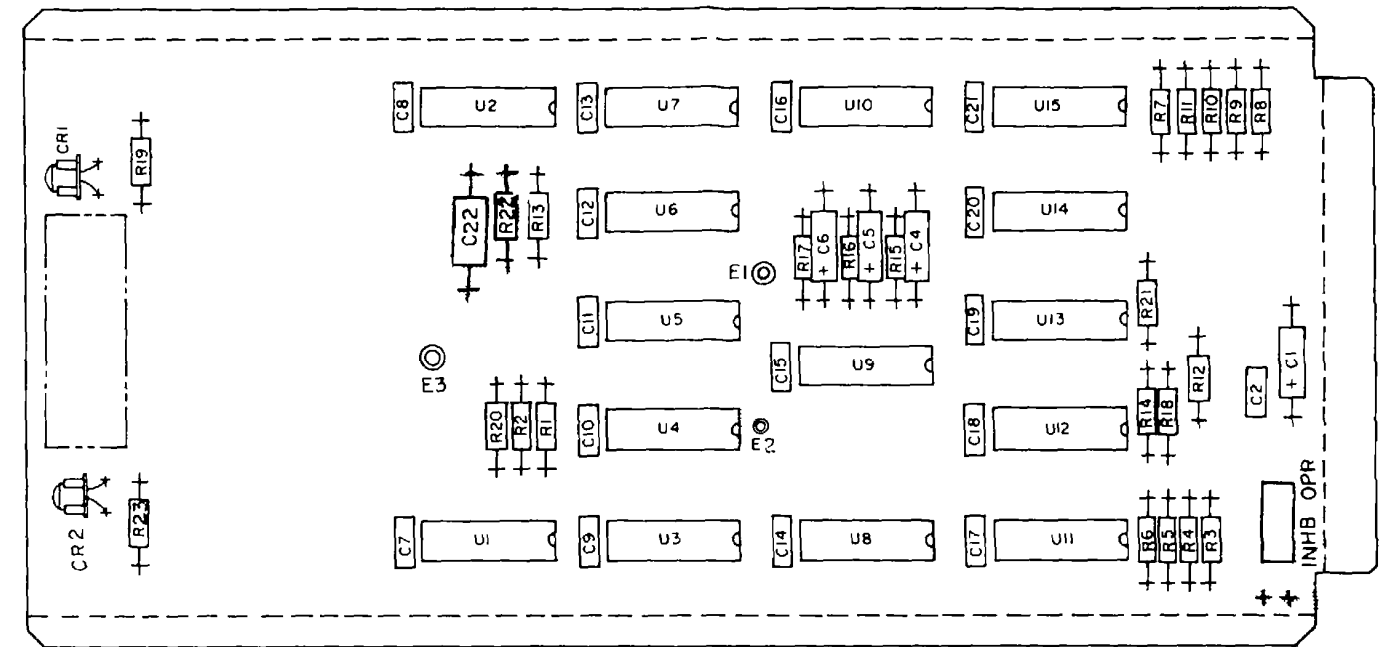
B. PARTS AND WIRING ON FRONT OF BOARD A2

EL2IB054

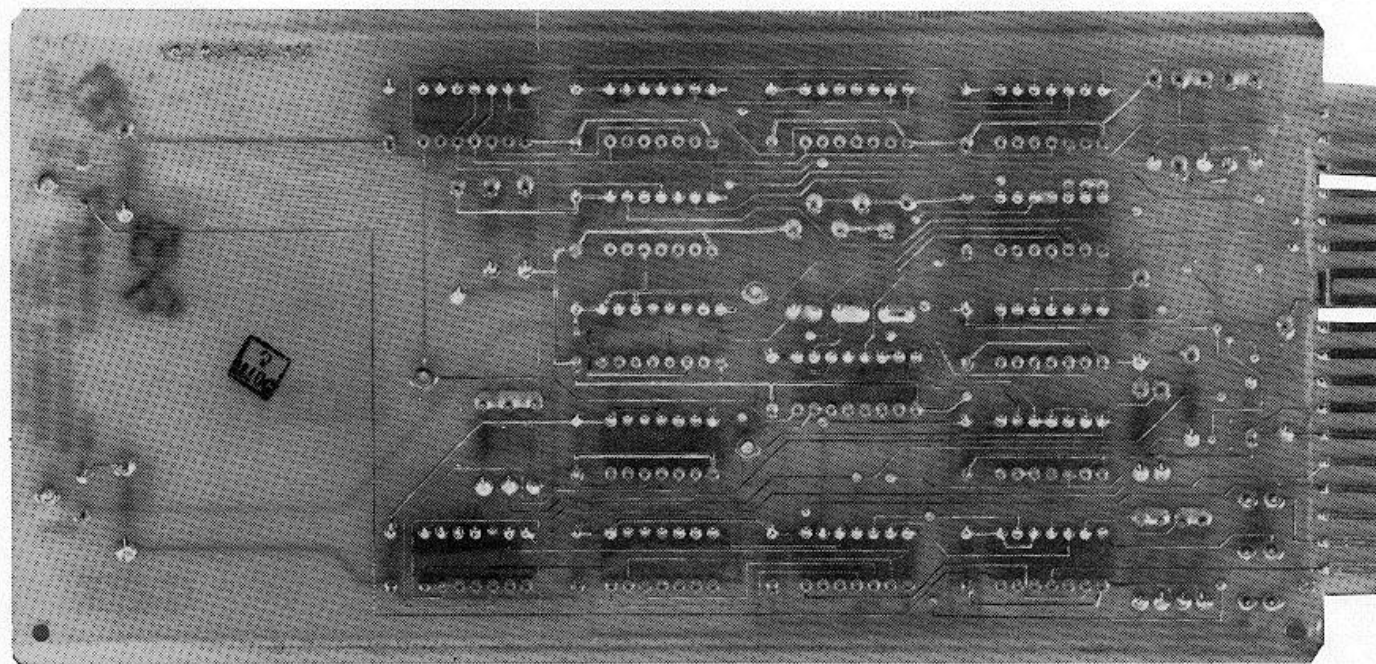
Figure 5-83.4. Combiner, alarm status 1A12A2, parts location diagram.



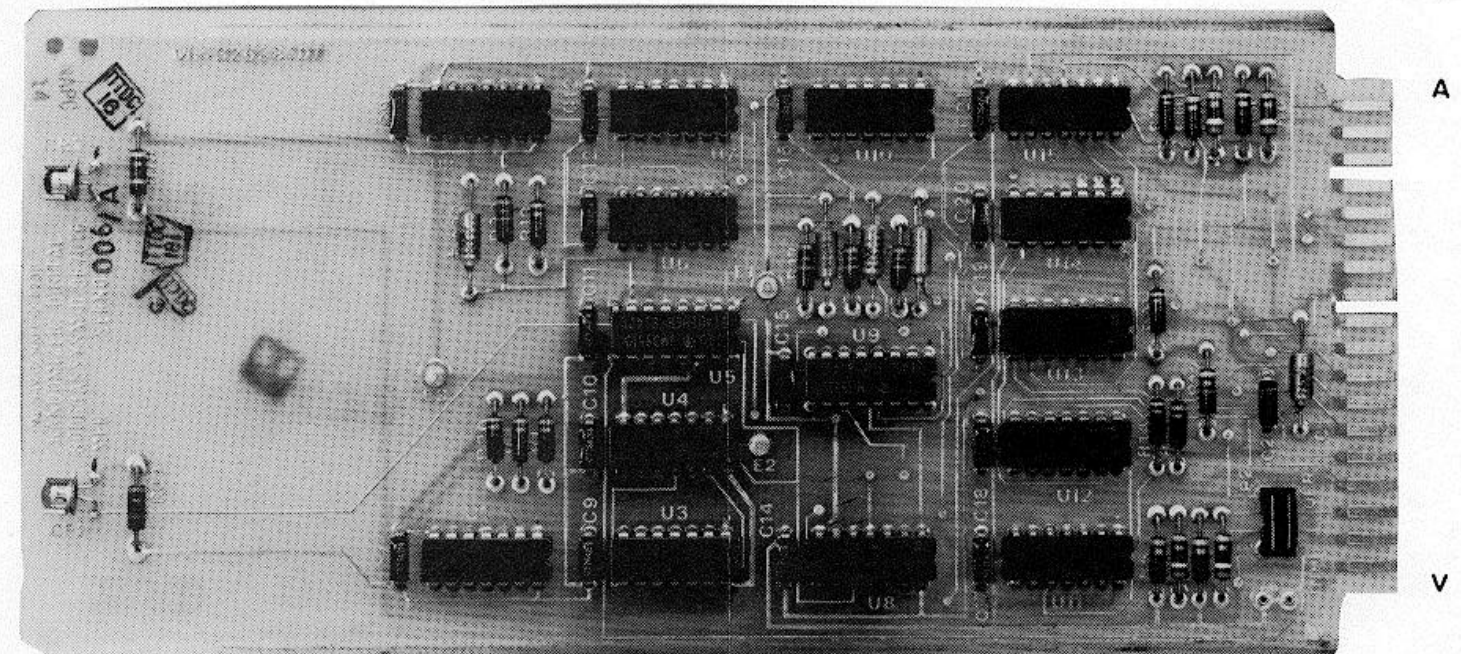
**NOTE:**  
 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.  
 FOR COMPLETE DESIGNATION, PREFIX WITH 1A123A3.



**A. REFERENCE DESIGNATIONS OF PARTS ON FRONT OF BOARD A (967016)**



**C. WIRING ON BACK OF BOARD (VIEW THROUGH FRONT)**

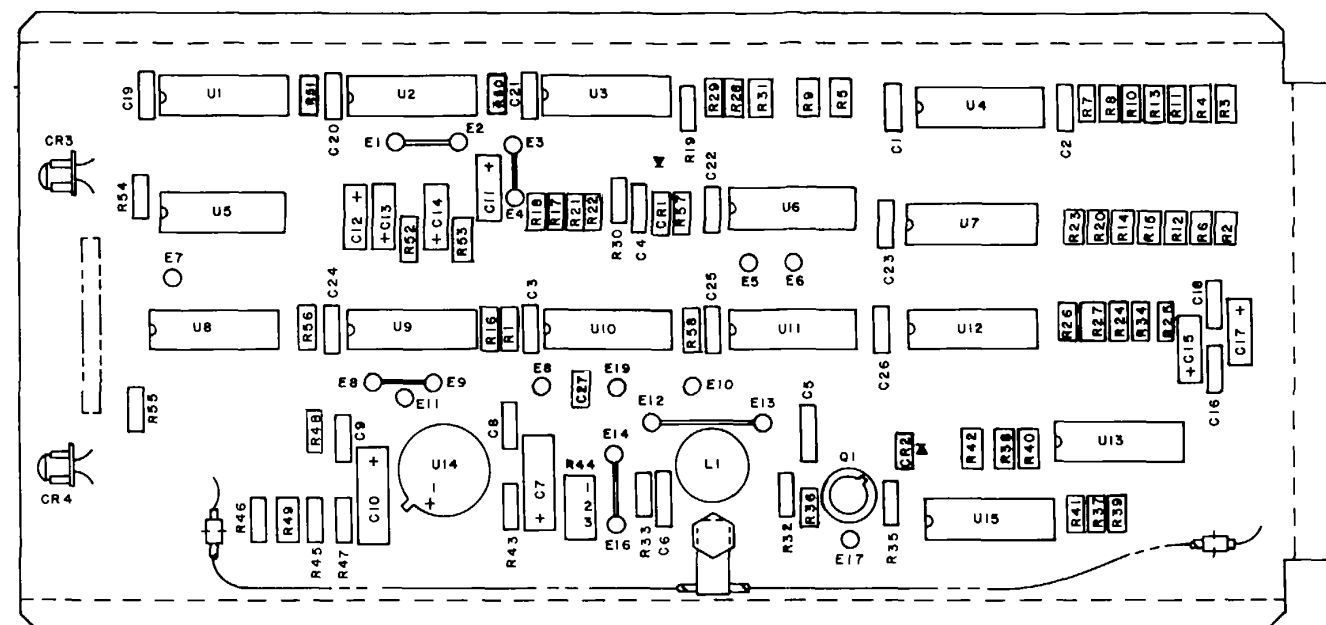


**B. PARTS AND WIRING ON FRONT OF BOARD**

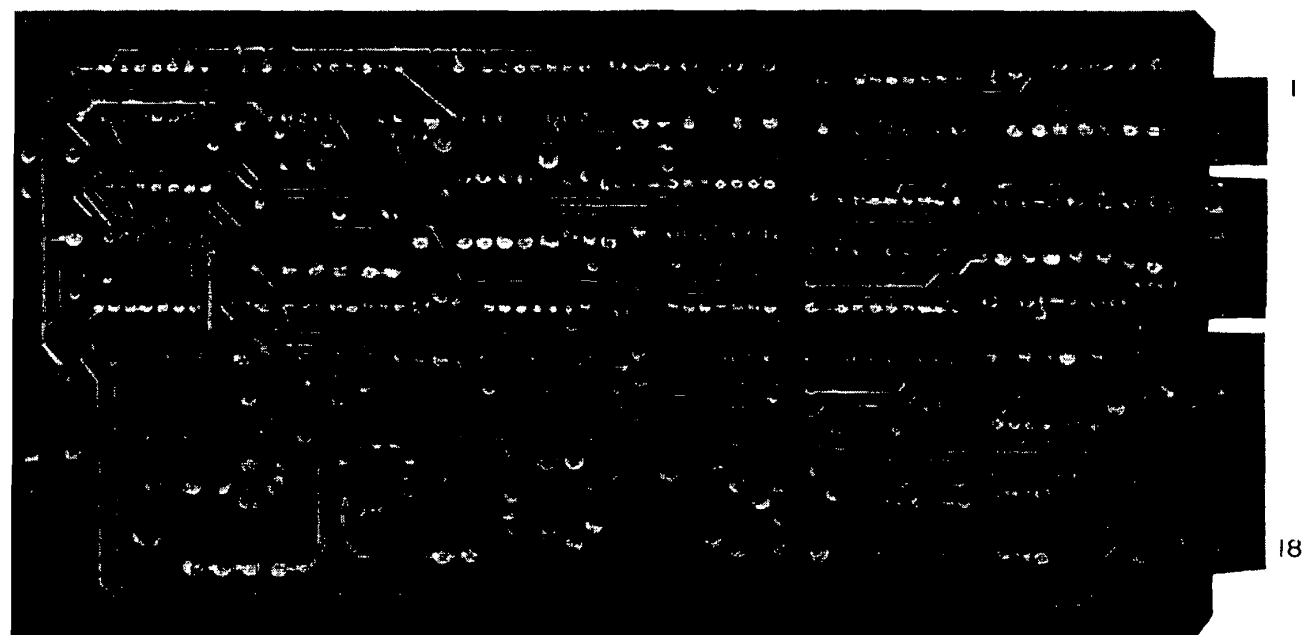
EL21B055

**Figure 5-83.5. Randomizer Digital 1A12A3, parts location diagram.**

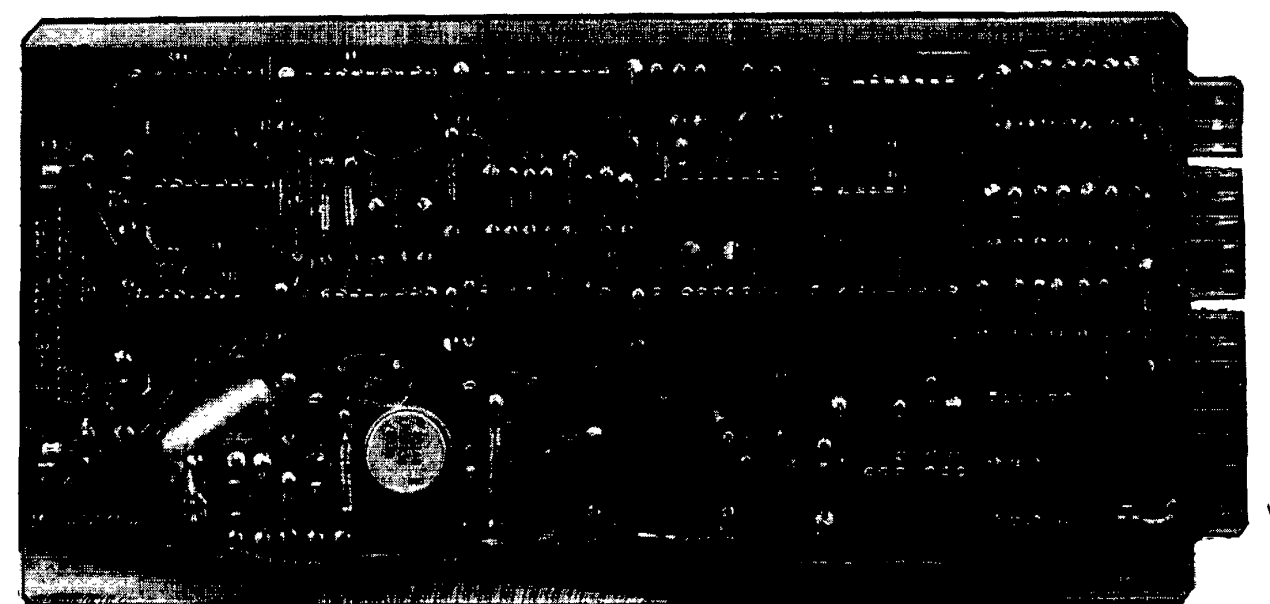
NOTE:  
 PARTIAL REFERENCE DESIGNATIONS ARE  
 SHOWN. FOR COMPLETE DESIGNATION,  
 PREFIX WITH 1A12A4.



A. REFERENCE DESIGNATIONS OF PARTS ON FRONT OF BOARD A4 (956400)



C. WIRING ON BACK OF BOARD (VIEW THROUGH FRONT)



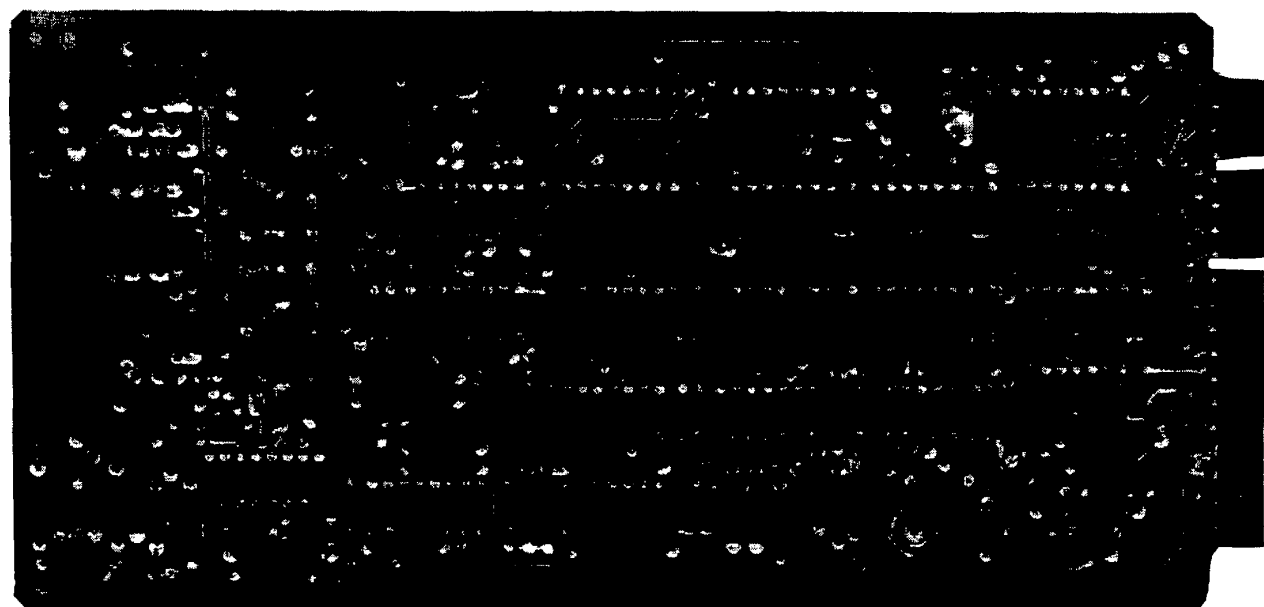
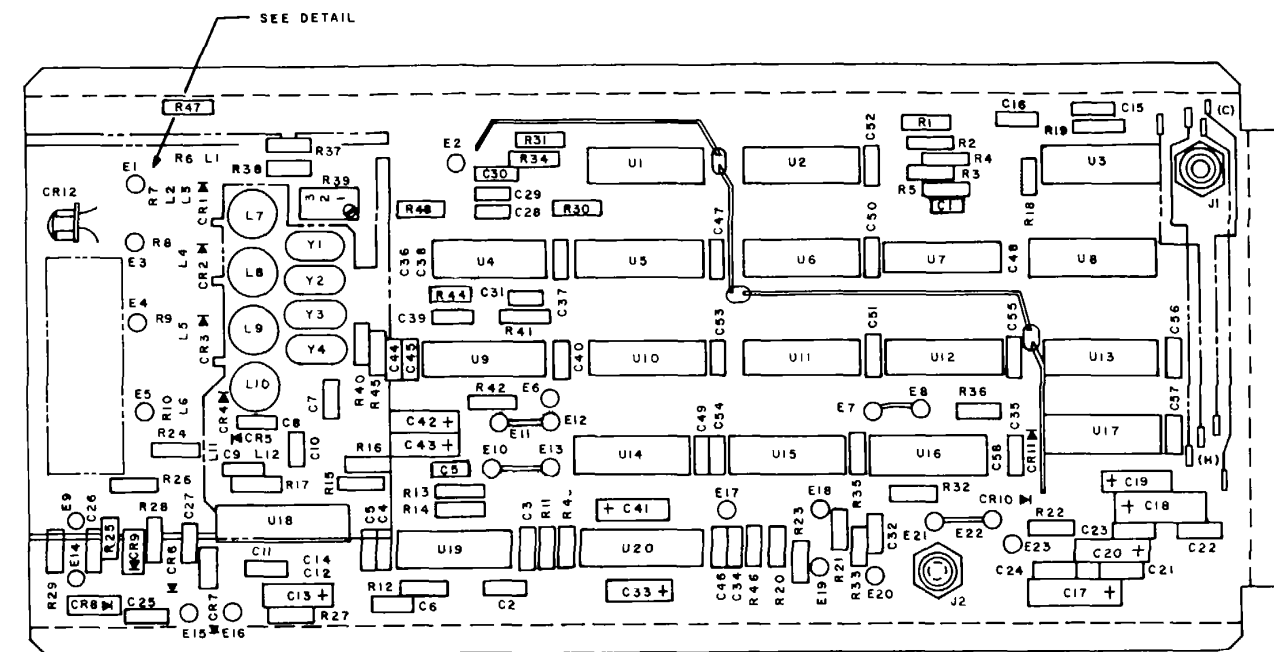
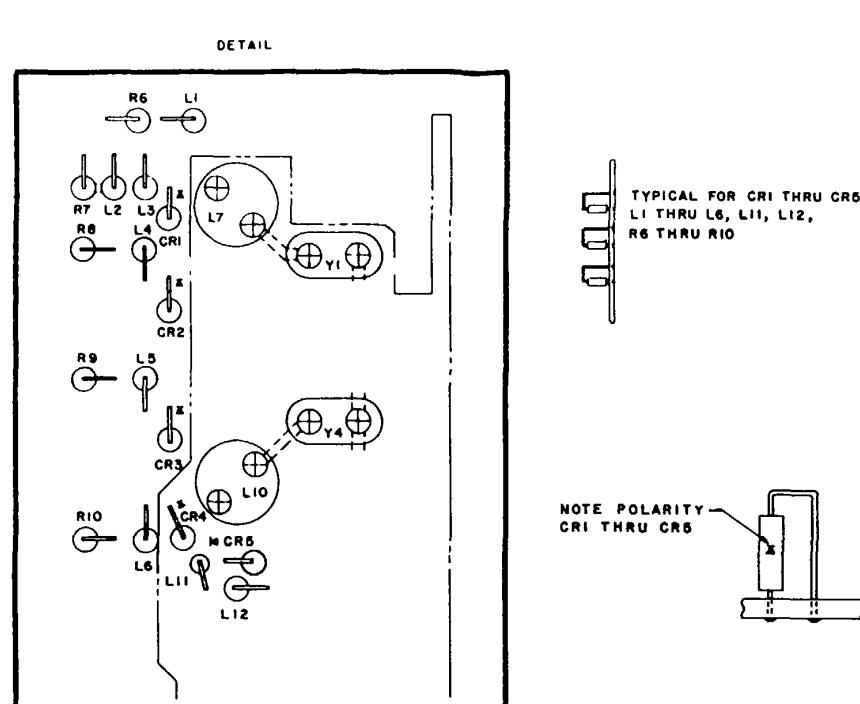
B. PARTS AND WIRING ON FRONT OF BOARD A4

EL2IB056

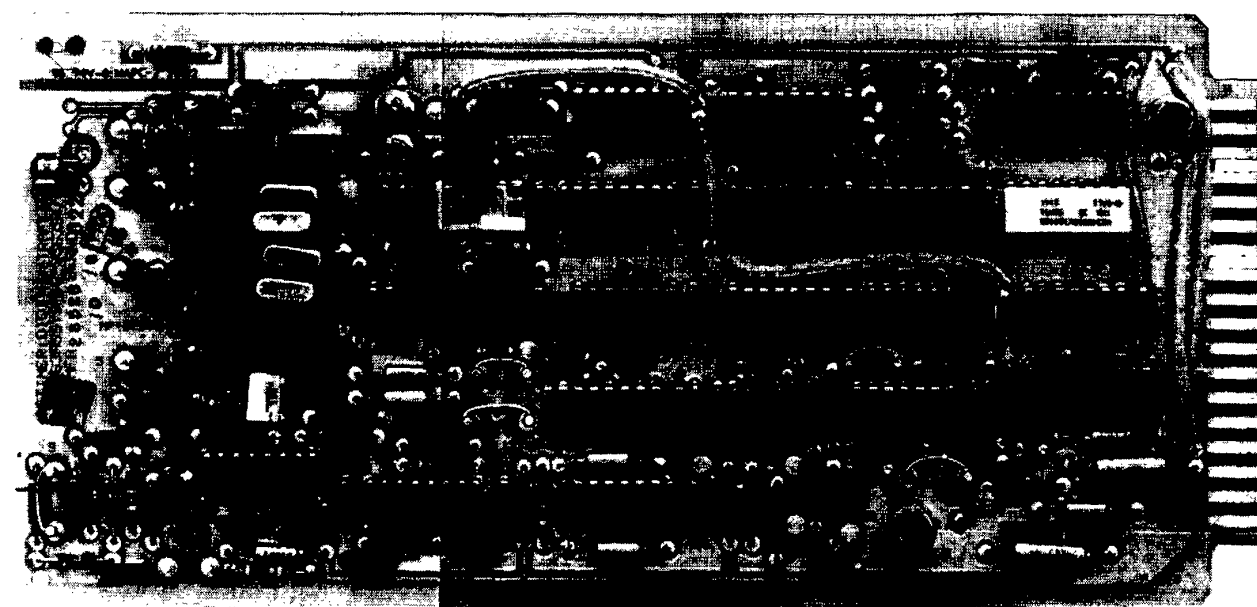
Figure 5-83.6. Buffer, digital interface 1A12A4, parts location diagram.

Change 6 5-184.11

NOTE:  
PARTIAL REFERENCE DESIGNATIONS  
ARE SHOWN. FOR COMPLETE  
DESIGNATION, PREFIX WITH 1A12A5.



C. WIRING ON BACK OF BOARD (VIEW THROUGH FRONT)

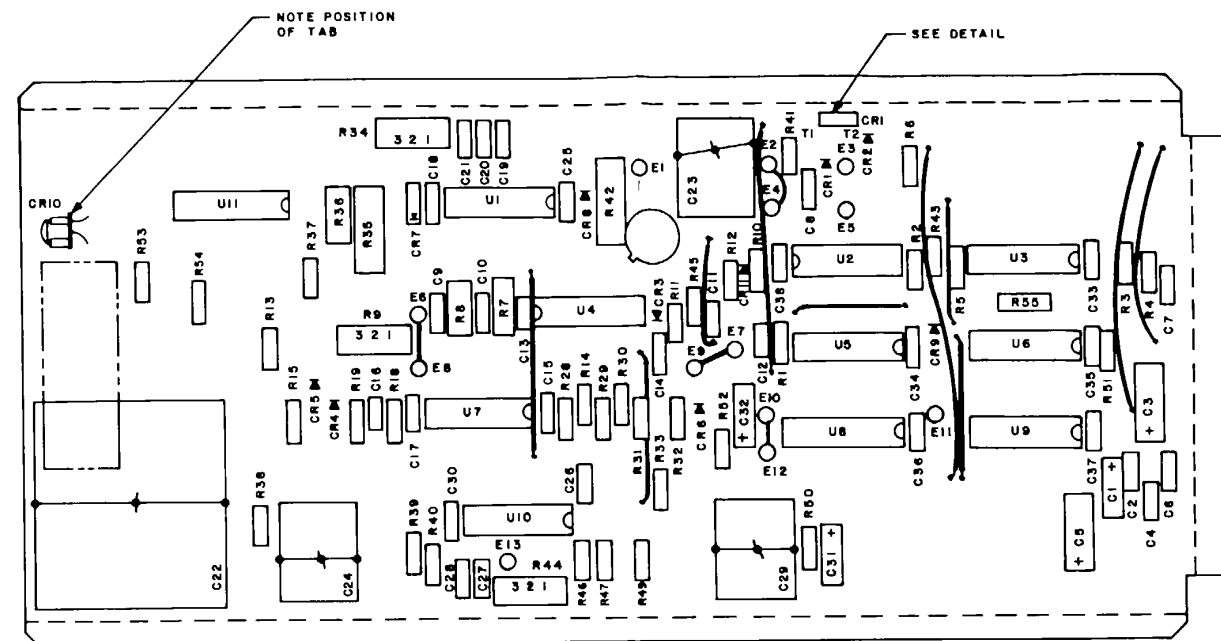


B. PARTS AND WIRING ON FRONT OF BOARD A5

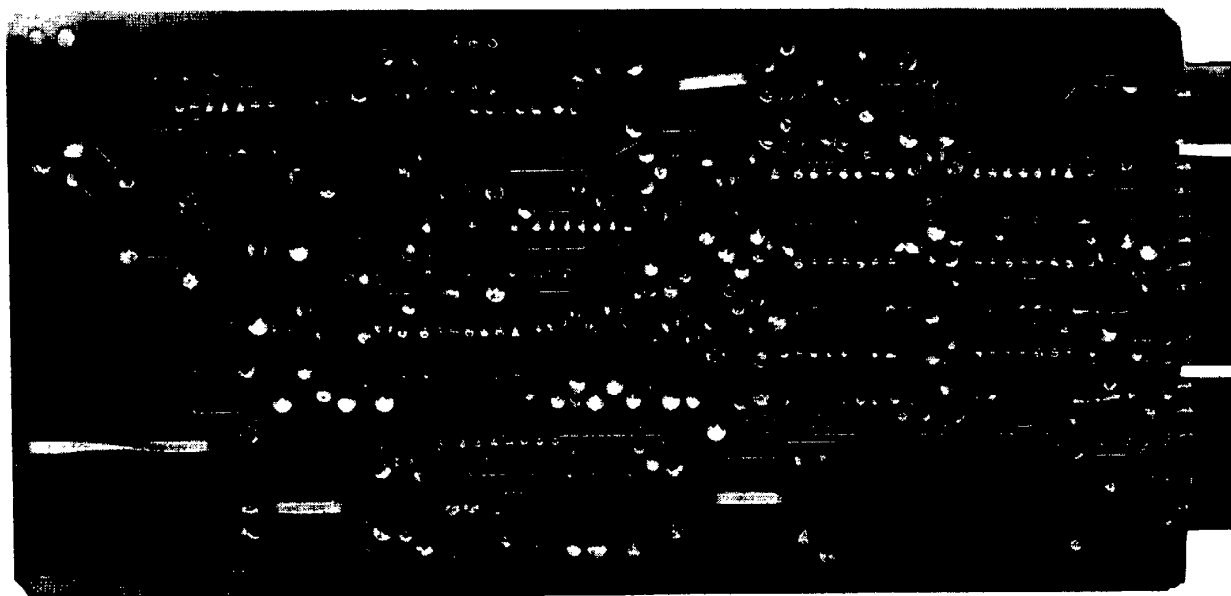
EL2IB057

Figure 5-83.7. Retimer, digital traffic 1A12A5, parts location diagram.

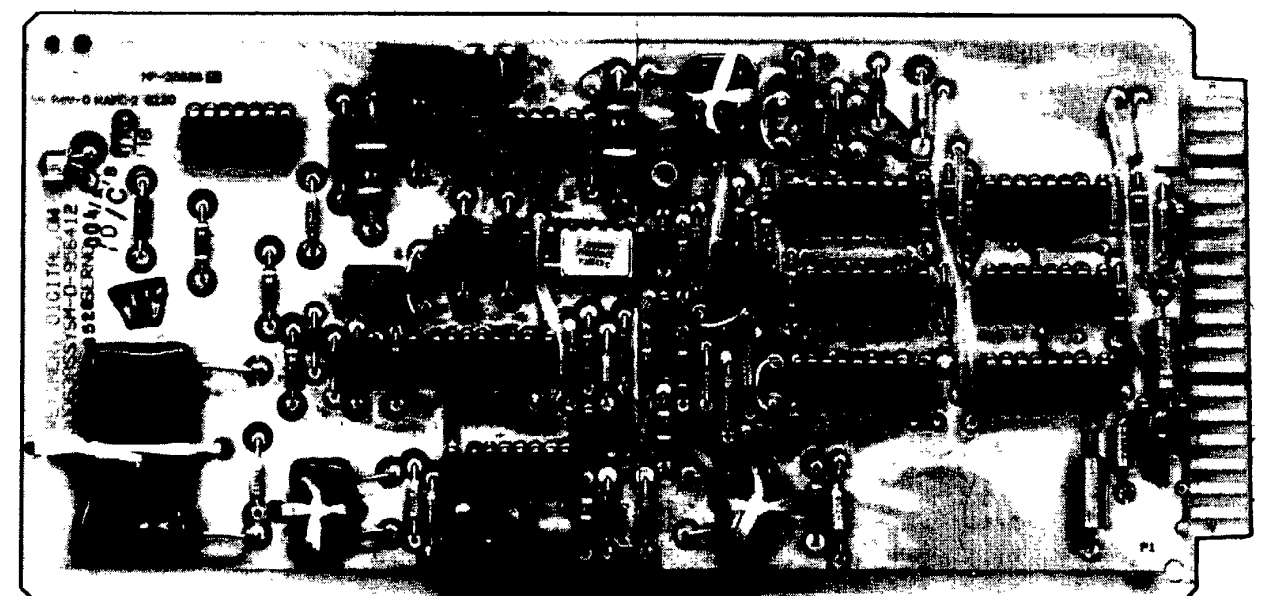
NOTE:  
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A12A6.



A. REFERENCE DESIGNATIONS OF PARTS ON FRONT OF BOARD A6 (956412)



C. WIRING ON BACK OF BOARD (VIEW THROUGH FRONT)

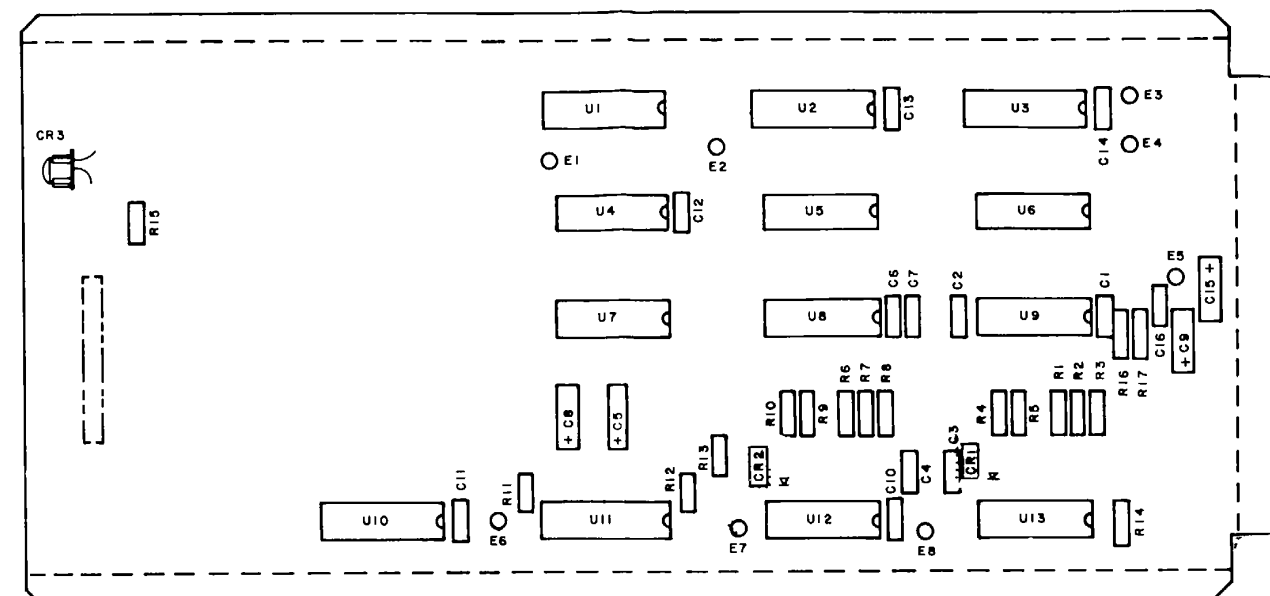


B. PARTS AND WIRING ON FRONT OF BOARD A6

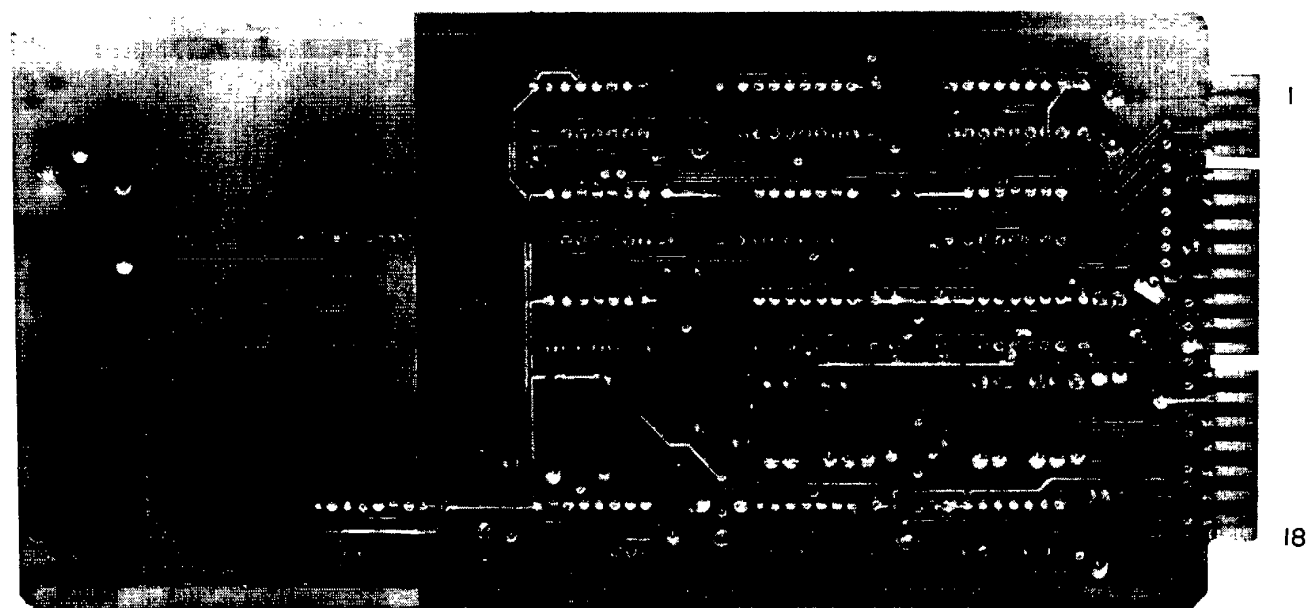
EL2IB058

Figure 5-83.8. Retimer, digital orderwire 1A12A6, parts location diagram.

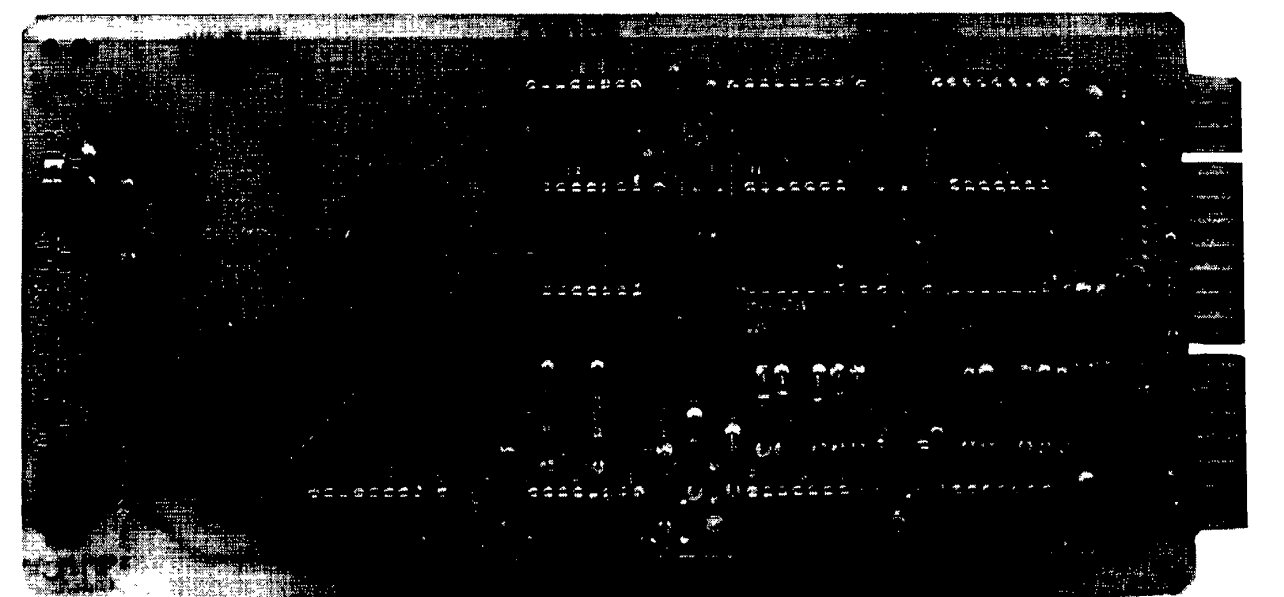
NOTE:  
 PARTIAL REFERENCE DESIGNATIONS ARE  
 SHOWN. FOR COMPLETE DESIGNATION,  
 PREFIX WITH 1A12A7.



A. REFERENCE DESIGNATIONS OF PARTS ON FRONT OF BOARD A7 (956406)



C. WIRING ON BACK OF BOARD (VIEW THROUGH FRONT)



B. PARTS AND WIRING ON FRONT OF BOARD A7

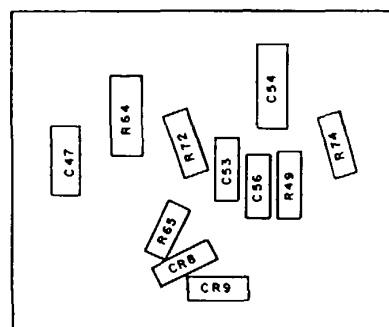
Figure 5-83.9. Demultiplexer, digital orderwire 1A12A7, parts location diagram.

Change 6 5-184.17

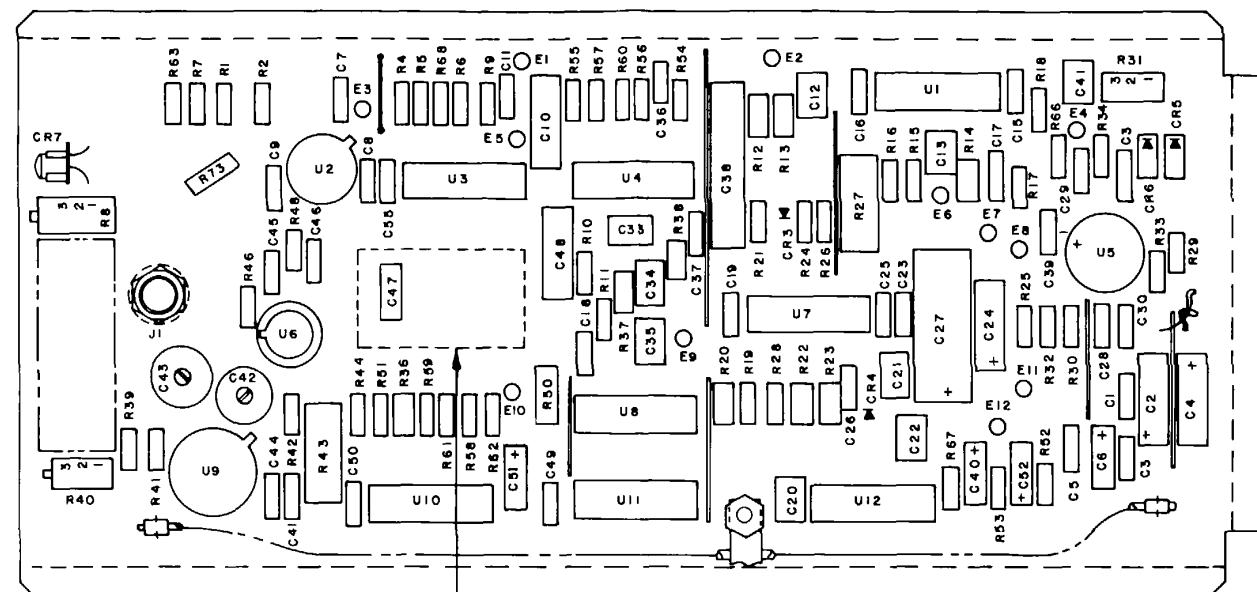
EL2IB059



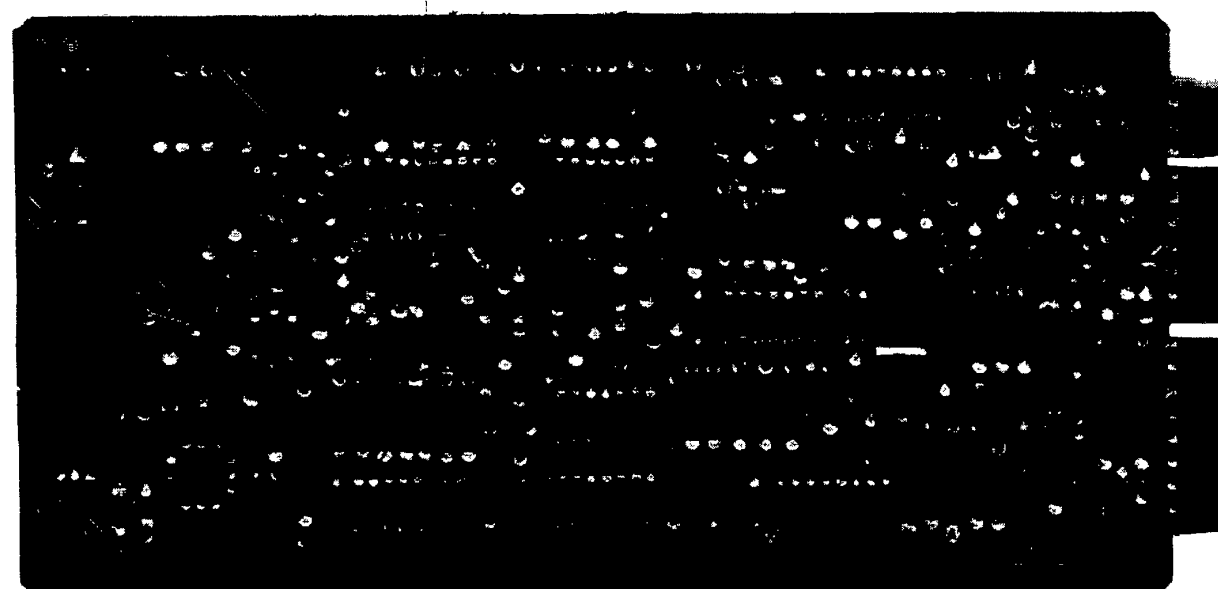
NOTE:  
PARTIAL REFERENCE DESIGNATIONS ARE  
SHOWN. FOR COMPLETE DESIGNATION,  
PREFIX WITH 1A12A1.



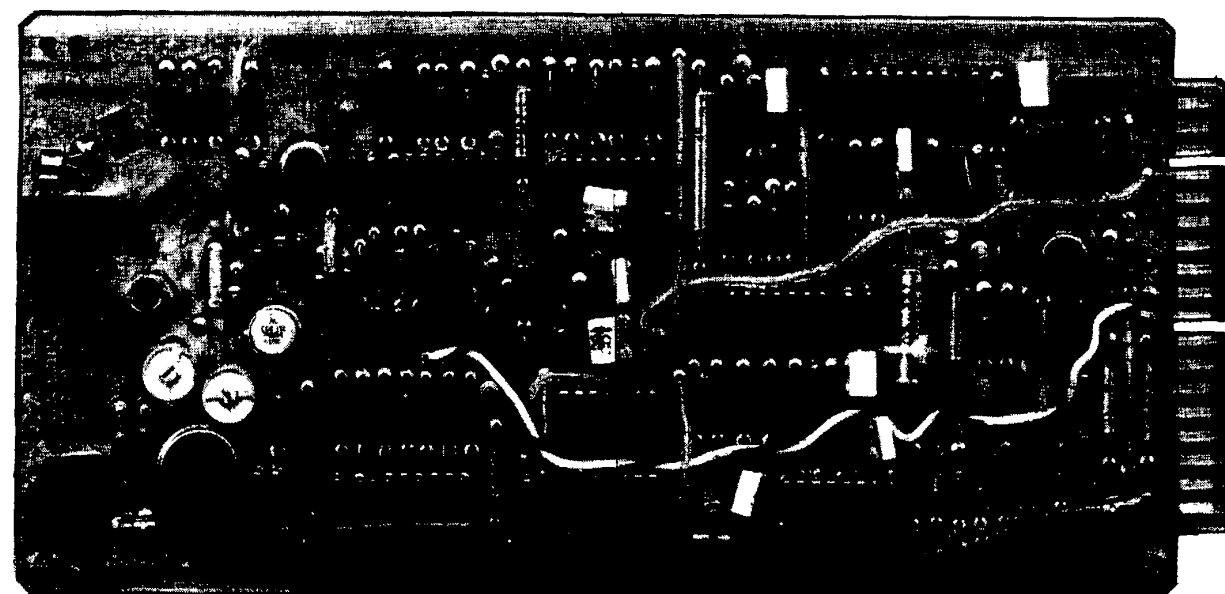
BOARD A8 DETAIL



A. REFERENCE DESIGNATIONS OF PARTS ON FRONT OF BOARD A8 (956403)



C. WIRING ON BACK OF BOARD (VIEW THROUGH FRONT)



B. PARTS AND WIRING ON FRONT OF BOARD A8

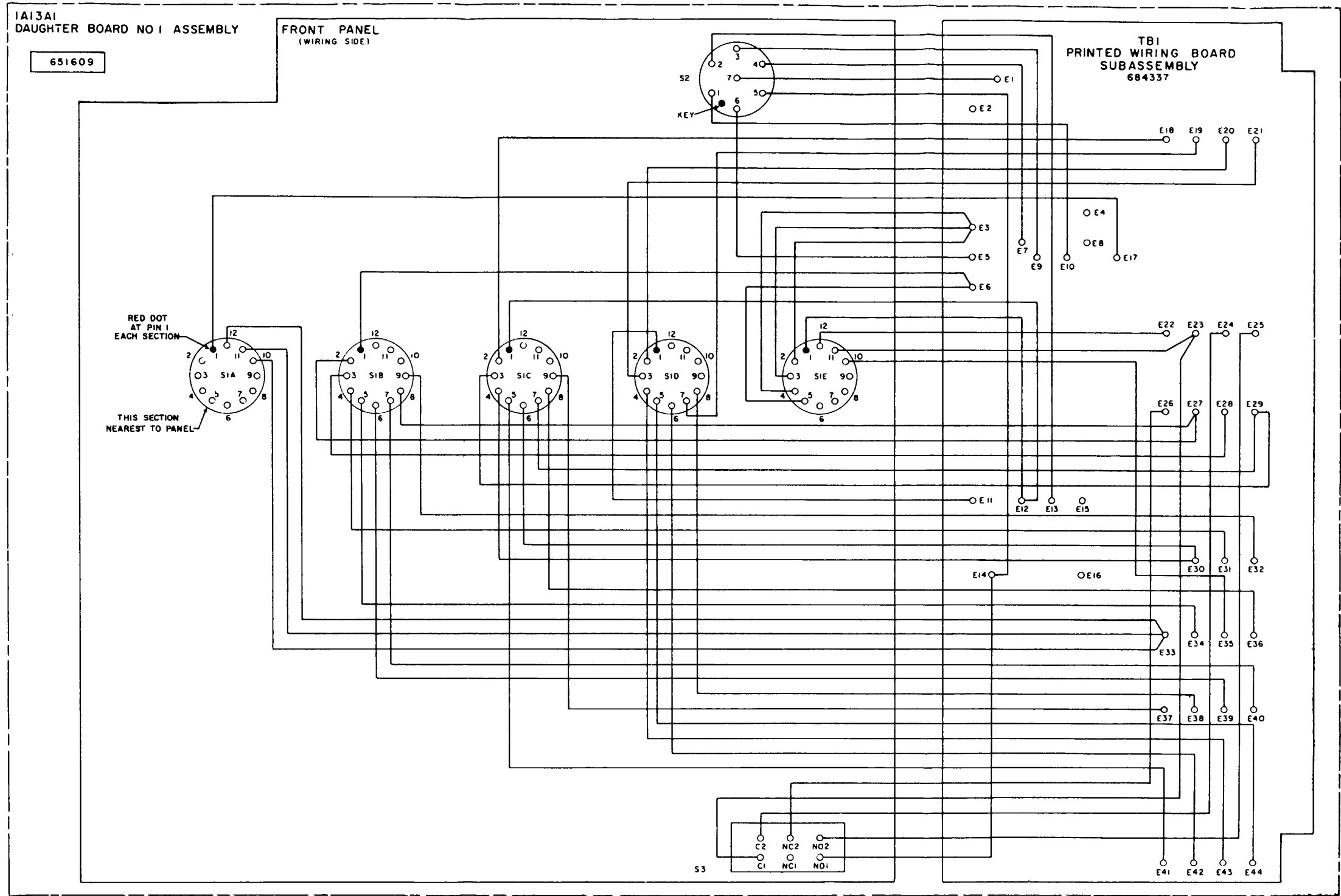
EL2IB060

Figure 5-83.10. Regenerator, digital 1A12A8, parts location diagram.

Change 6 5-184.19

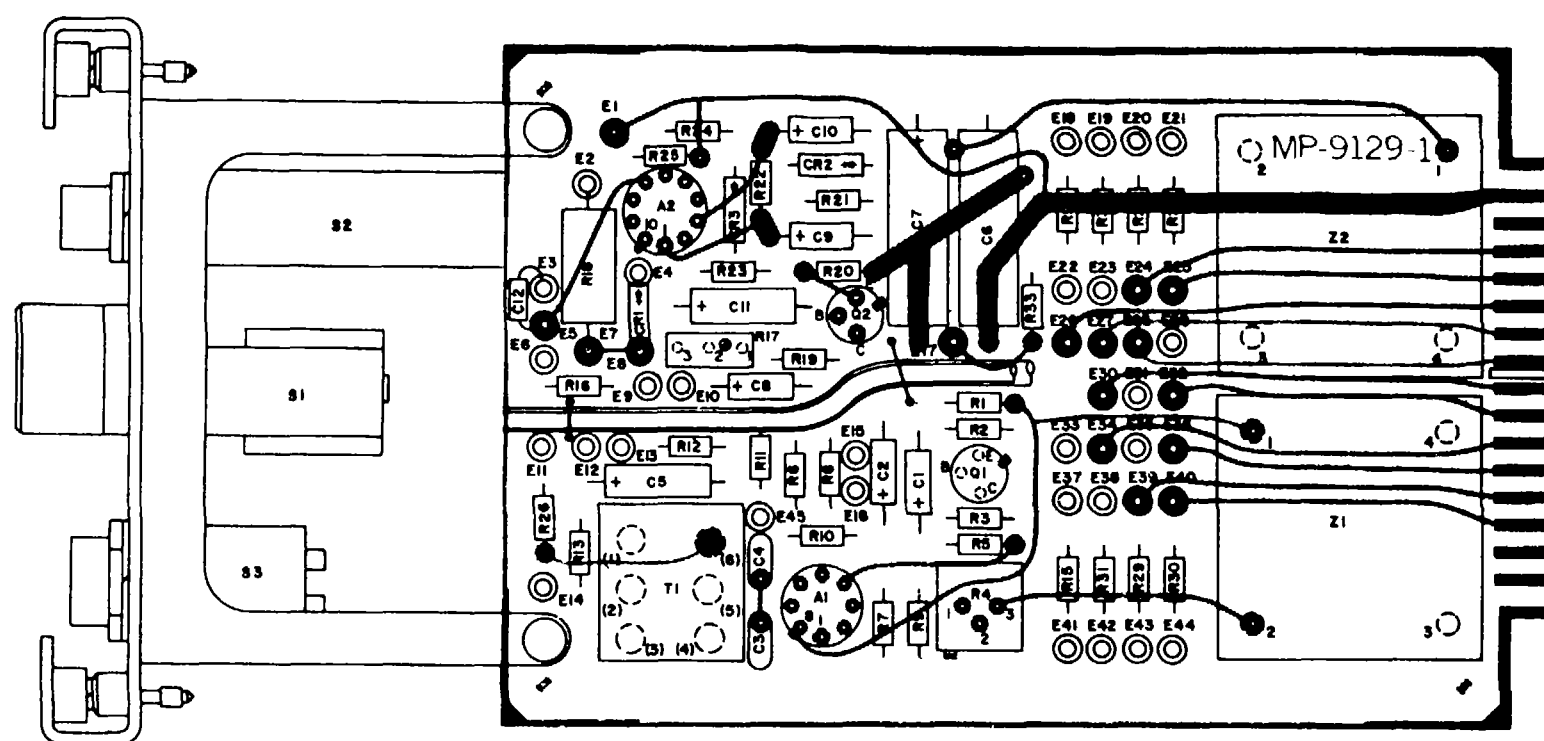
NOTES

- 1 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE REFERENCE DESIGNATION, PREFIX WITH 1A13A1
- 2 ALL WIRE IS NO 24 AWG STRANDED, TEFLON INSULATED
- 3 SWITCH S1 IS VIEWED FROM END OPPOSITE CONTROL KNOB SECTION A IS CLOSEST TO KNOB.

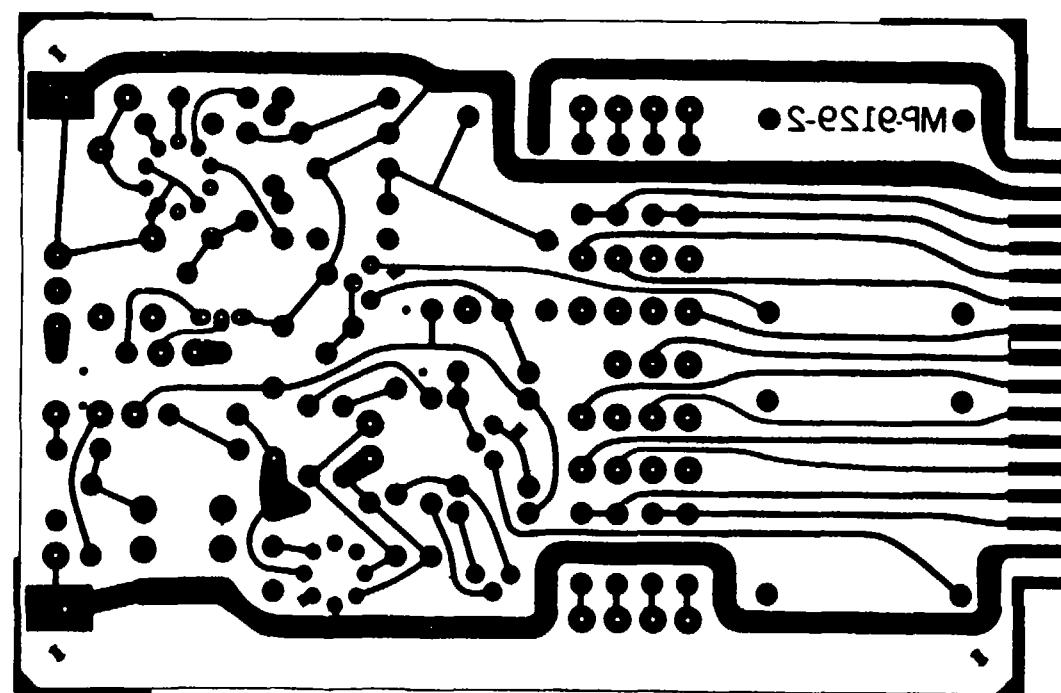


EL5820-695-35-TM-197

Figure 5-84. Daughter board No. 1 assembly 1A13A1, wiring diagram.



A. PARTS LOCATION AND WIRING ON FRONT OF BOARD AI (651609).



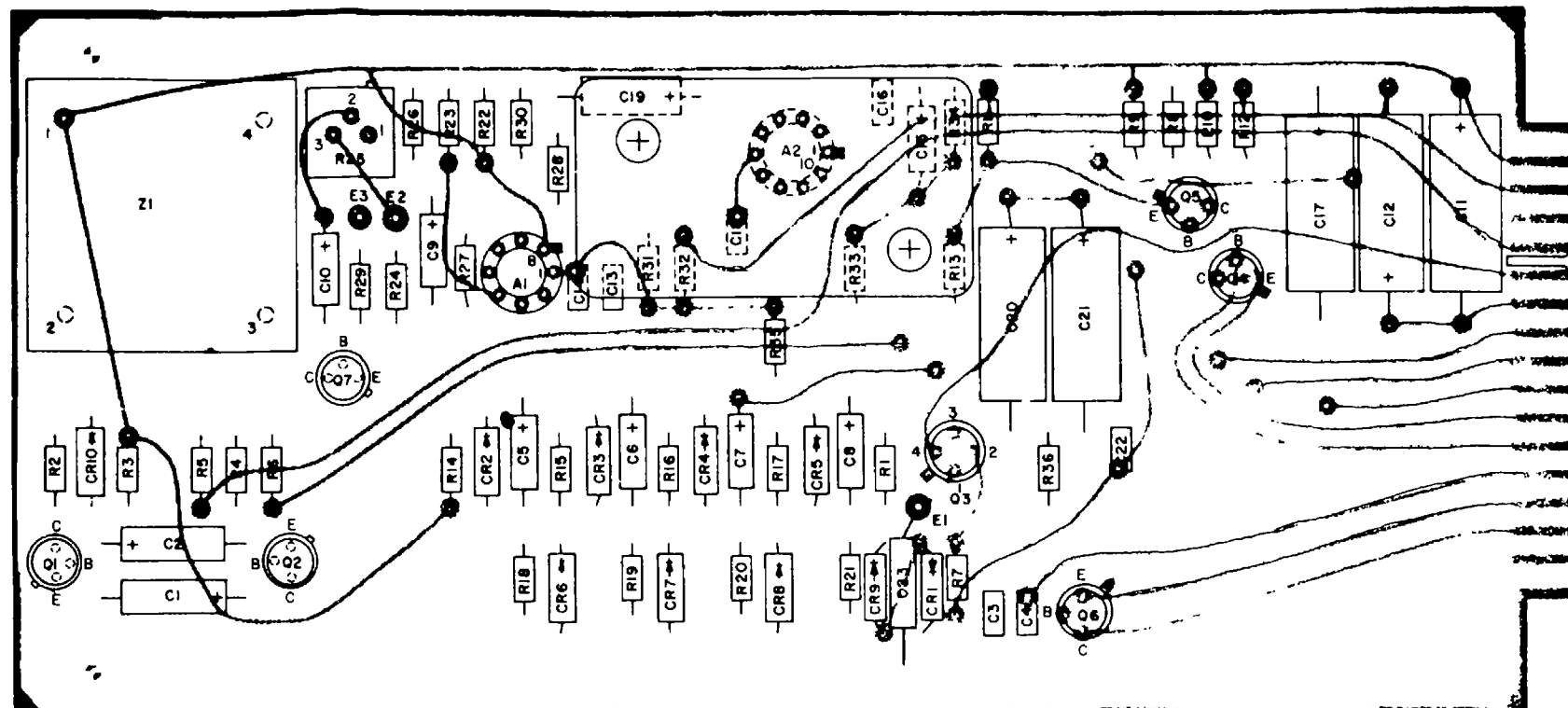
B WIRING ON BACK OF BOARD AI (VIEWED THROUGH FRONT)

EL5820-695-35-TM-CI-43

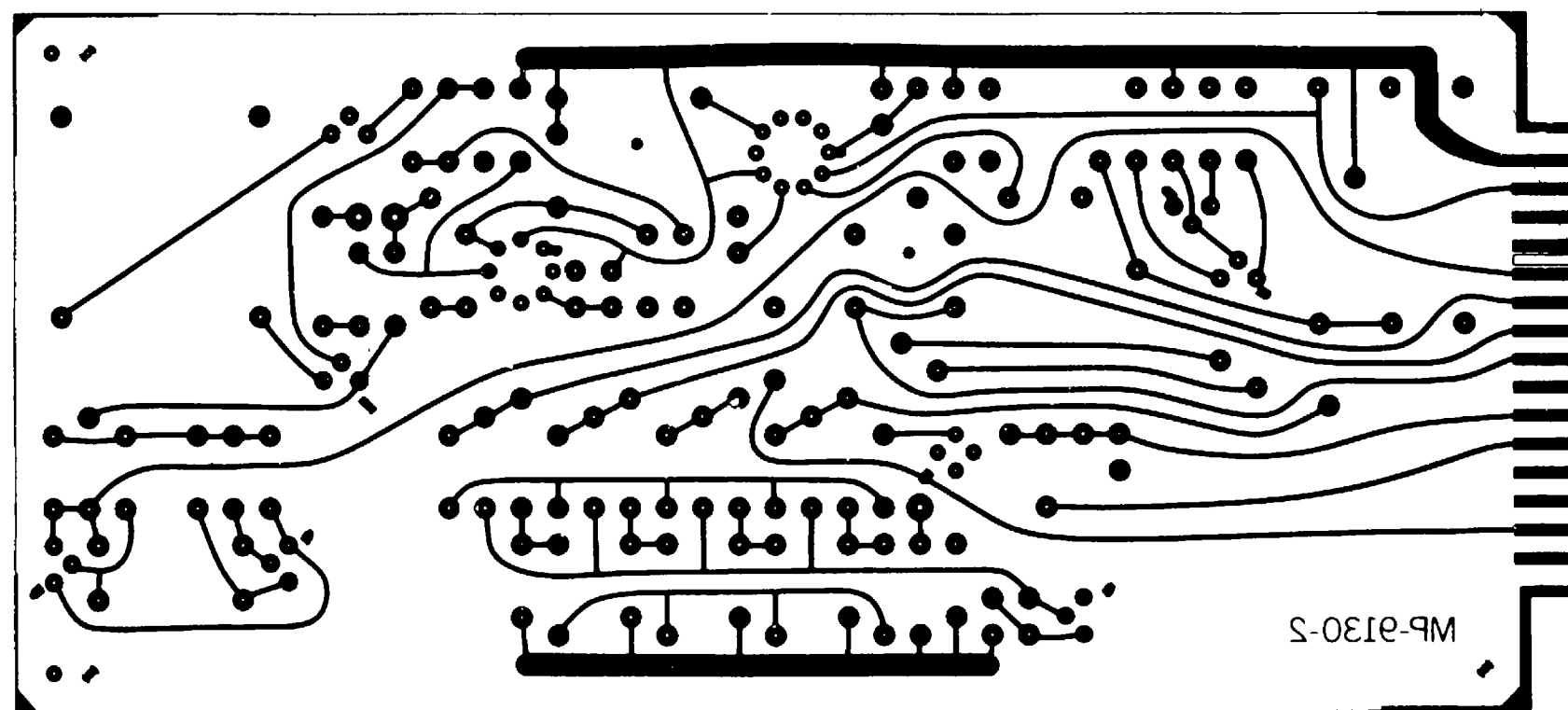
NOTES  
 PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN FOR COMPLETE  
 DESIGNATION, PREFIX WITH 1A13A1

Figure 5-85. Daughter board No. 1 assembly 1A13A1, parts-location and printed wiring diagram.

NOTE:  
 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN  
 FOR COMPLETE DESIGNATION, PREFIX WITH 1A13A2



A PARTS AND WIRING ON FRONT OF BOARD A2 (651610)



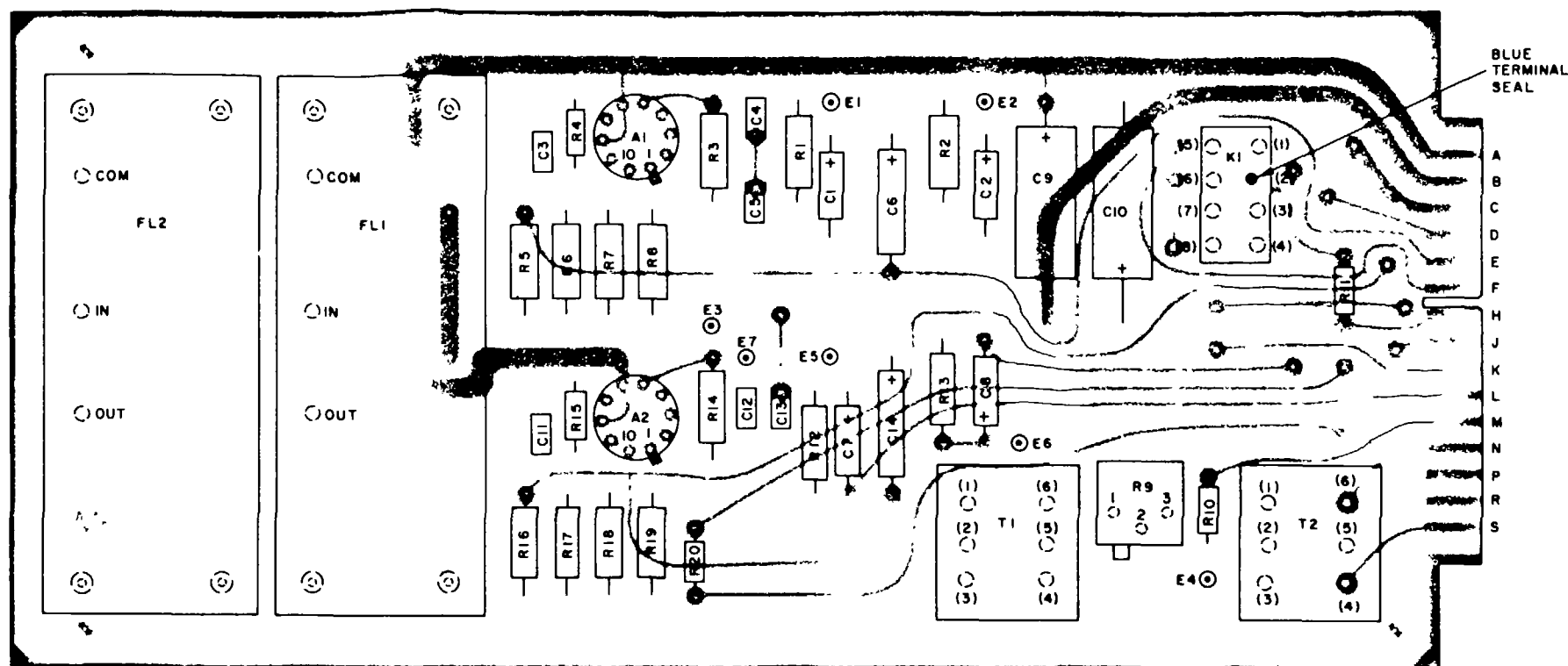
B WIRING ON BACK OF BOARD A2 (VIEWED THROUGH FRONT).

EL5820-695-35-TM-CI-44

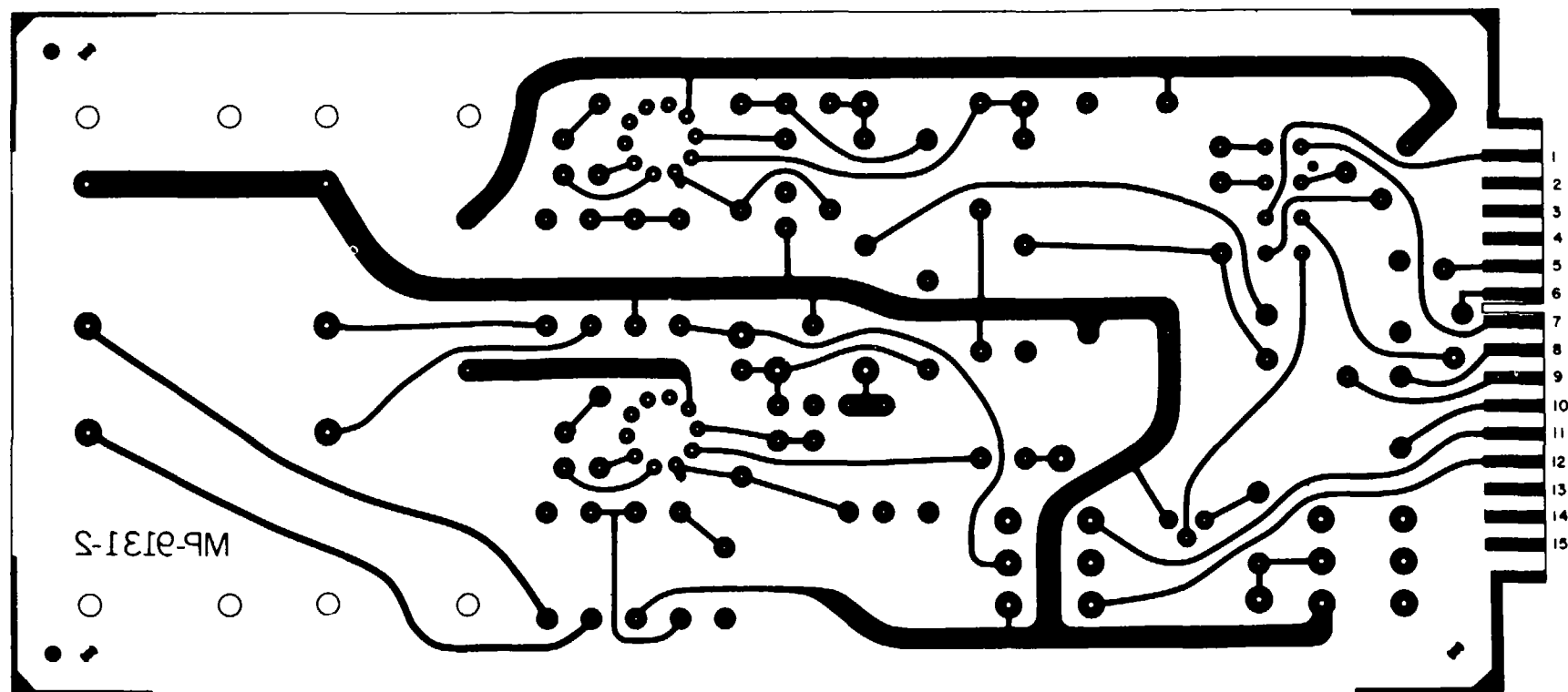
Figure 5-86. Daughter board No. 2 assembly 1A13A2, parts location and printed wiring diagram.

Change 1 5-189

NOTE  
 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN  
 FOR COMPLETE DESIGNATION, PREFIX WITH 1A13A3



A PARTS AND WIRING ON FRONT OF BOARD A3 (651611)

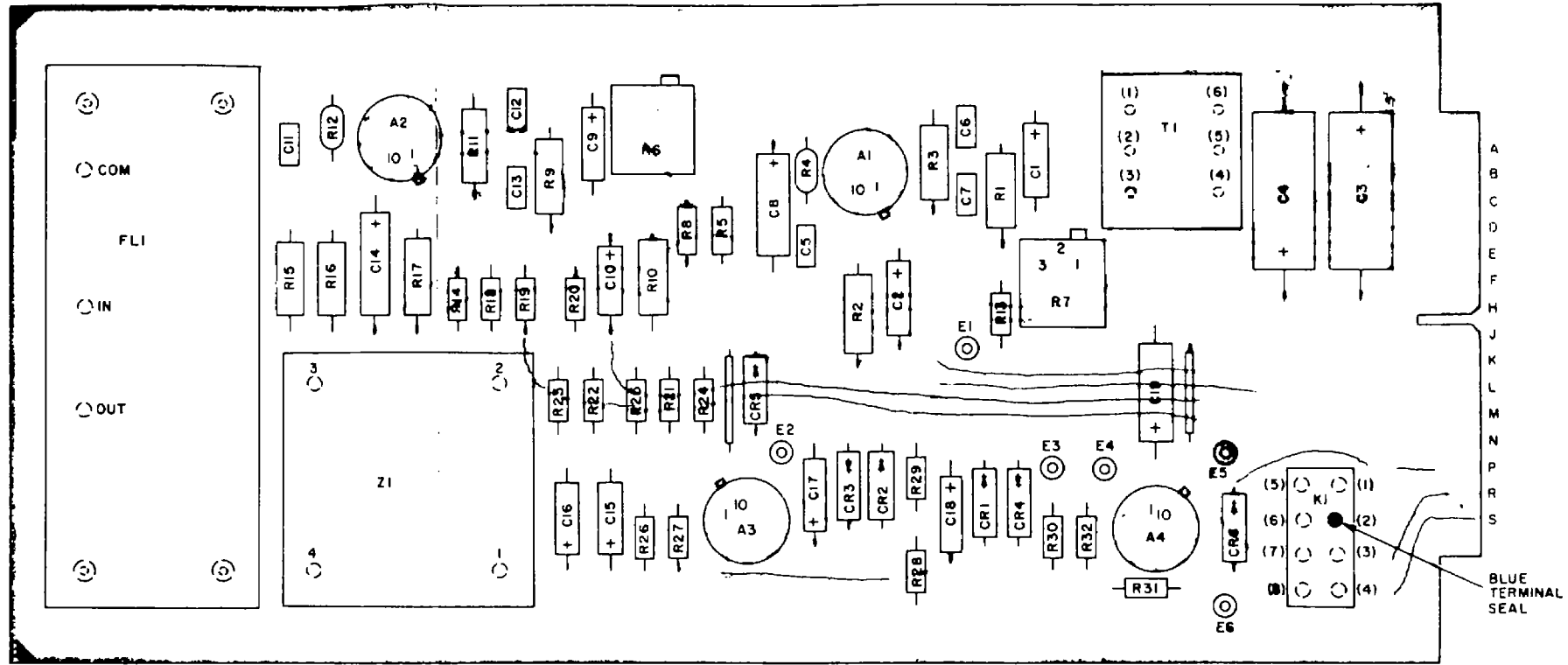


B. WIRING ON BACK OF BOARD A3 (VIEWED THROUGH FRONT)

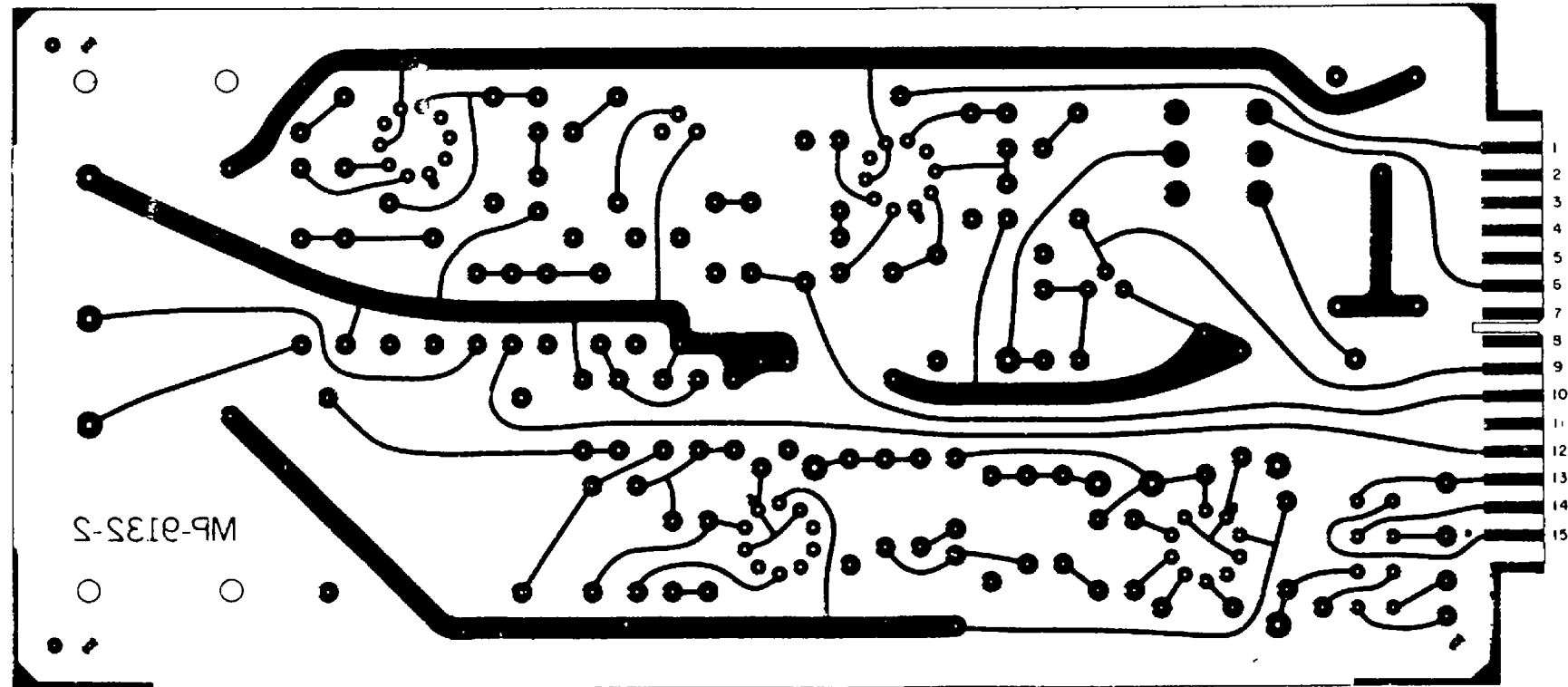
EL5820-695-35-TM-200

Figure 5-87. Daughter board No. 3 assembly 1A13A3, parts location and printed wiring diagram.

NOTE  
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN  
FOR COMPLETE DESIGNATION, PREFIX WITH 1A13A4



A PARTS AND WIRING ON FRONT OF BOARD A4 (651612)

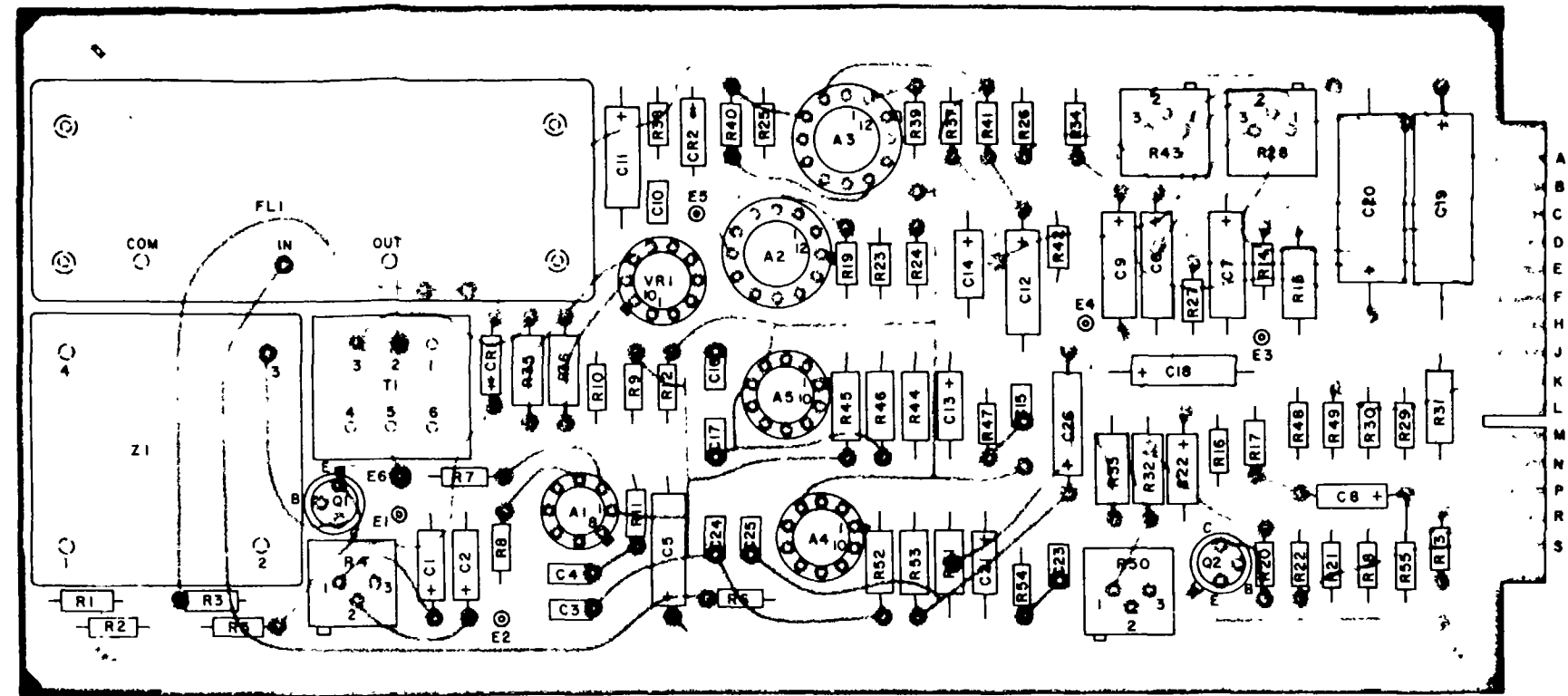


B WIRING ON BACK OF BOARD A4 (VIEWED THROUGH FRONT)

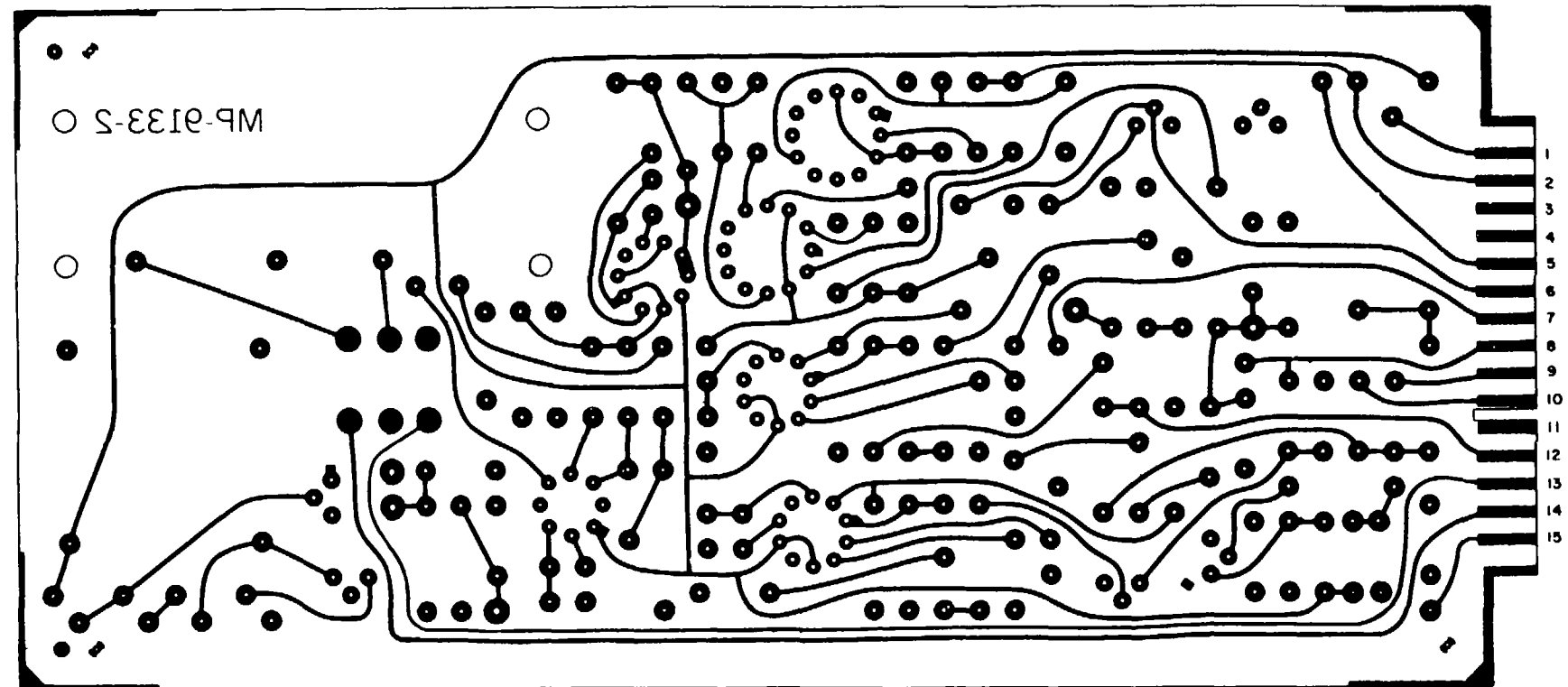
EL5820-695-35-TM-201

Figure 5-88. Daughter board No. 4 assembly 1A13A4, parts location and printed wiring diagram.

NOTE:  
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN  
FOR COMPLETE DESIGNATION, PREFIX WITH 1A13A5



A PARTS AND WIRING ON FRONT OF BOARD A5 (651613)



B WIRING ON BACK OF BOARD A5 (VIEWED THROUGH FRONT).

EL5820-695-35-TM-CI-45

Figure 5-89. Daughter board No. 5 assembly 1A13A5, parts location and printed wiring diagram.  
Change 1 5-195

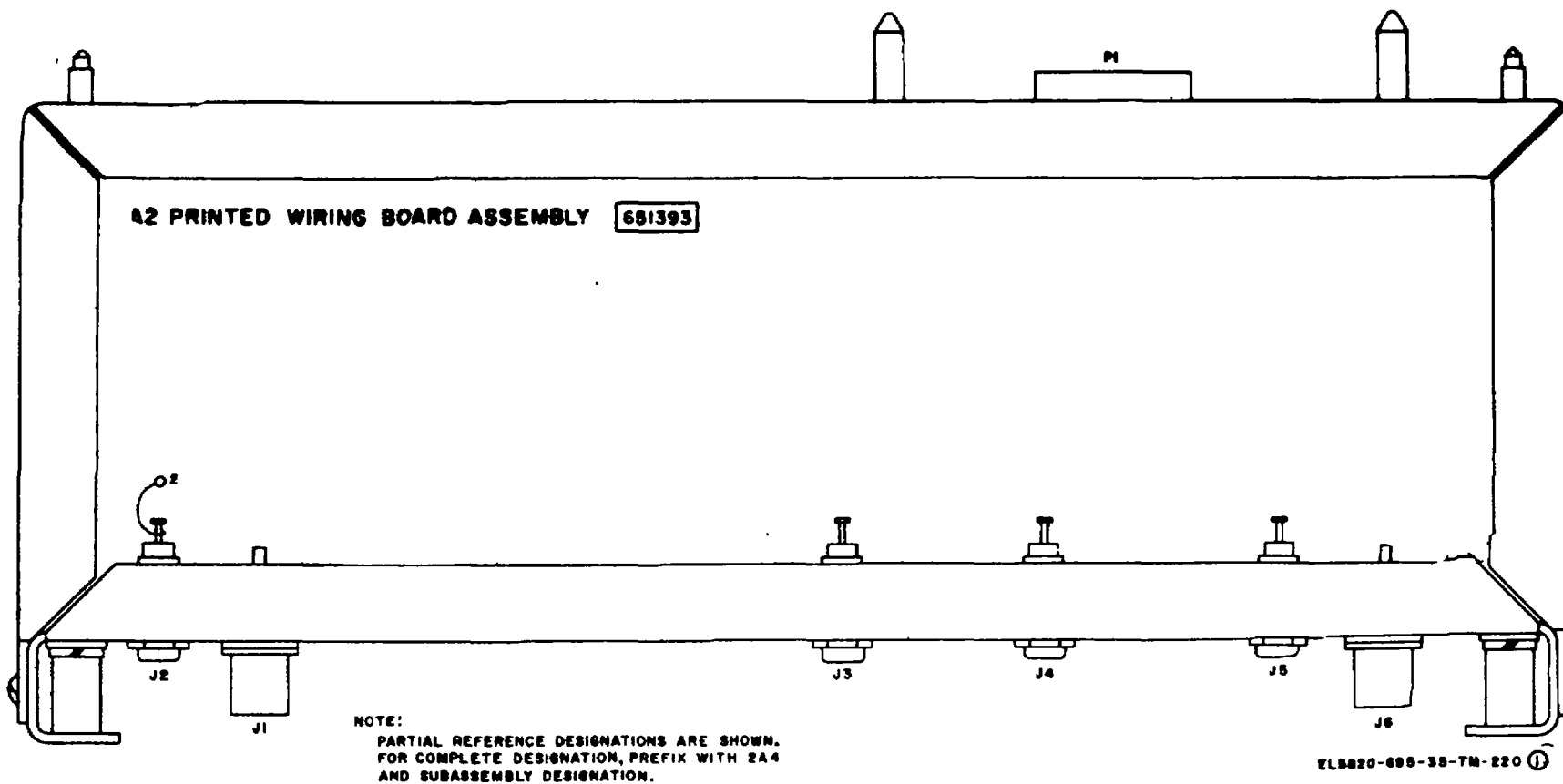
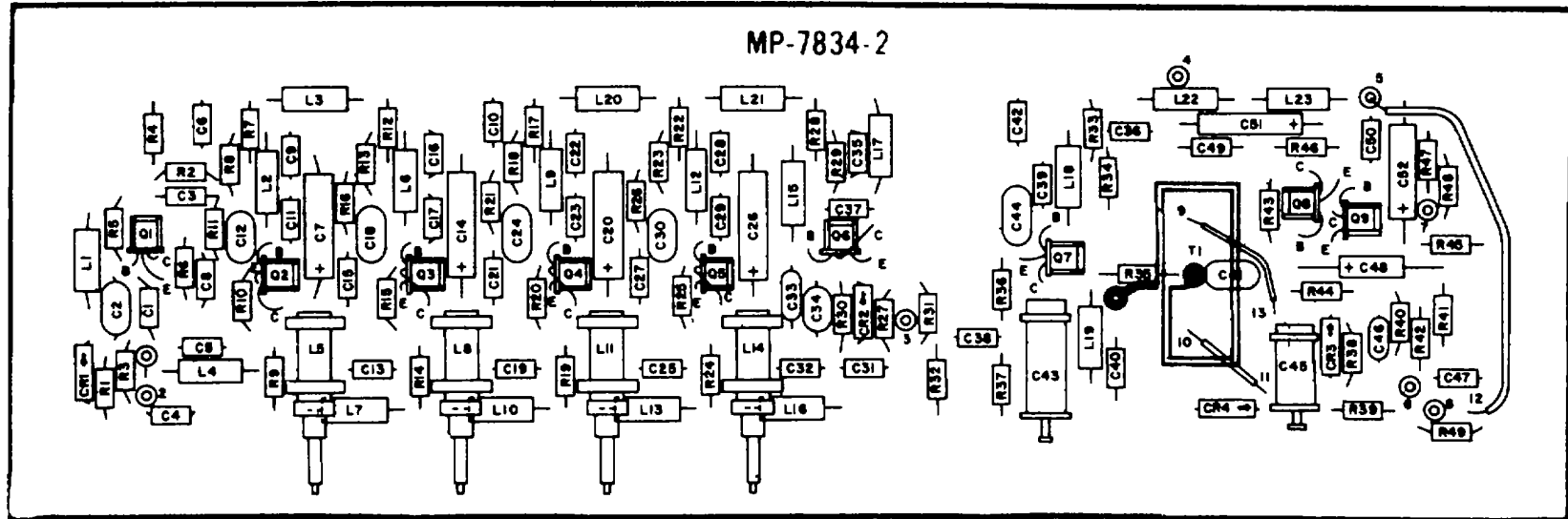
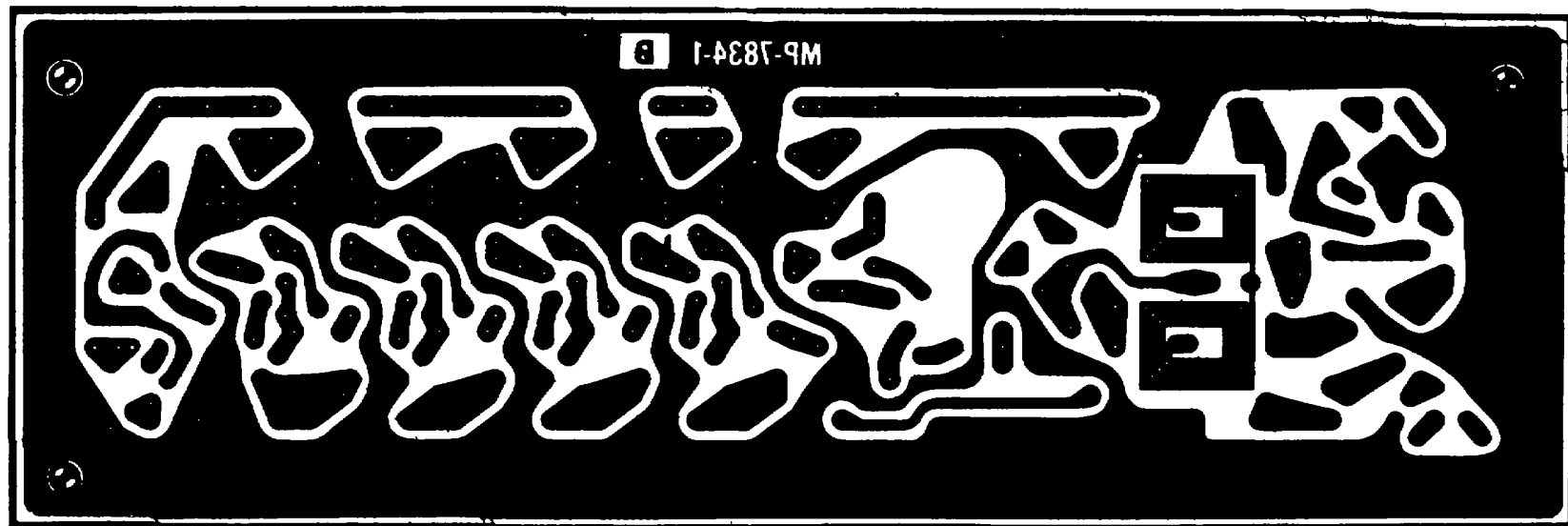


Figure 5-90 (1). Demodulator 2A4, parts location and printed wiring diagram (part 1 of 2)





A. PARTS AND WIRING ON FRONT OF BOARD A2

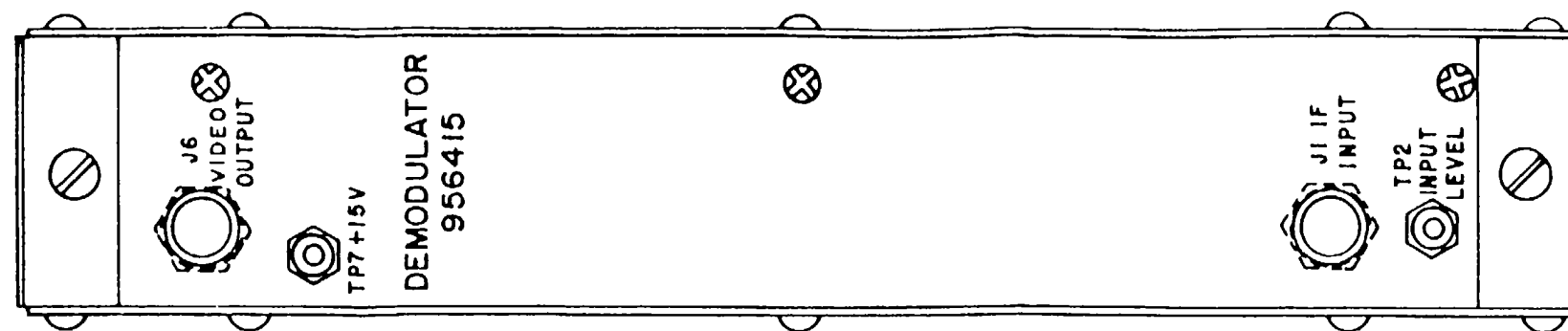


B. WIRING ON BACK OF BOARD A2 (VIEWED THROUGH FRONT)

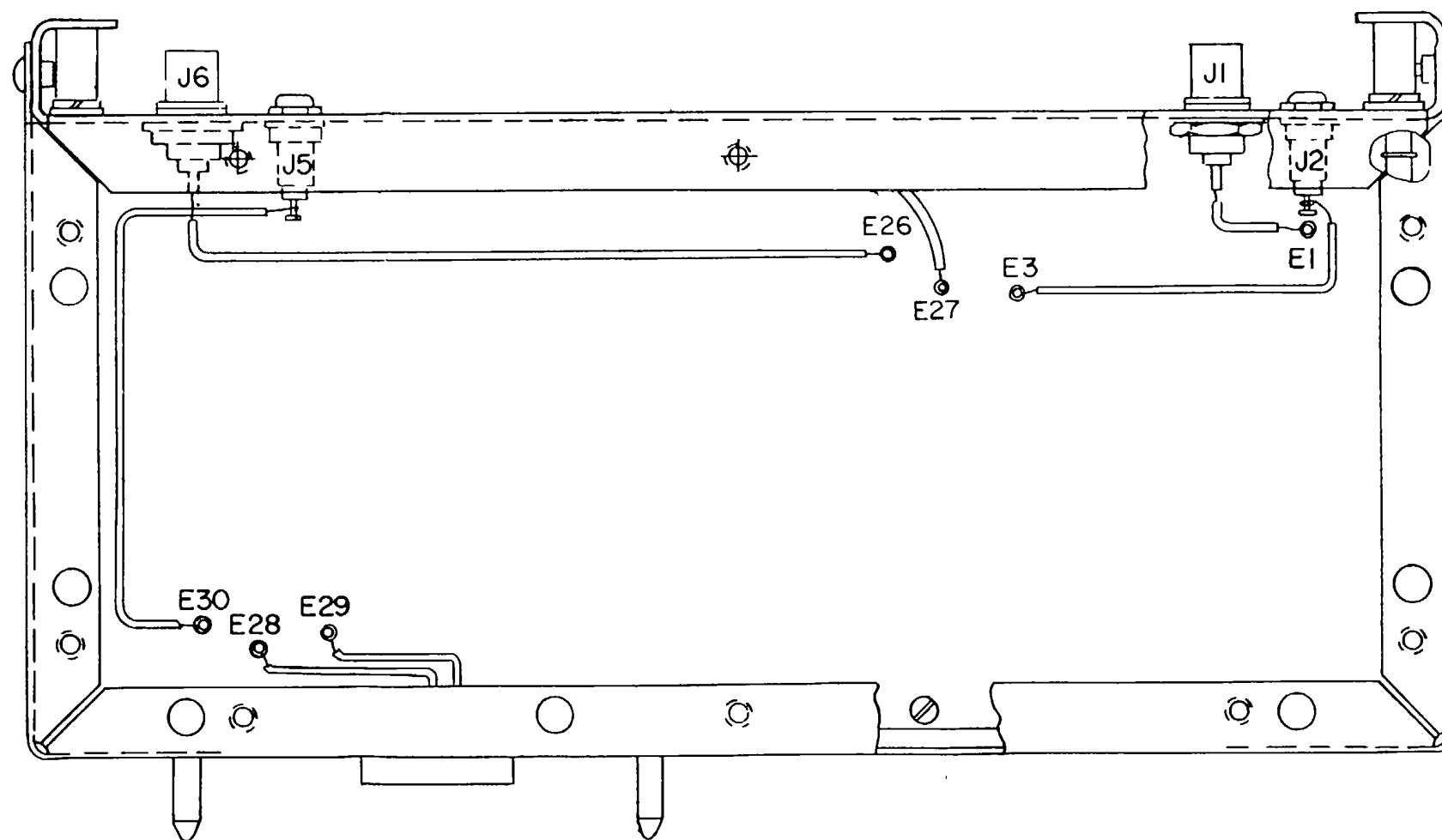
EL5820-695-35-TM-220 ③

Figure 5-90 (2). Demodulator 2A4, parts location and printed wiring diagram (part 2 of 2).

NOTE:  
PARTIAL REFERENCE DESIGNATIONS ARE  
SHOWN. FOR COMPLETE DESIGNATION,  
PREFIX WITH 2A4.



FRONT VIEW OF 2A4

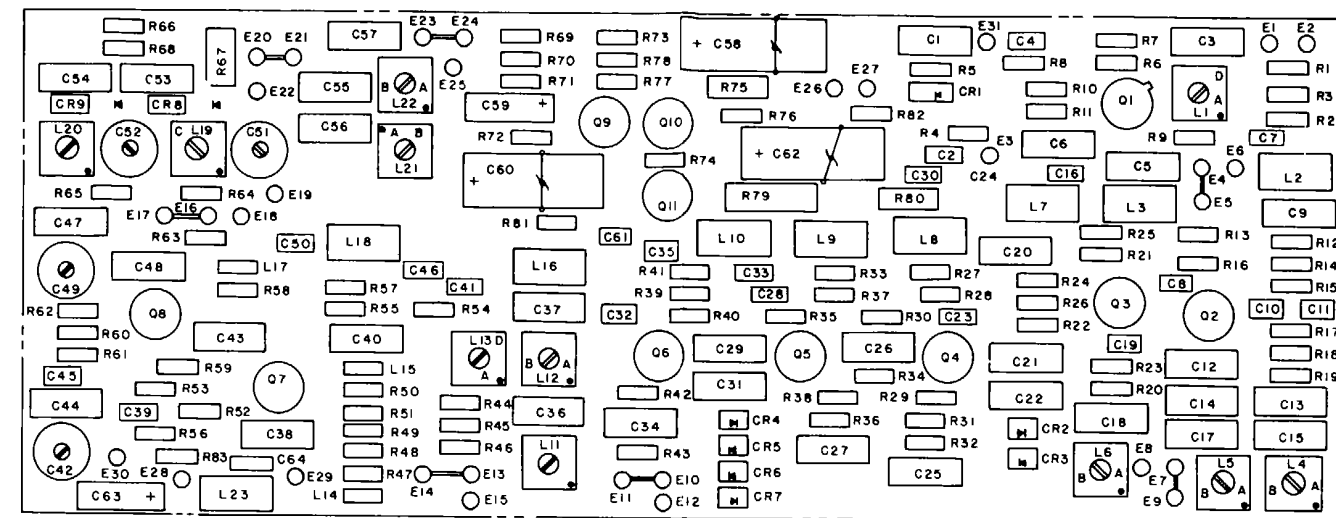
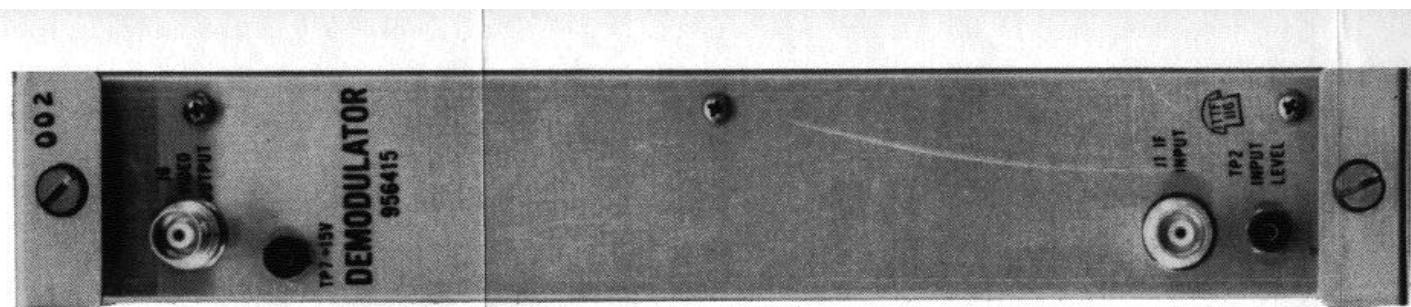


SIDE VIEW OF 2A4

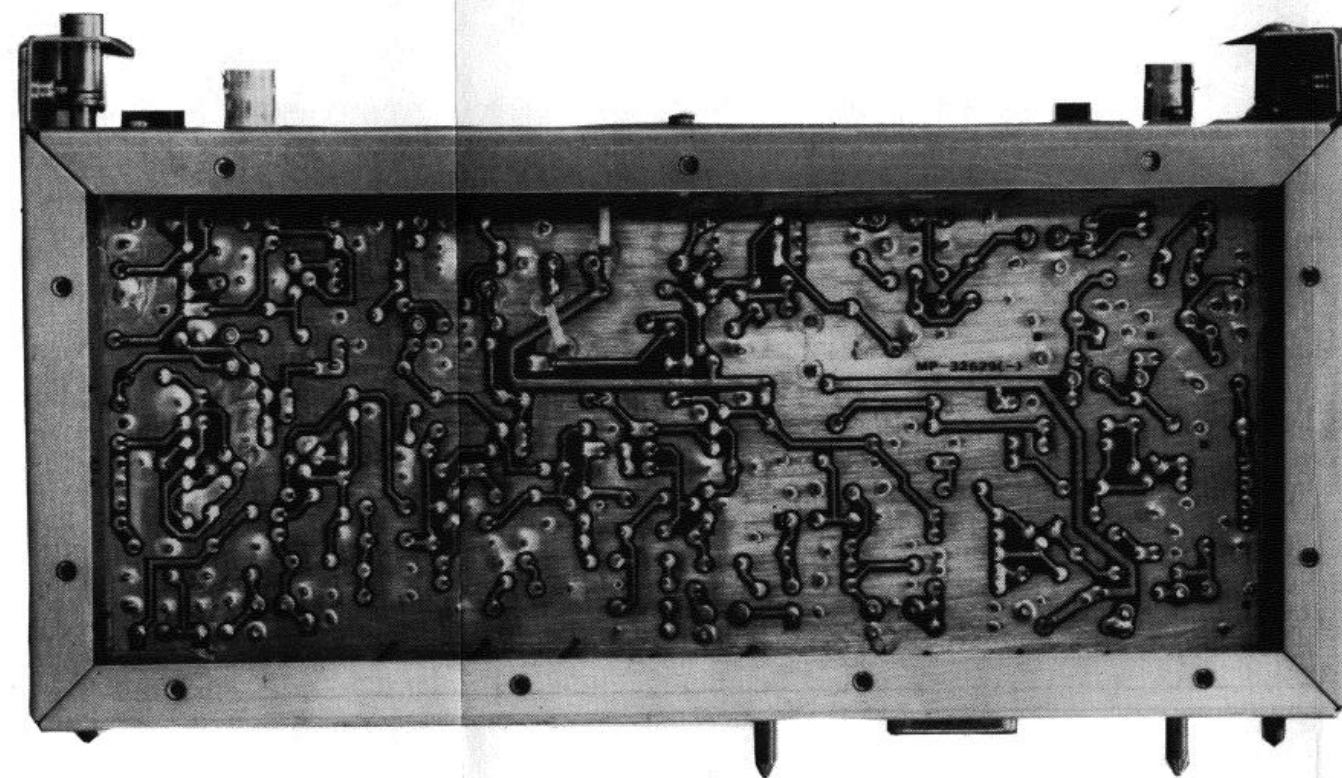
EL2IB108

Figure 5-90.1(1). Demodulator 2A4 (956415), parts location and printed wiring diagram (sheet 1 of 2)

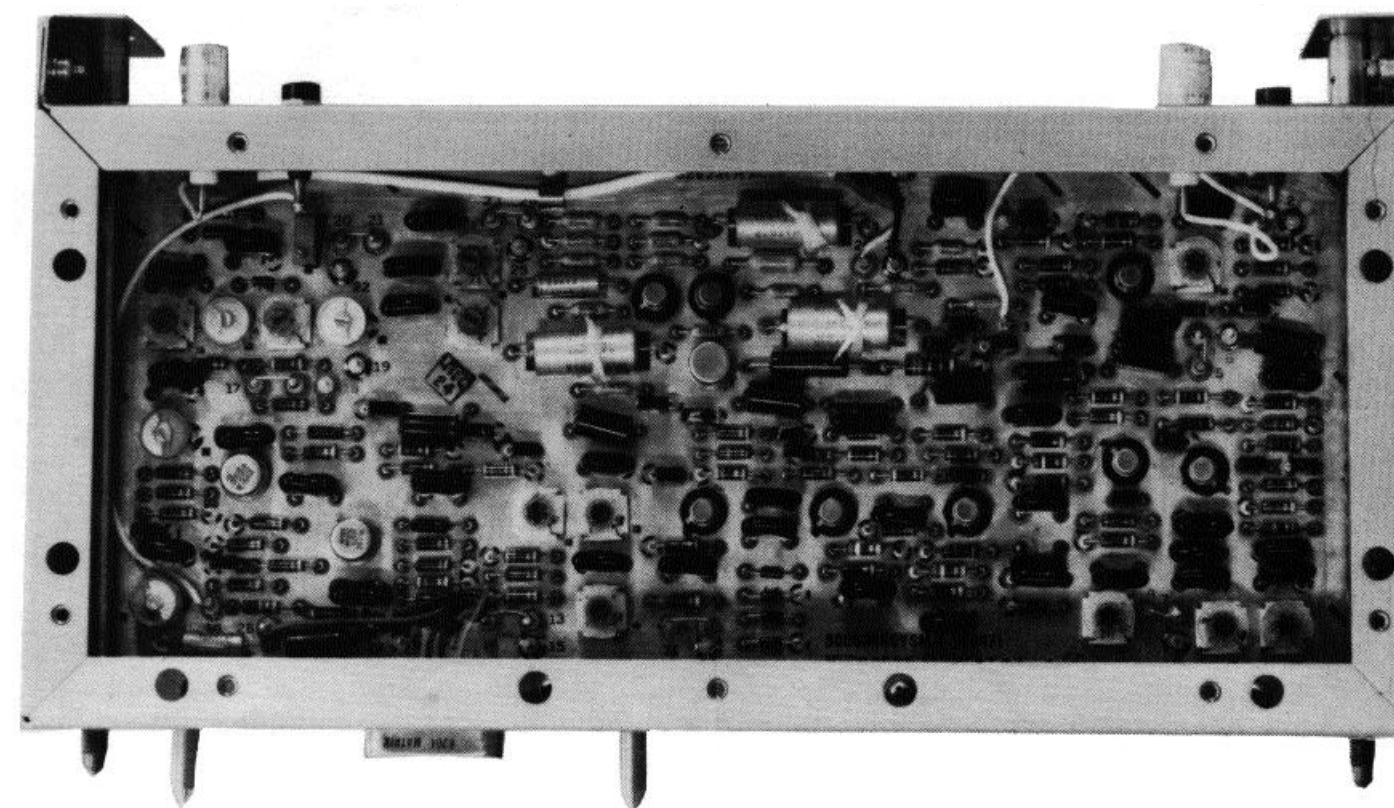
Change 6 5-198.1



A. REFERENCE DESIGNATIONS OF PARTS ON FRONT OF BOARD 2A4 (956471)



C. WIRING ON BACK OF BOARD



B. PARTS AND WIRING ON FRONT OF BOARD 2A4

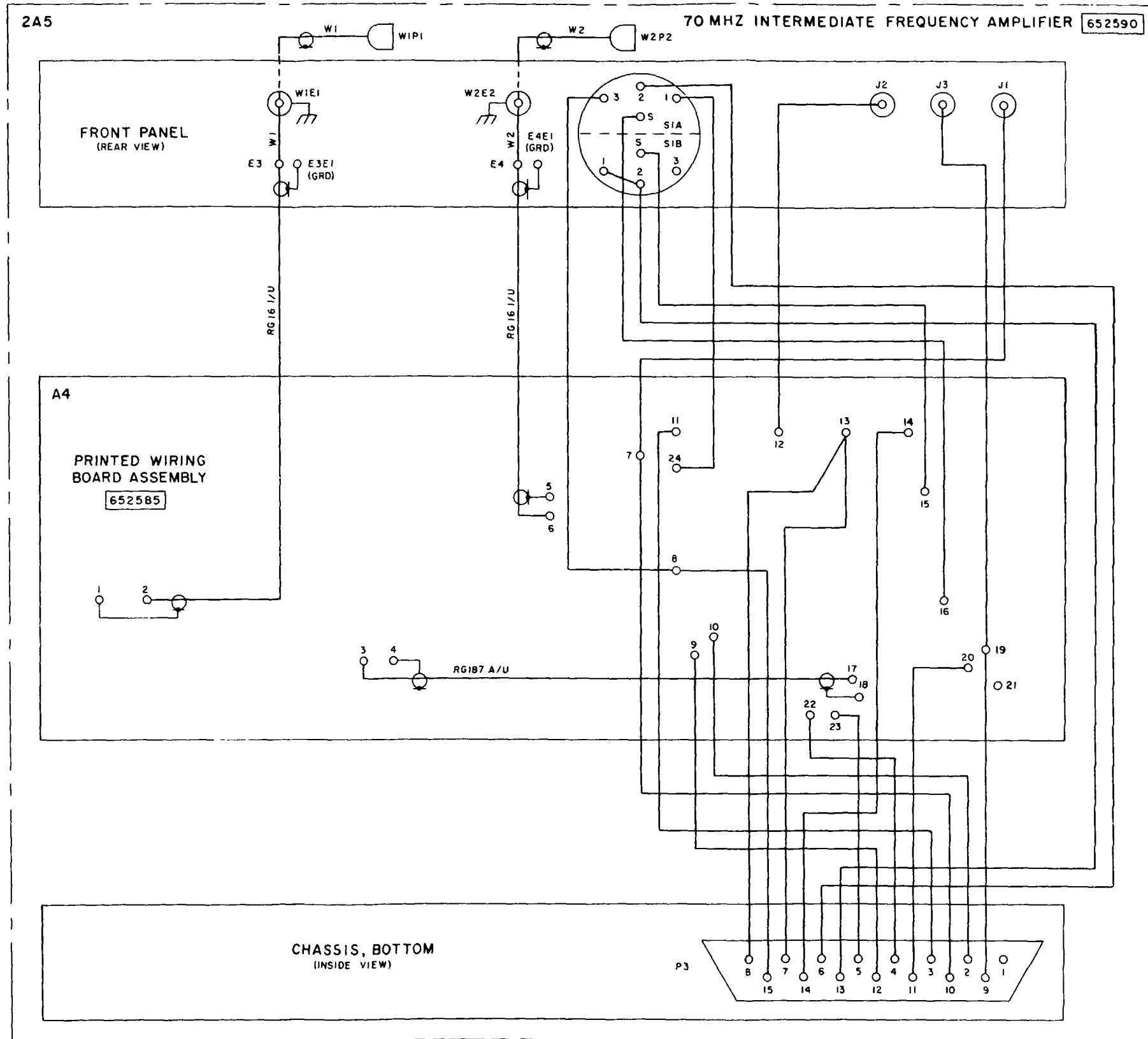
EL2IB147

Figure 5-90.1 (2). Demodulator 2A4 (956415), parts location and printed wiring diagram (sheet 2 of 2)

Change 6 5-198.3

NOTES

- 1 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATIONS
- 2 ALL WIRE IS NO 22 AWG STRANDED, TEFLON INSULATED



EL5820-695-35-TM-221

Figure 5-91 70 MHz intermediate frequency amplifier 2A5, wiring diagram.

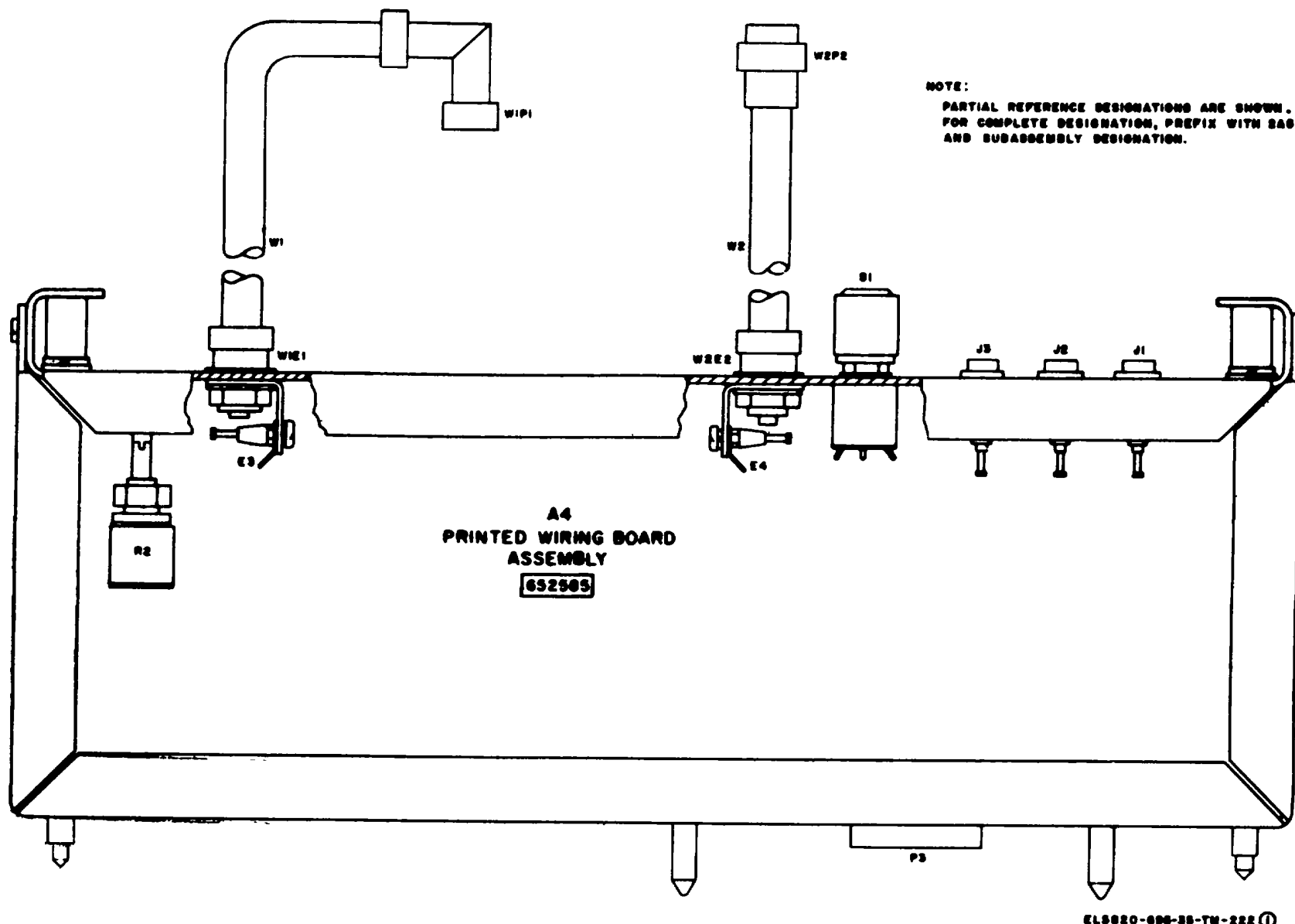
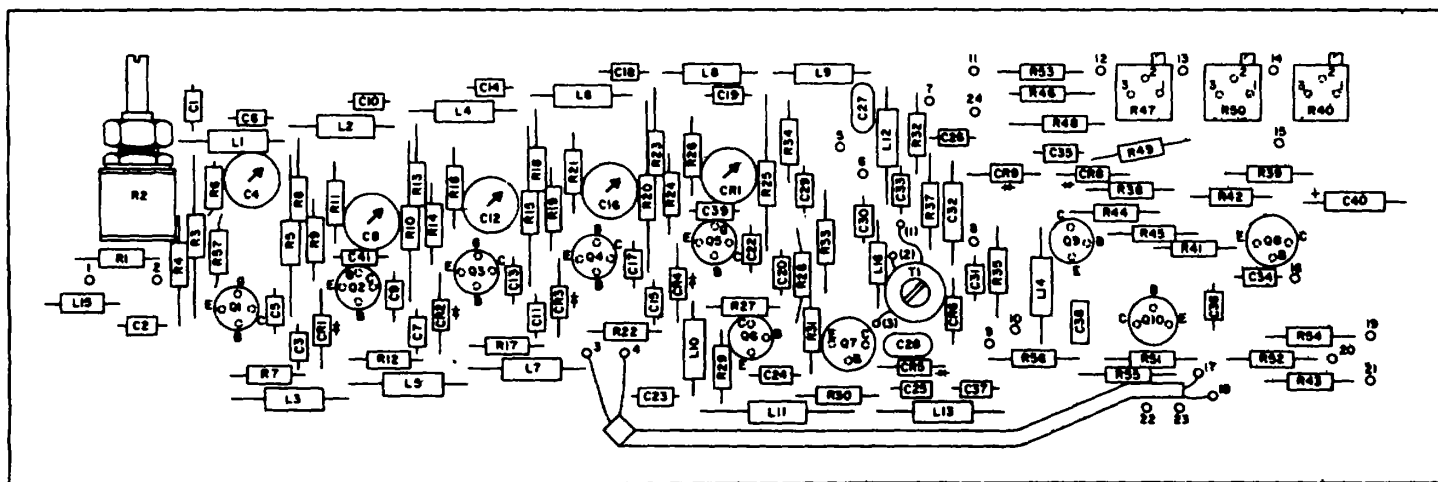
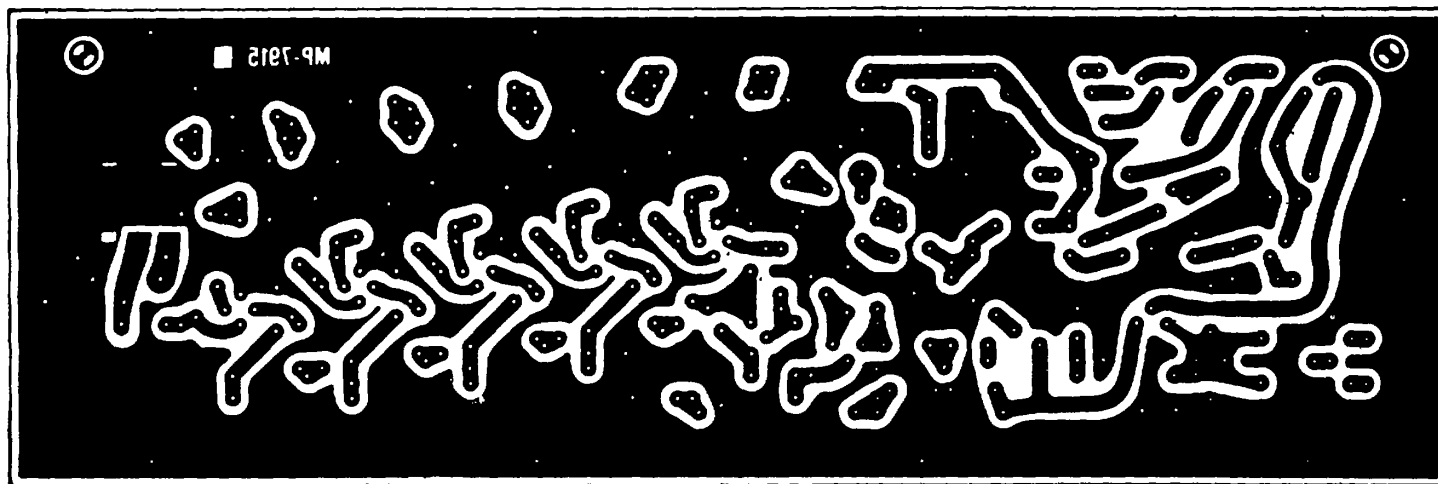


Figure 5-92(1). 70 MHz intermediate frequency amplifier 2A5, parts location and printed wiring diagram (part 1 of 2).



A. PARTS AND WIRING ON FRONT OF BOARD A4 (652585)

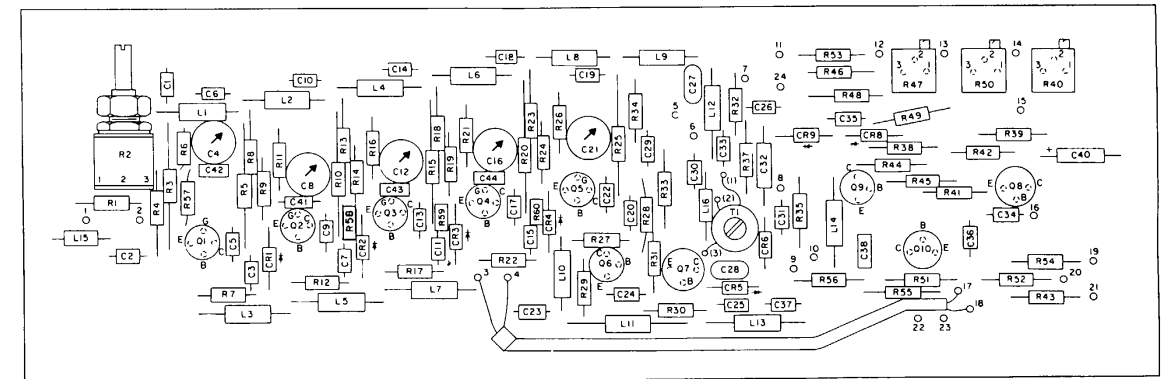
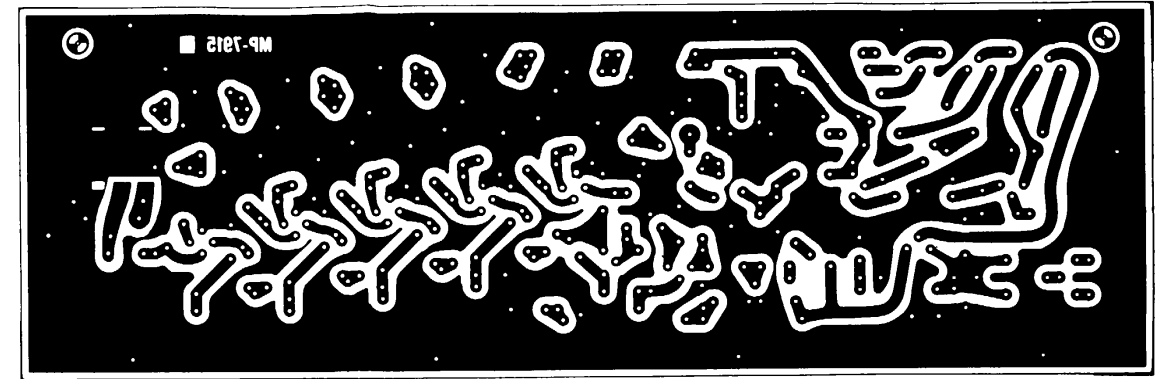
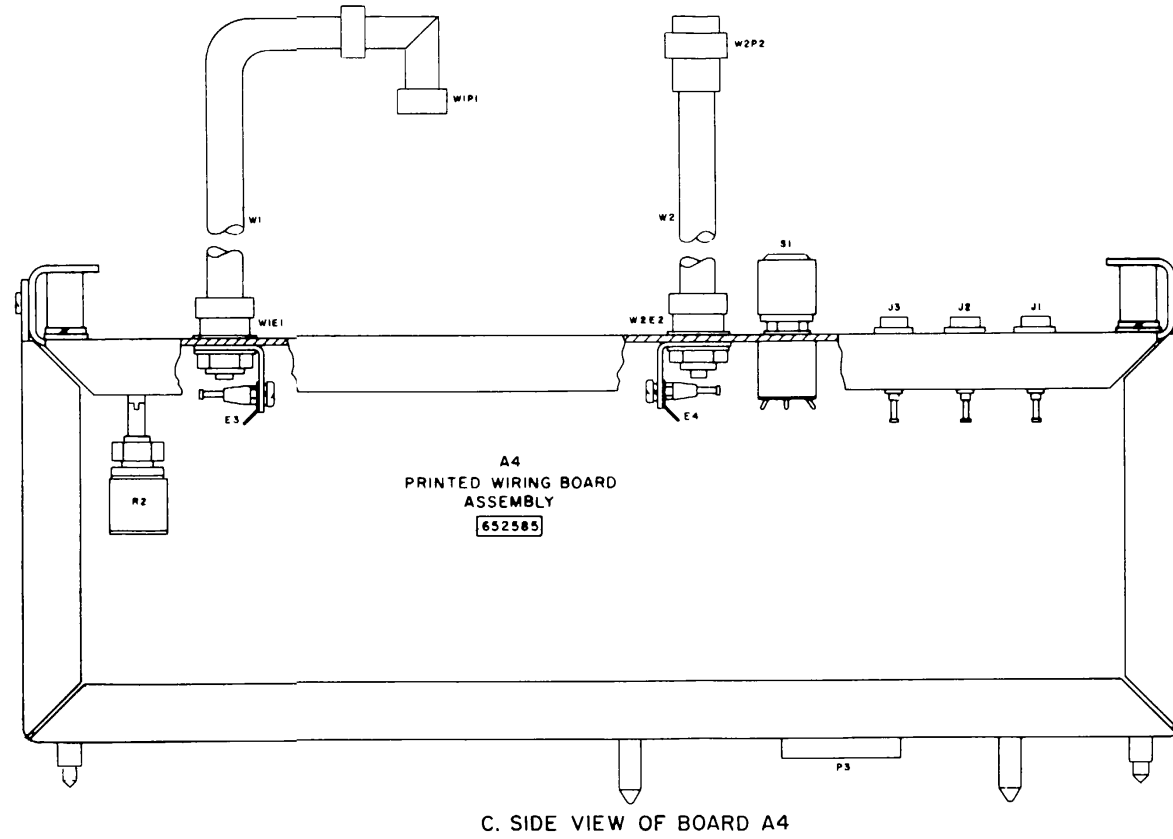
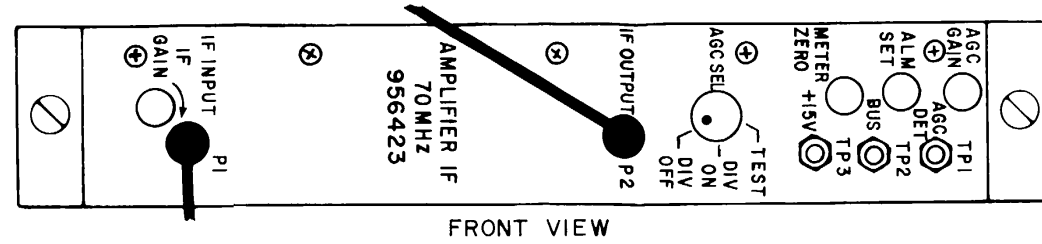
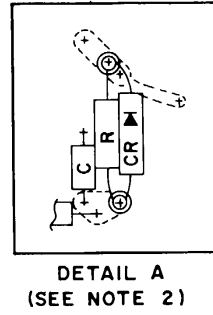


B. WIRING ON BACK OF BOARD A4 (VIEWED THROUGH FRONT

EL5820-35-TM-222(2)

Figure 5-92(2). 70 MHz intermediate frequency amplifier 2A5, parts location and printed wiring diagram (part 2 of 2).

- NOTE:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH 2A5 AND SUBASSEMBLY DESIGNATION.
  2. DETAIL APPLIES TO C7, R58, CR2; C11, R59, CR3; AND C15, R60, CR4.



SEE DETAIL A

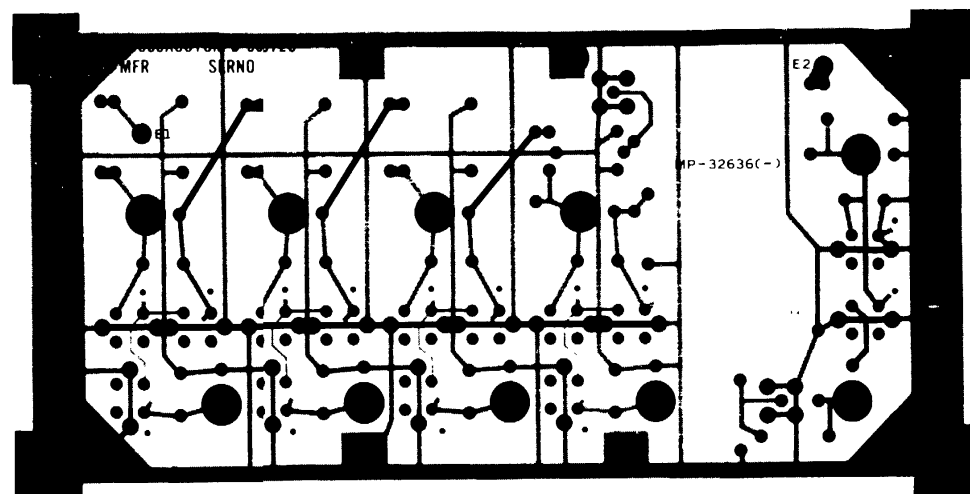
A. PARTS ON FRONT OF BOARD A4 (652585)

EL2IB081

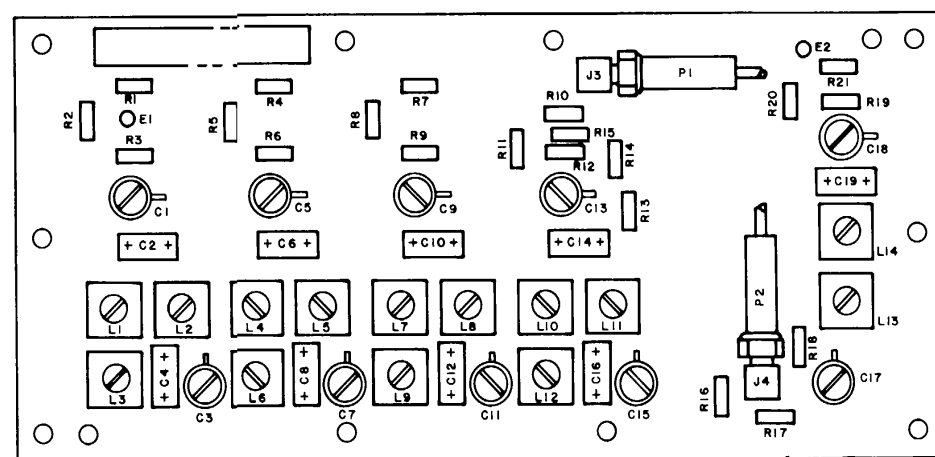
Figure 5-92.1. 70 MHz intermediate frequency amplifier 2A5 (956423) parts location diagram.

Change 6 5-202.1

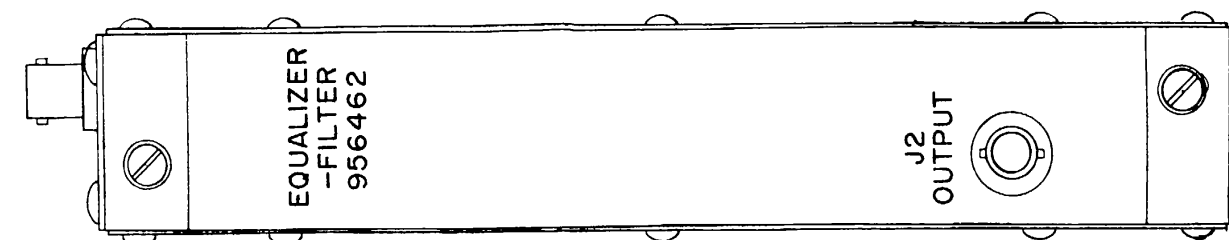
NOTE  
 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN  
 FOR COMPLETE DESIGNATION, PREFIX WITH 2A6  
 AND SUB-ASSEMBLY DESIGNATION



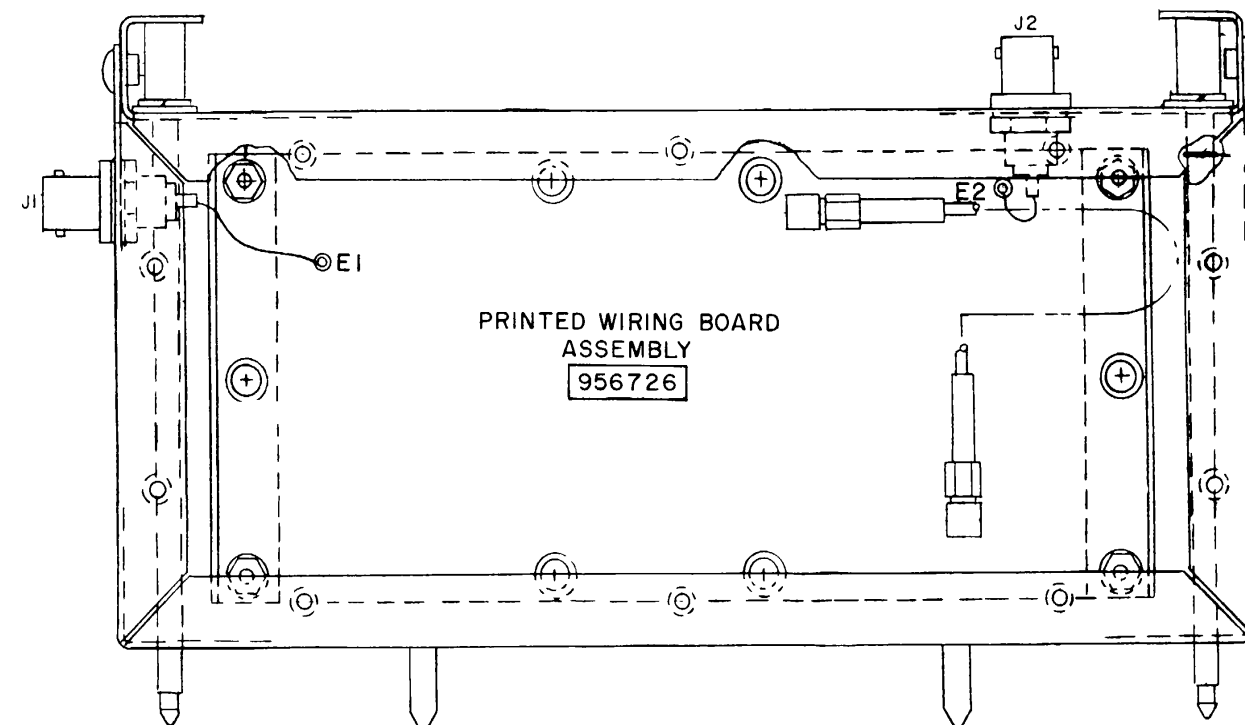
C. PRINTED BOARD FRONT AND REAR WIRING



A. ASSEMBLY 2A6 COMPONENTS



D. FRONT VIEW OF 2A6



B. SIDE VIEW OF 2A6

EL21B129

Figure 5-92.2 Equalizer filter 2A6, parts location diagram.

Change 6 5-202.3



- NOTE
- 1 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 2A7 NUMBER AND SUBASSEMBLY DESIGNATION.
  - 2 ALL WIRE IS NO 22 AWG STRANDED, TEFLON INSULATED

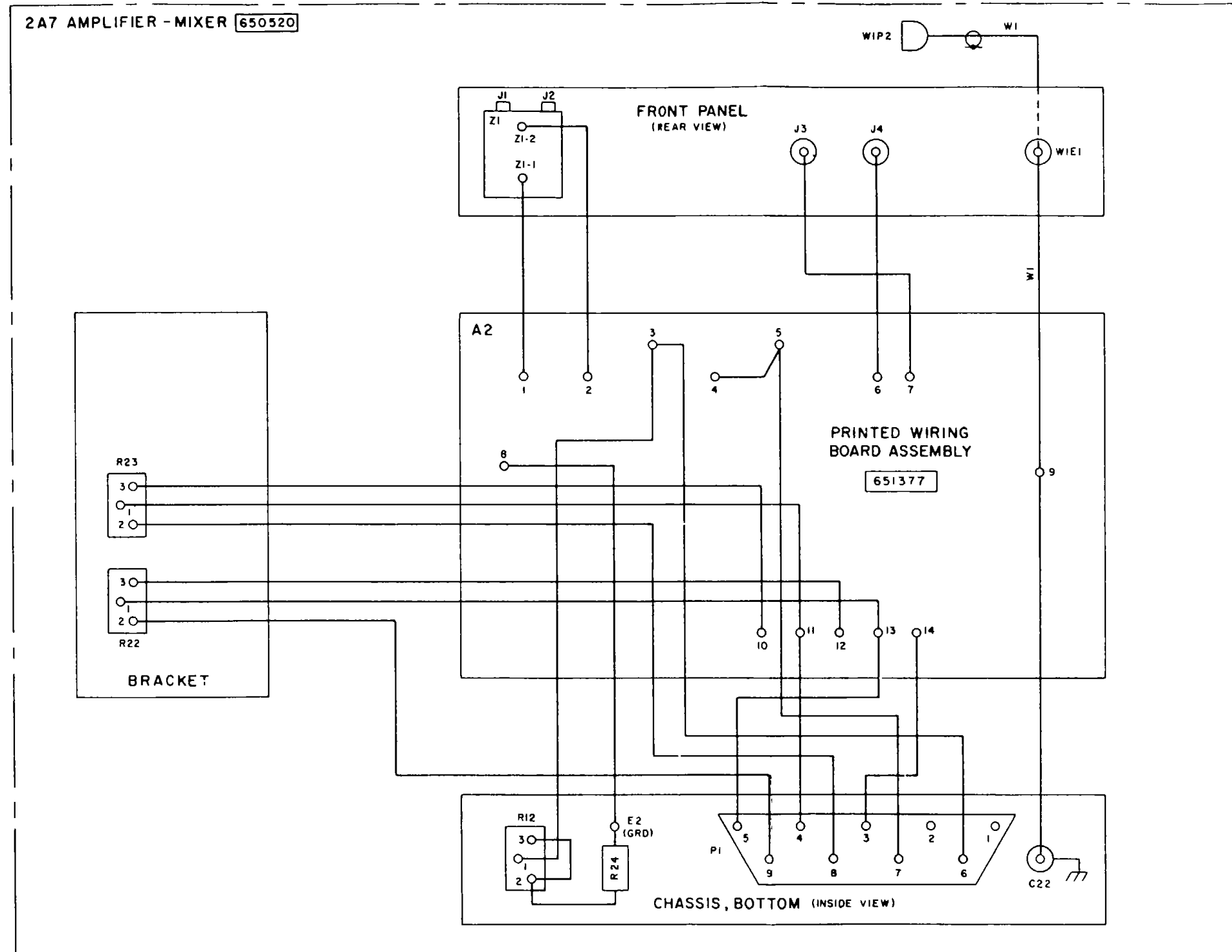
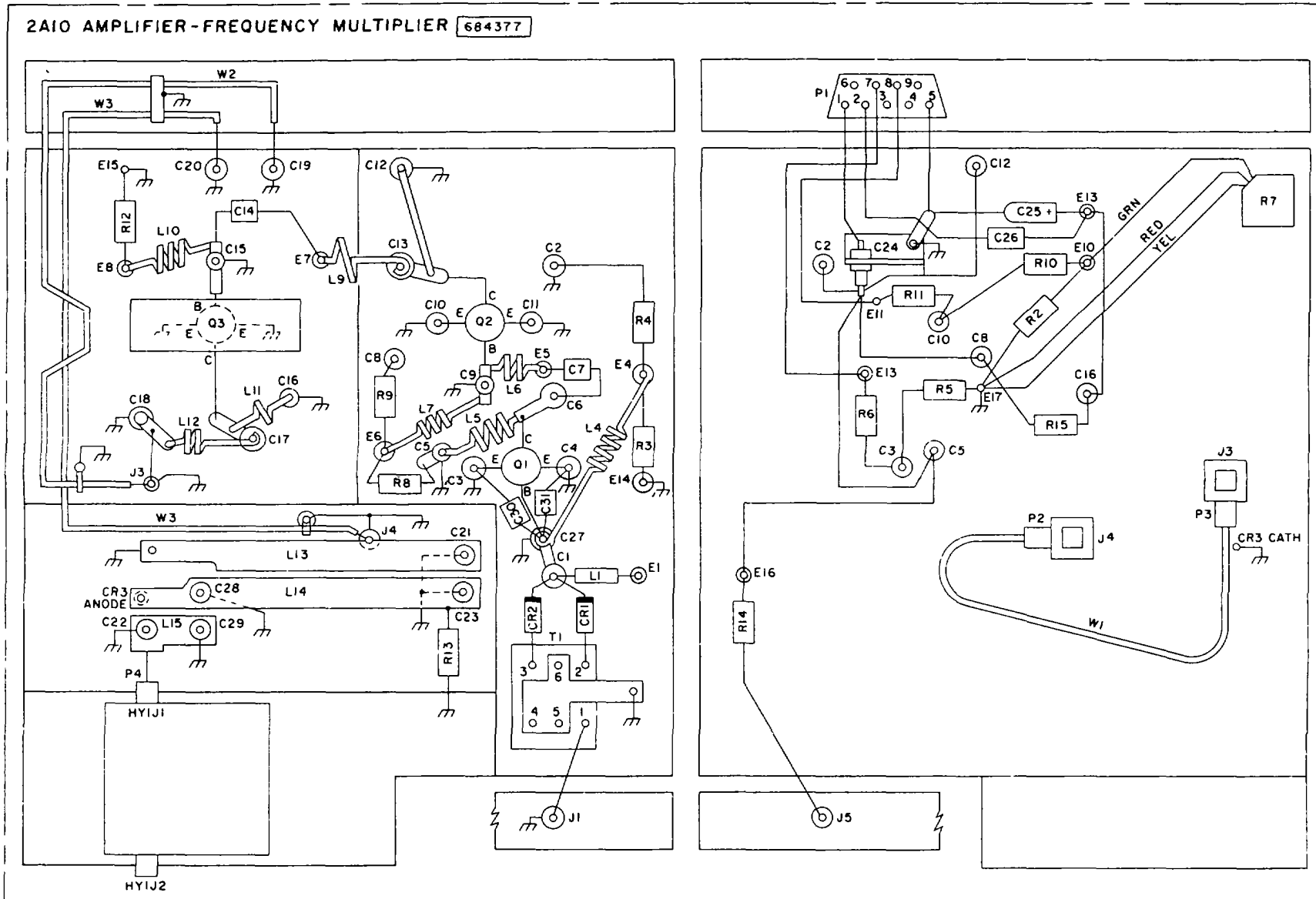


Figure 5-93. Amplifier-mixer 2A7, wiring diagram.  
5-203



NOTE

1 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH 2A10

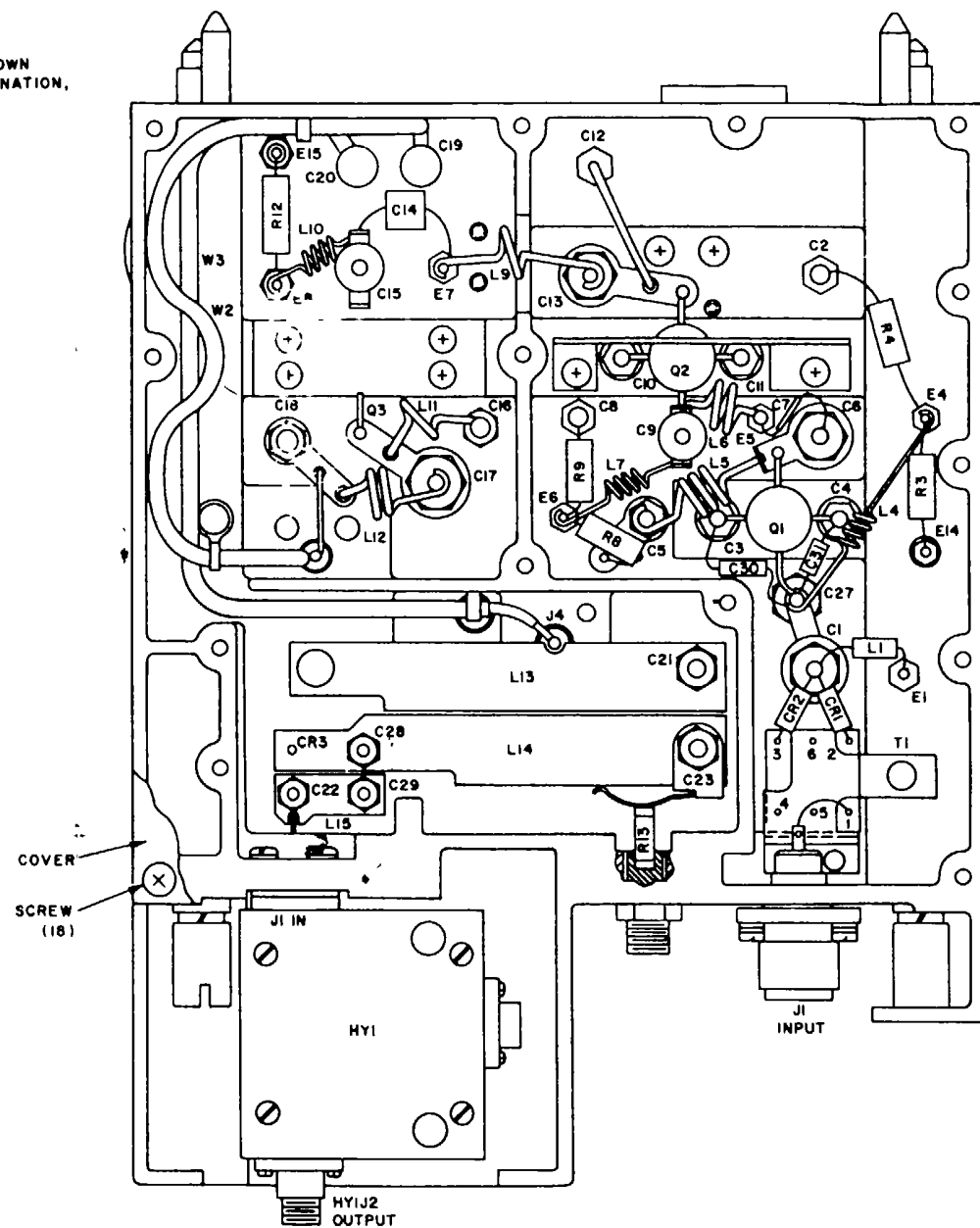
2 WIRING IS NO 22 AWG STRANDED WIRE, TEFLON INSULATED

EL5820-695-35-TM-C1-46

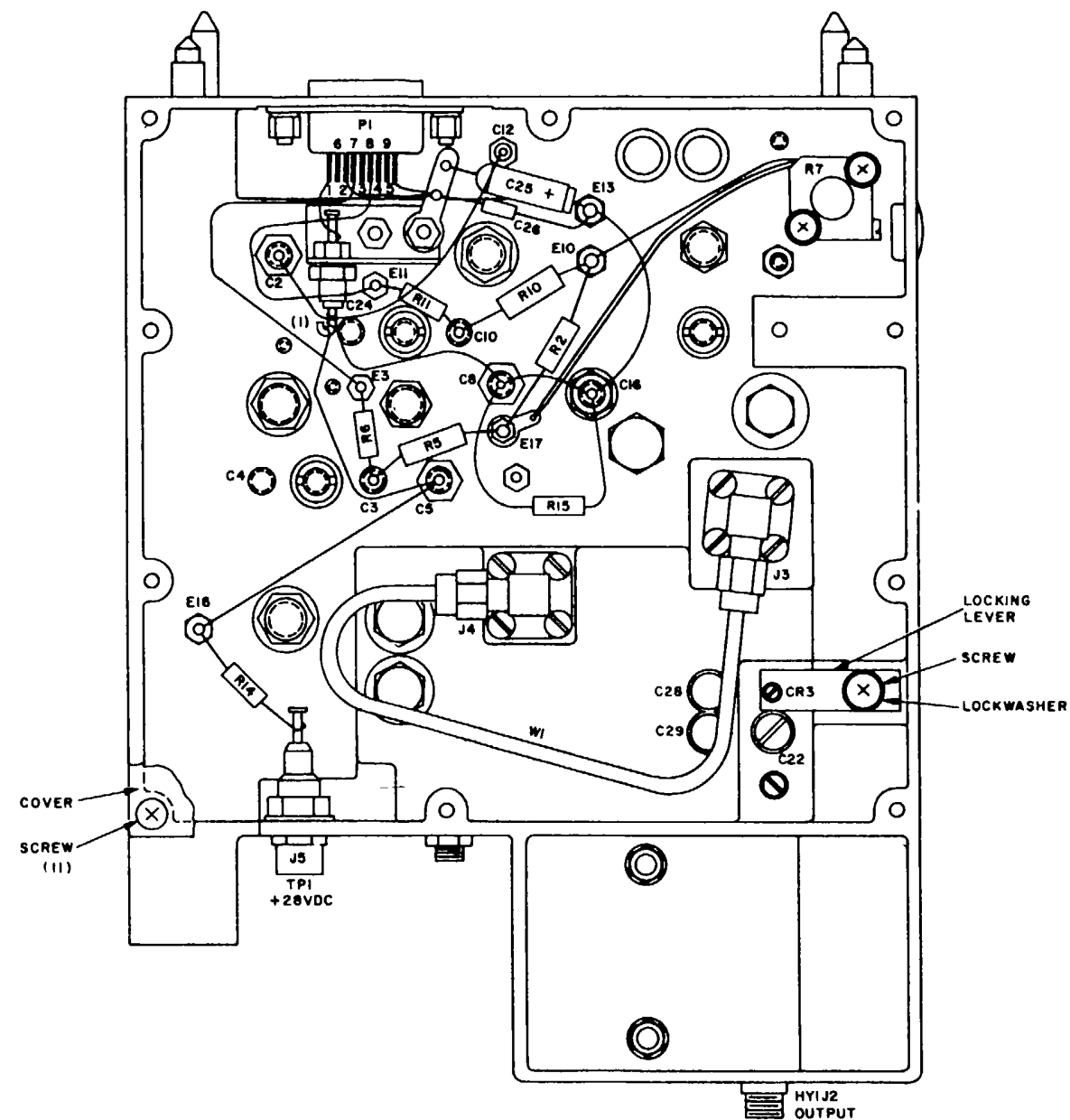
Figure 5-94. Amplifier-frequency multiplier 2A10, wiring diagram.  
Change 1 5-205

NOTE

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH 2A10



A TOP VIEW, COVER REMOVED.



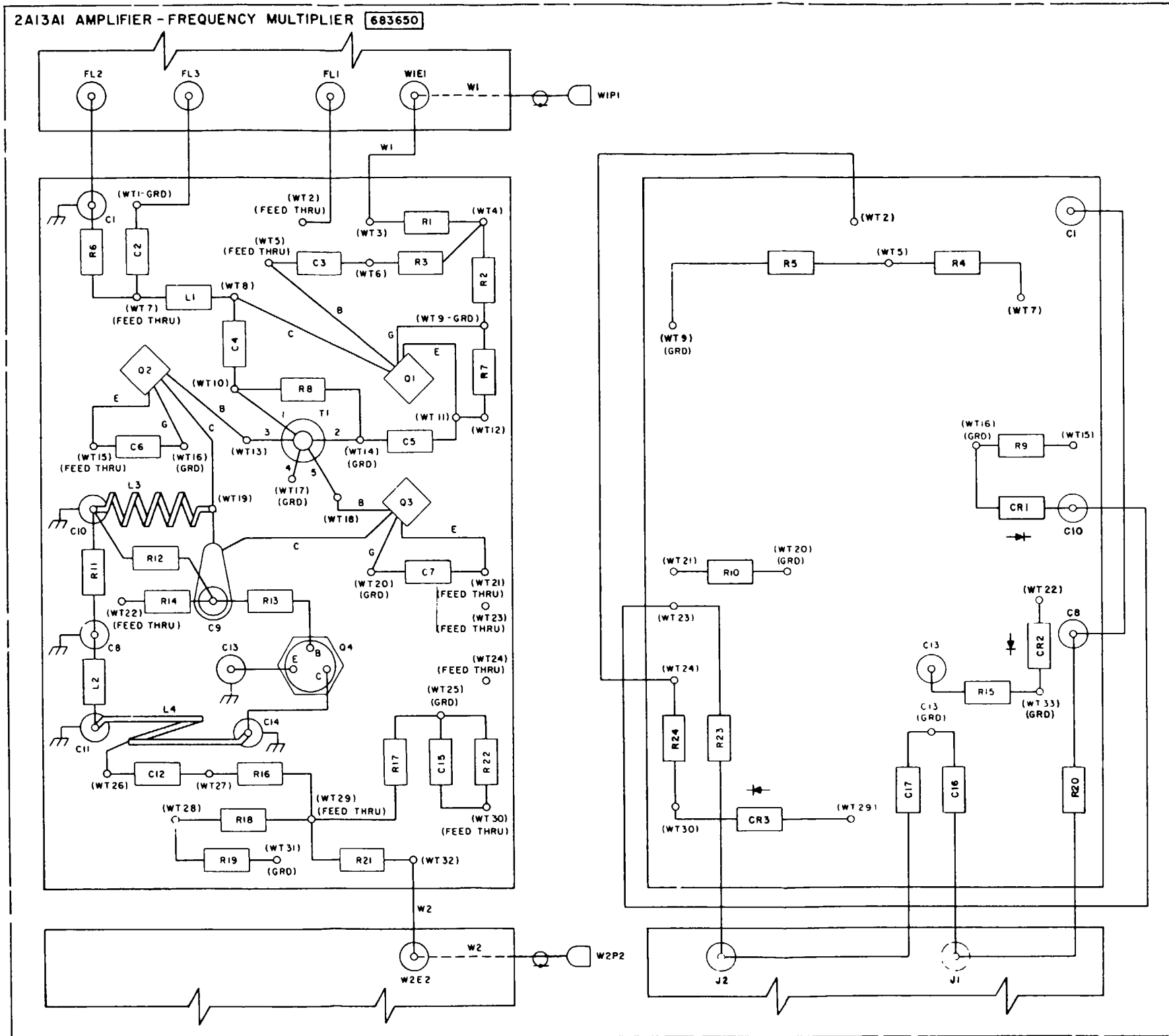
B BOTTOM VIEW, COVER REMOVED.

EL5820-695-35-TM-CI-47

Figure 5-95. Amplifier-frequency multiplexer 2A10, parts location.  
Change 1 5-207

NOTES

- 1 PARTIAL REFERENC DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH 2A13A1
- 2 ALL WIRE IS NO.22 AWG STRANDED TEFLON INSULATED.
- 3. WIRING TIEPOINTS (WT...) TERMINAL NUMBERS ARE ASSIGNED FOR IDENTIFICATION PURPOSES ONLY. THEY ARE NOT MARKED ON EQUIPMENT



EL5820-695-35-TM-232

Figure 5-96. Amplifier-frequency multiplier 2A13A, wiring diagram.  
5-209

NOTE  
 PARTIAL REFERENCE DESIGNATIONS  
 ARE SHOWN FOR COMPLETE  
 DESIGNATION PREFIX WITH 2A13  
 AND SUBASSEMBLY DESIGNATION

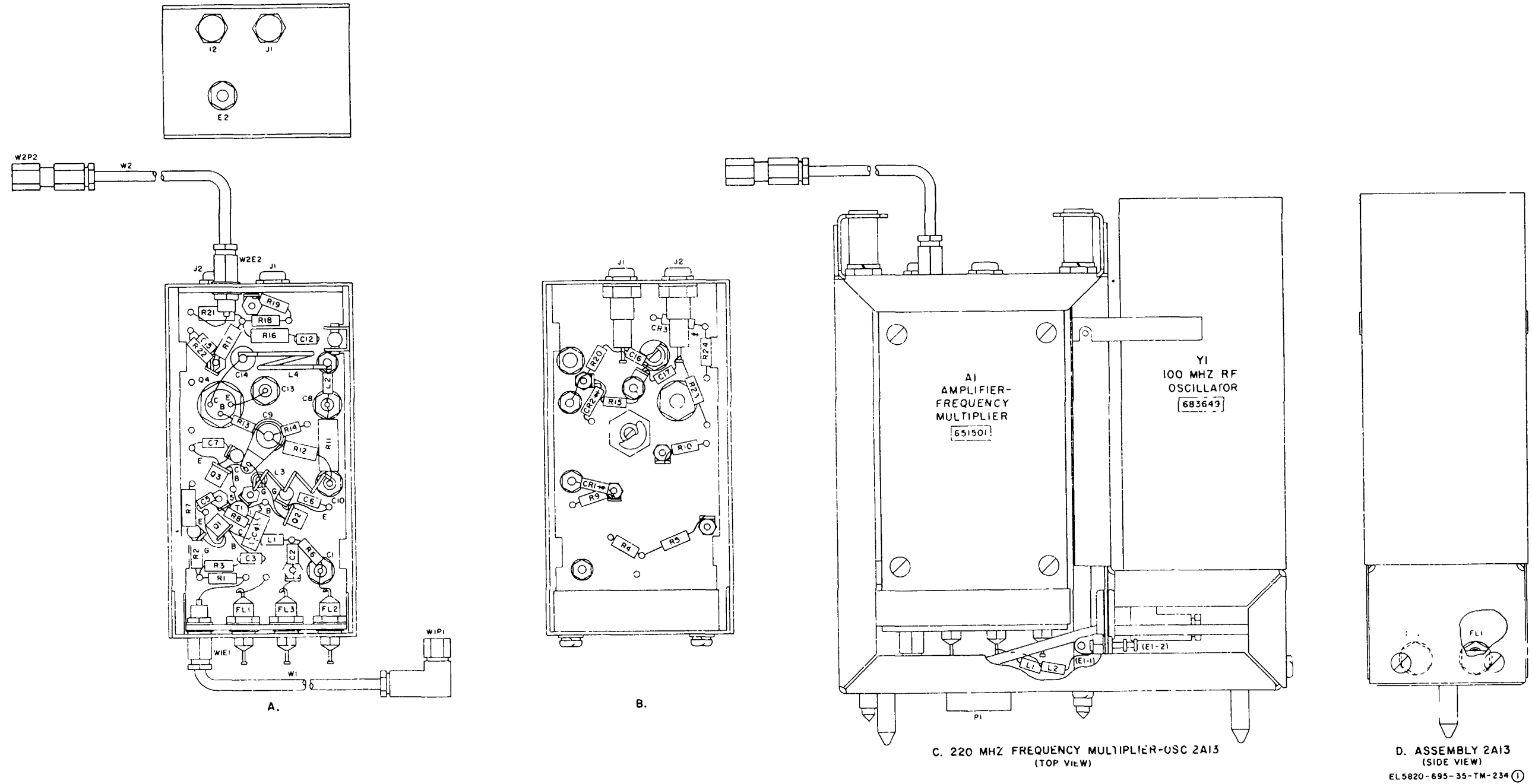
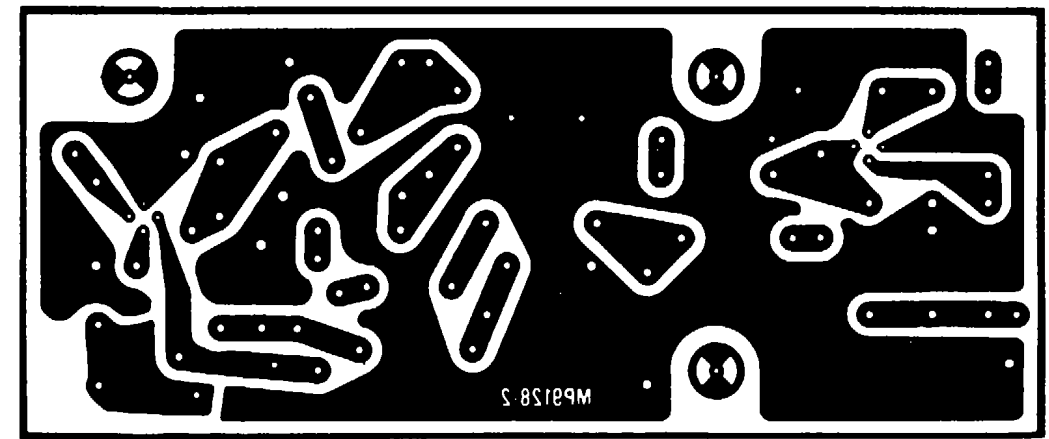
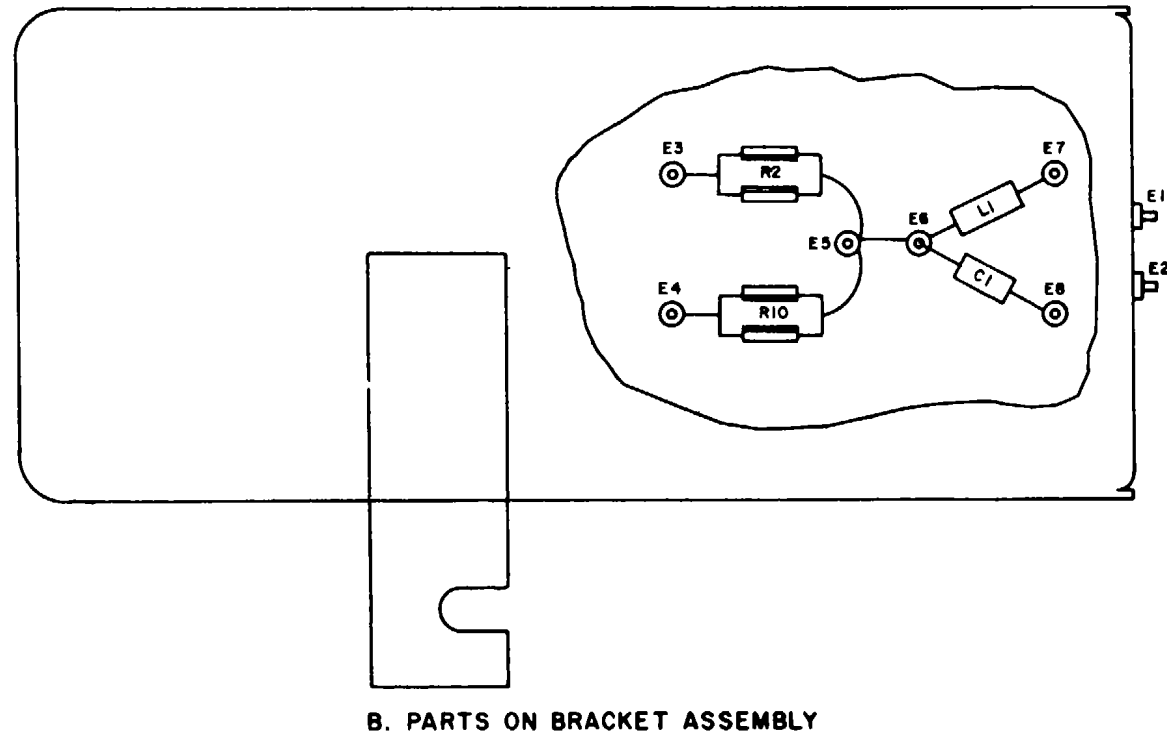
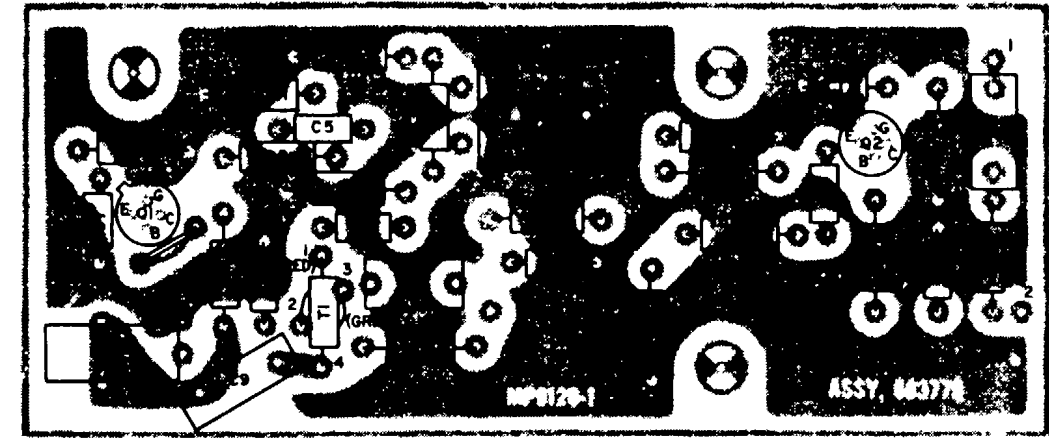
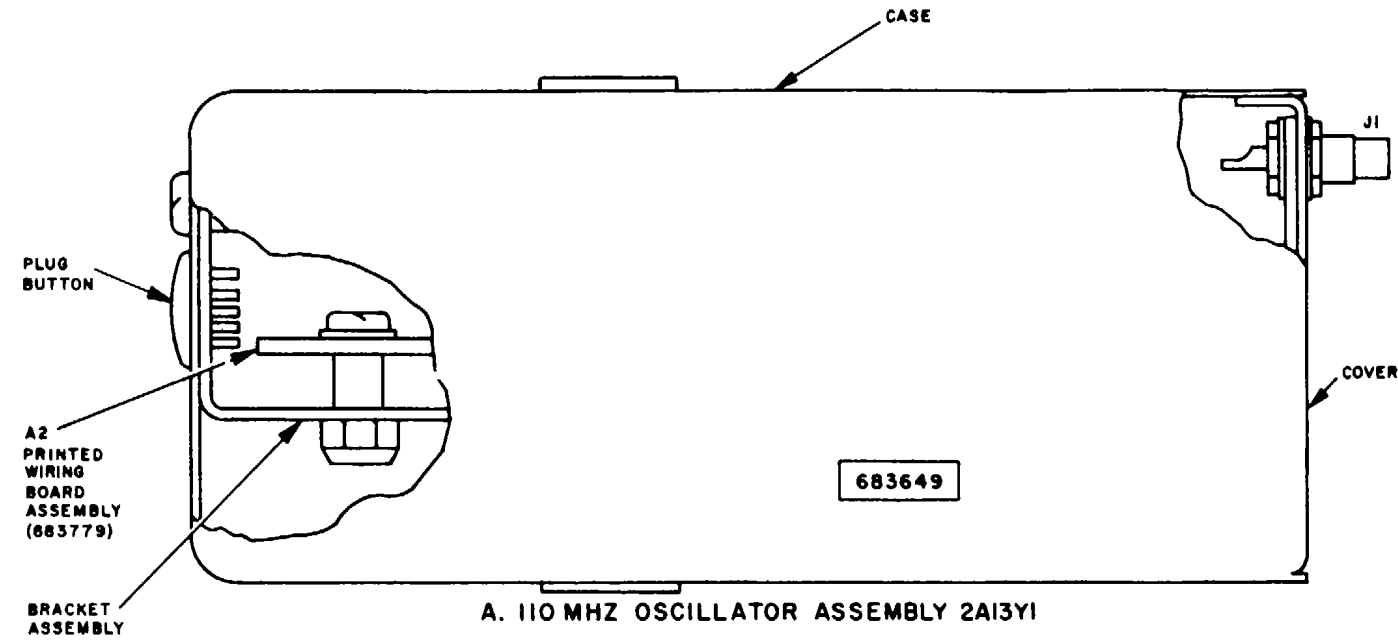


Figure 5-97(1). 220 MHz frequency multiplier-osc 2A13, parts location (part 1 of 2).  
 5-211



EL5820-695-35-TM-234 ②

Figure 5-97(2). 220 MHz frequency multiplier-osc 1A13, parts location (part 2 of 2).  
5-213

UNIT 3  
CONVERTER - MULTIPLIER  
CV-3633/GRC-144(V)

- NOTES
- 1 THERMOSTATIC SWITCH S1 NORMALLY CLOSED AT AMBIENT TEMPERATURE
  - 2 AIR FLOW SWITCH S2, NORMALLY CLOSED WHEN SYSTEM IS DE-ENERGIZED
  - 3 FOR STATUS PANEL 3AB SCHEMATIC DIAGRAM REFER TO FIGURE 5-106
  - 4 PARTIAL REFERENCE DESIGNATIONS PREFIX WITH UNIT NUMBER
  - 5 CONNECTOR J2 PHYSICAL ORIENTATION WITH RESPECT TO ELECTRICAL EQUIPMENT CHASSIS
  - 6 UNLESS OTHERWISE SPECIFIED ALL WIRE SHALL BE STRANDED, TEFLON INSULATED, SIZES AS FOLLOWS  
NO 16 AWG - FOR 115V AC POWER  
NO 20 AWG - FOR LOW VOLTAGE AC AND DC AND GROUND  
NO 22 AWG - FOR ALL OTHER WIRING
  - 7 CONTACT ARRANGEMENTS FOR VARIOUS CONNECTORS ARE SHOWN IN TABLE 1
  - 8 THE SYMBOL ← P DENOTES TWISTED PAIR

TABLE 1 CONNECTOR PIN ARRANGEMENTS (MATING SIDE VIEW)

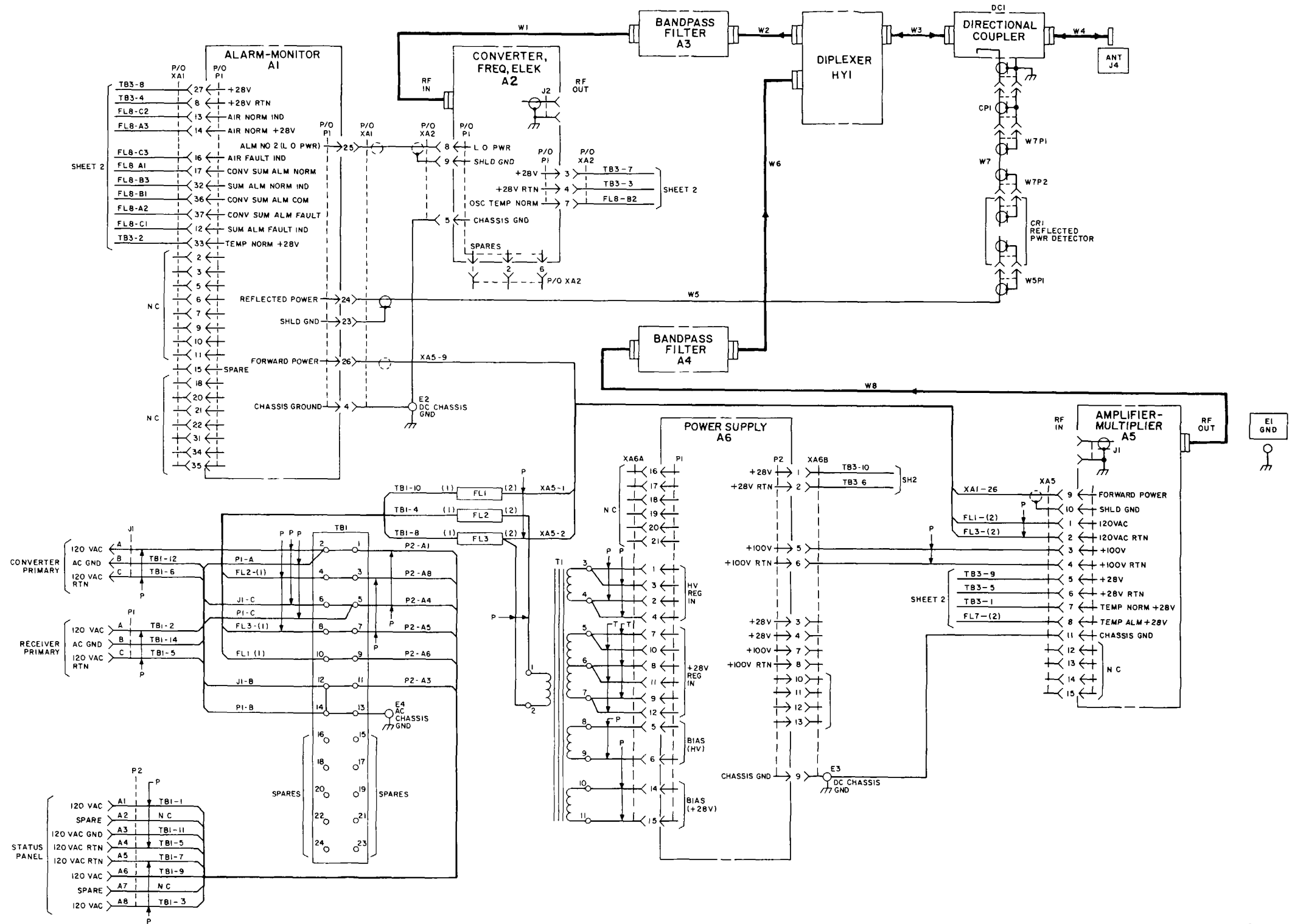
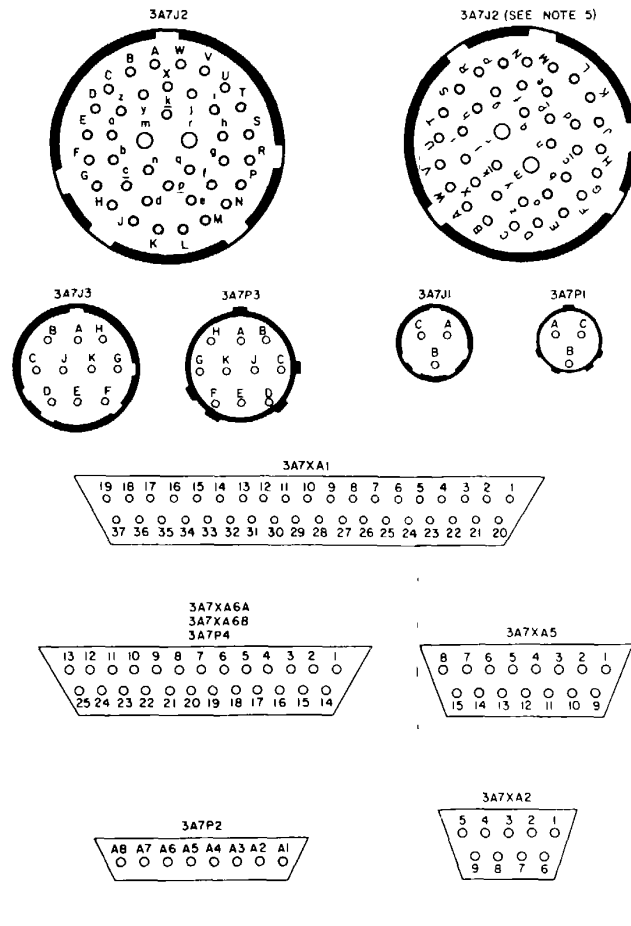


Figure 5-98 (1). Converter multiplier CV-3633/GRC-144(V), unit 3, interconnecting diagram (sheet 1 of 2).

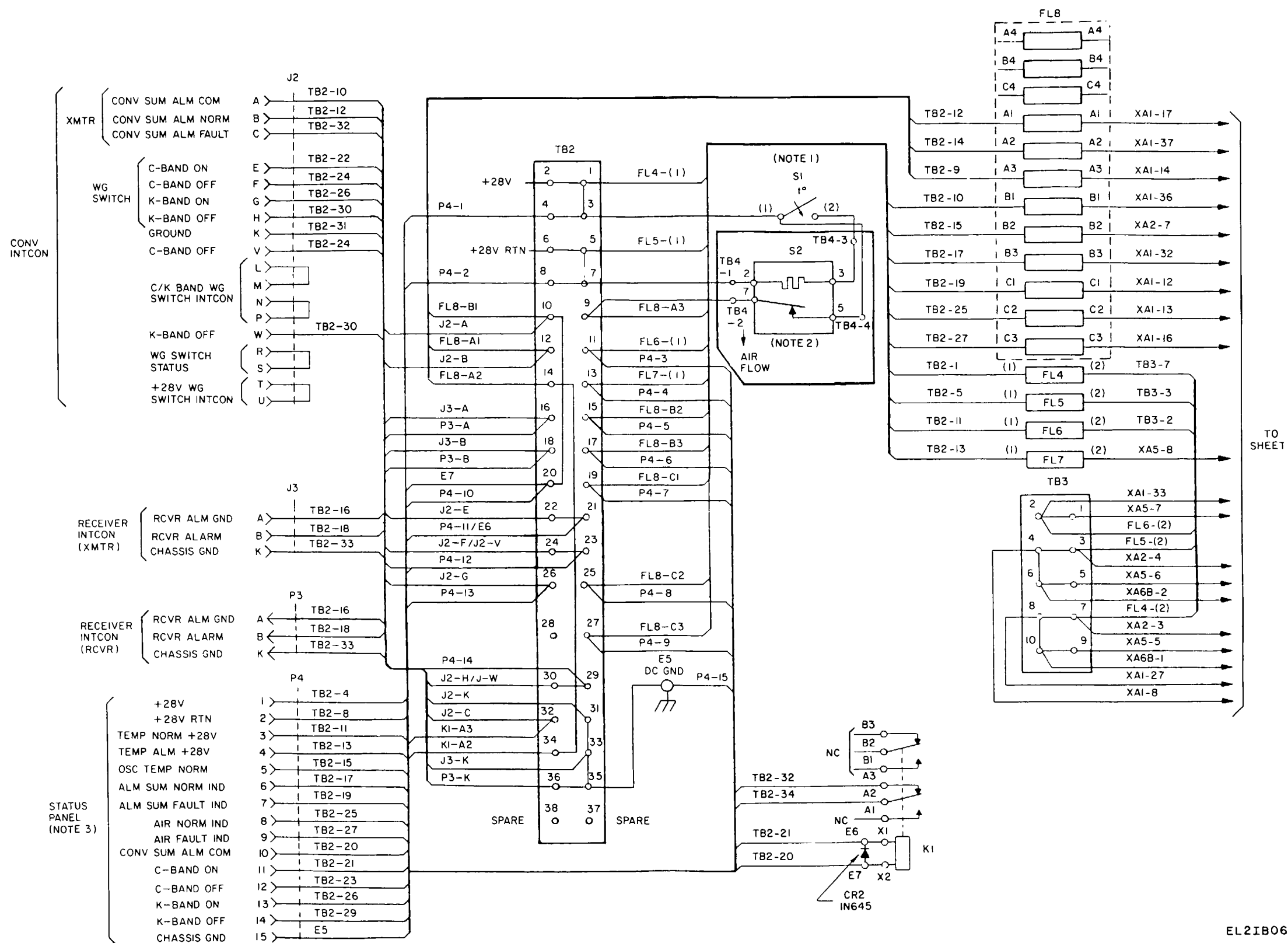


Figure 5-98 (2). Converter multiplier CV-3633/GRC-144(V), unit 3, interconnecting diagram (sheet 2 of 2).



- NOTE
- 1 UNLESS OTHERWISE SPECIFIED CAPACITORS ARE IN MICROFARADS, INDUCTORS ARE IN MICROHENRIES, RESISTORS ARE IN OHMS AND ARE 1/4 WATT, 5 PERCENT
  - 2 PARTIAL REFERENCE DESIGNATION ARE SHOWN FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION
  - 3 XXXX INDICATES MARKING ON EQUIPMENT

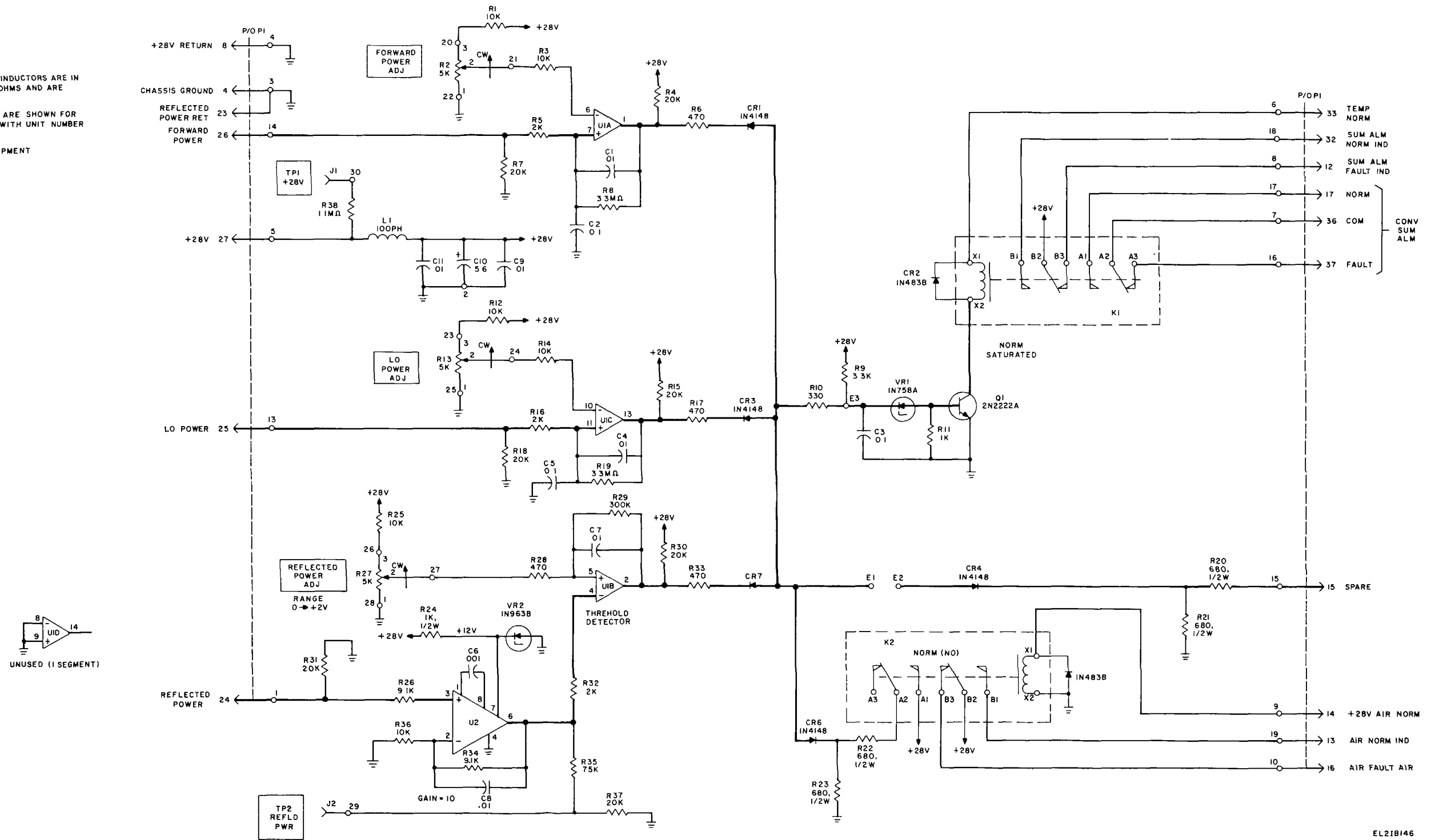


Figure 5-99. Alarm Monitor 3A1, schematic diagram.

Change 6 5-219

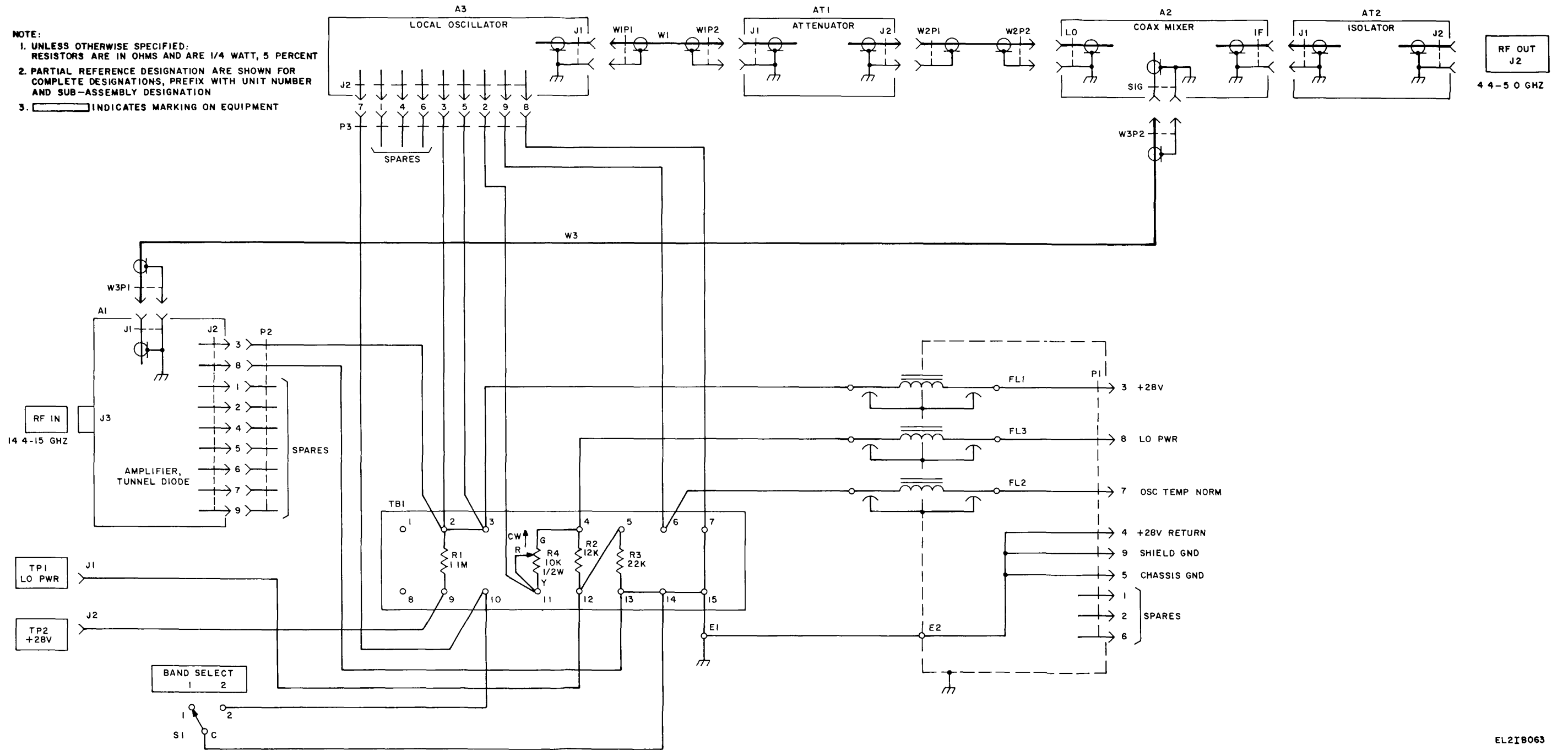
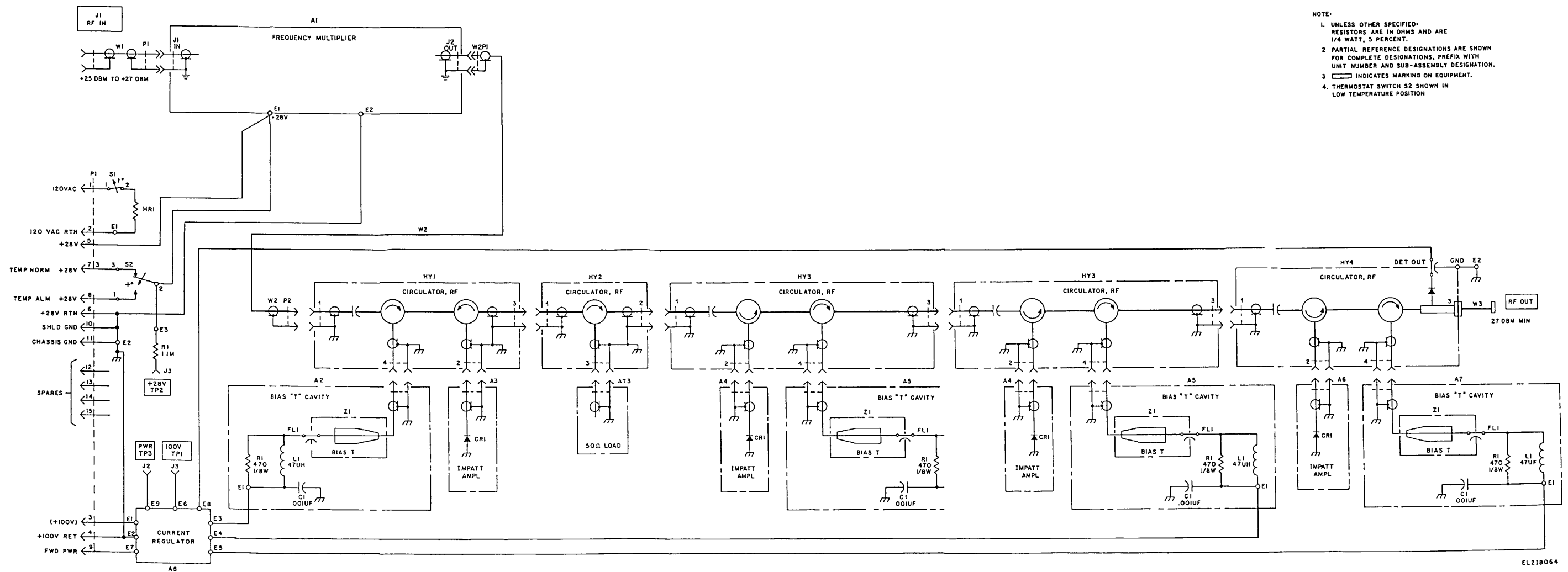


Figure 5-100. Converter, frequency electronic 3A2, schematic diagram.

Change 6 5-221



- NOTE:
1. UNLESS OTHER SPECIFIED, RESISTORS ARE IN OHMS AND ARE 1/4 WATT, 5 PERCENT.
  2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.
  3.   INDICATES MARKING ON EQUIPMENT.
  4. THERMOSTAT SWITCH S2 SHOWN IN LOW TEMPERATURE POSITION

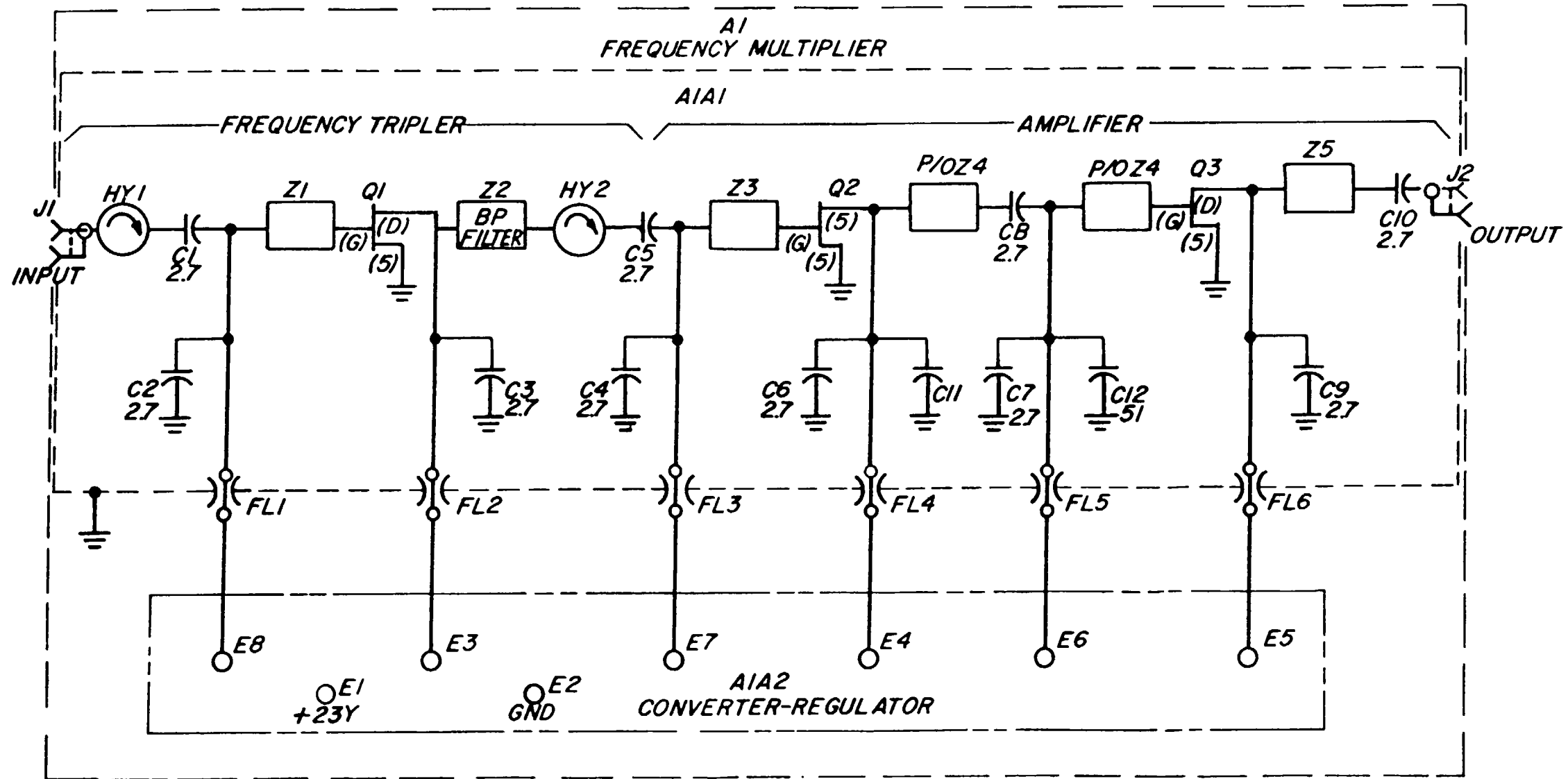
Figure 5-101. Amplifier multiplier 3A5, schematic diagram (sheet 2 of 2).

Change 6 5-223

EL218064

NOTE:

1. UNLESS OTHER SPECIFIED, RESISTORS ARE IN OHMS AND ARE 1/4 WATT, 5 PERCENT.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.
3. NUMBERS IN PARENTHESIS ARE NOT MARKED ON COMPONENT



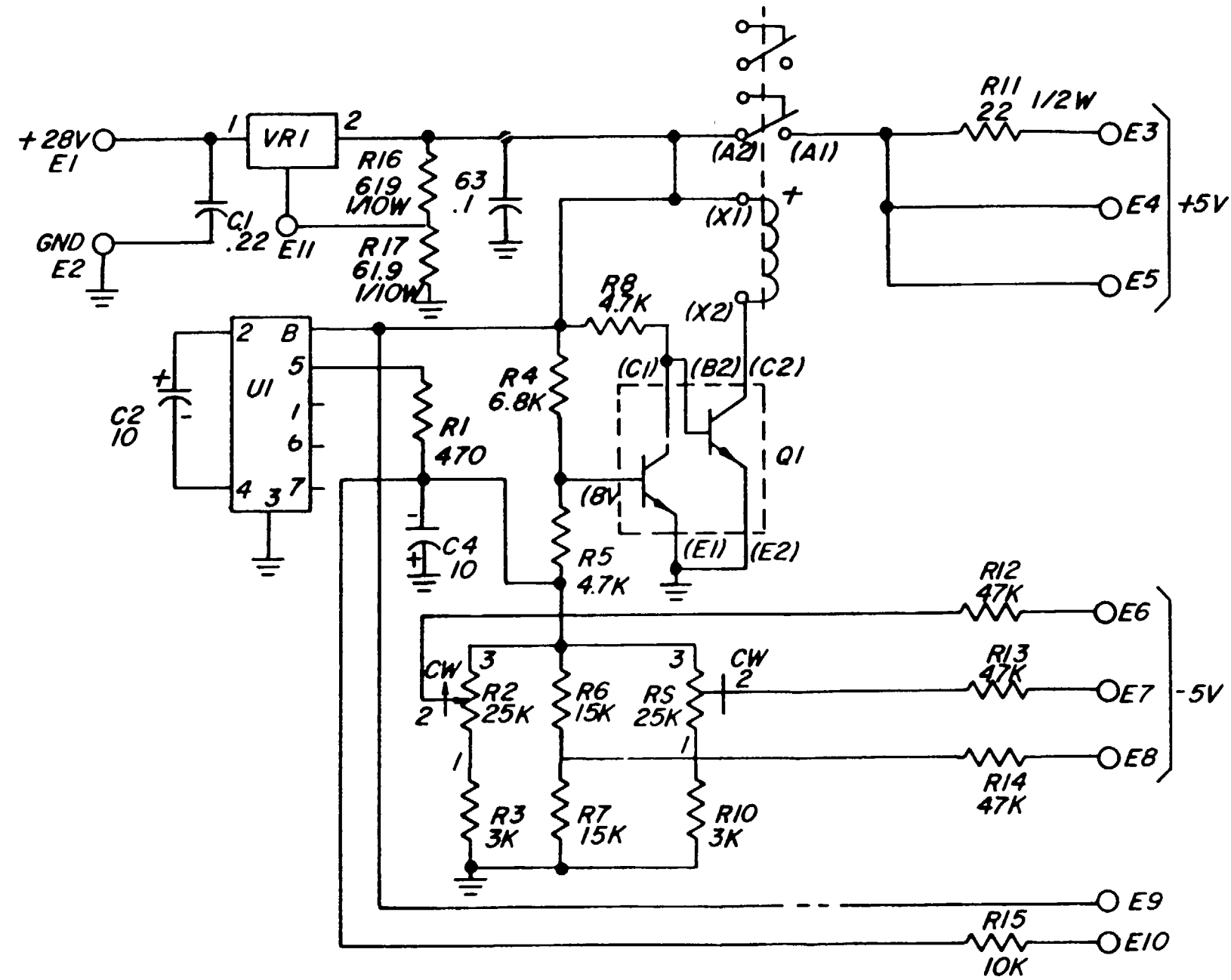
EL2IB151

Figure 5-101.1. Frequency multiplier 3A5A1, schematic diagram.

Change 6 5-223.1

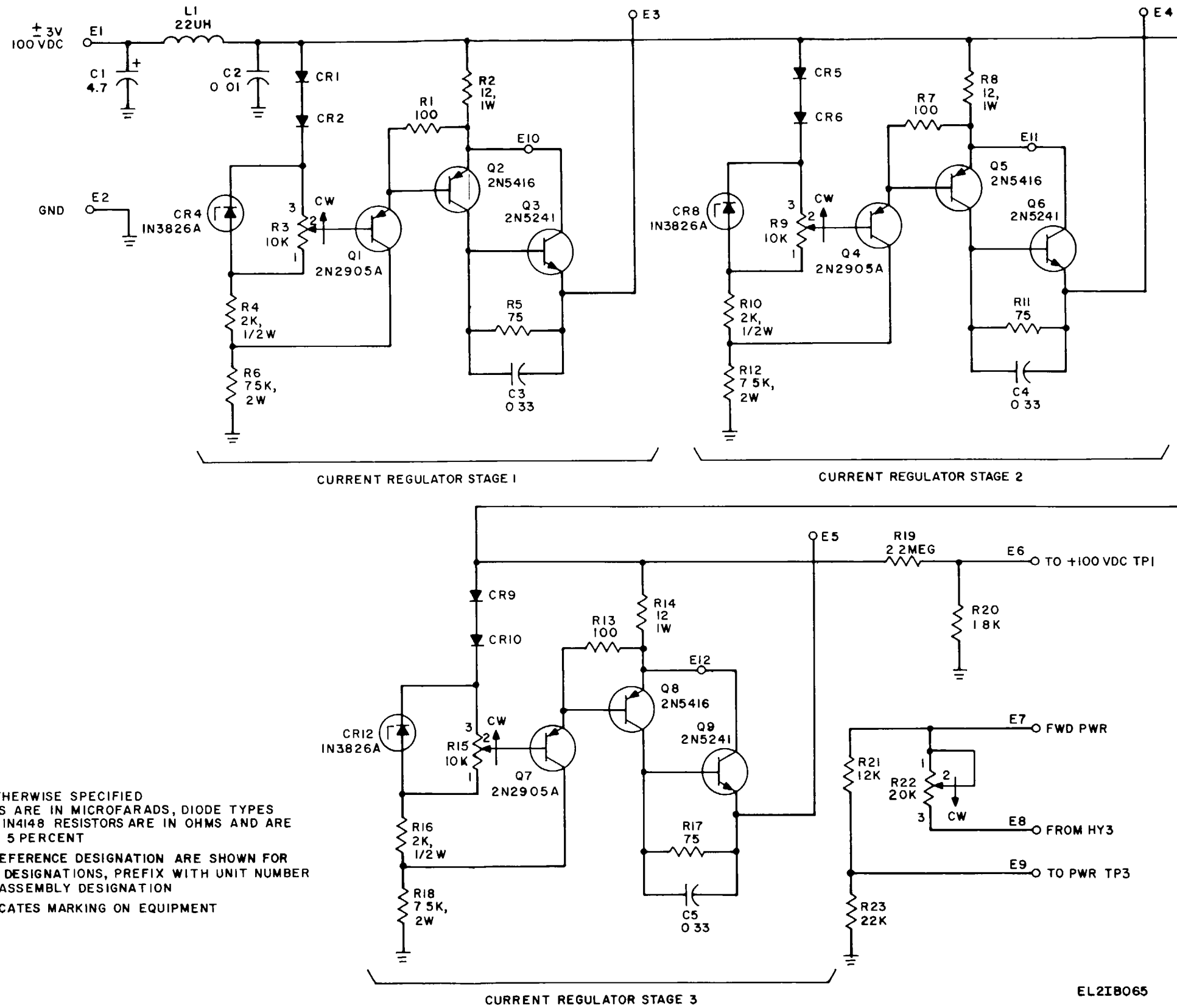
NOTE:

1. UNLESS OTHER SPECIFIED, RESISTORS ARE IN OHMS AND ARE 1/4 WATT, 5 PERCENT.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION
3. NUMBERS IN PARENTHESIS ARE NOT MARKED ON COMPONENT



EL2IB152

Figure 5-101.2. Converter-regulator 3A5A1A2, schematic diagram.



- NOTE:
- 1 UNLESS OTHERWISE SPECIFIED CAPACITORS ARE IN MICROFARADS, DIODE TYPES ARE IN4148 RESISTORS ARE IN OHMS AND ARE 1/4 WATT, 5 PERCENT
  - 2 PARTIAL REFERENCE DESIGNATION ARE SHOWN FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION
  - 3  INDICATES MARKING ON EQUIPMENT

Figure 5-102. Current regulator 3A5A8, schematic diagram.

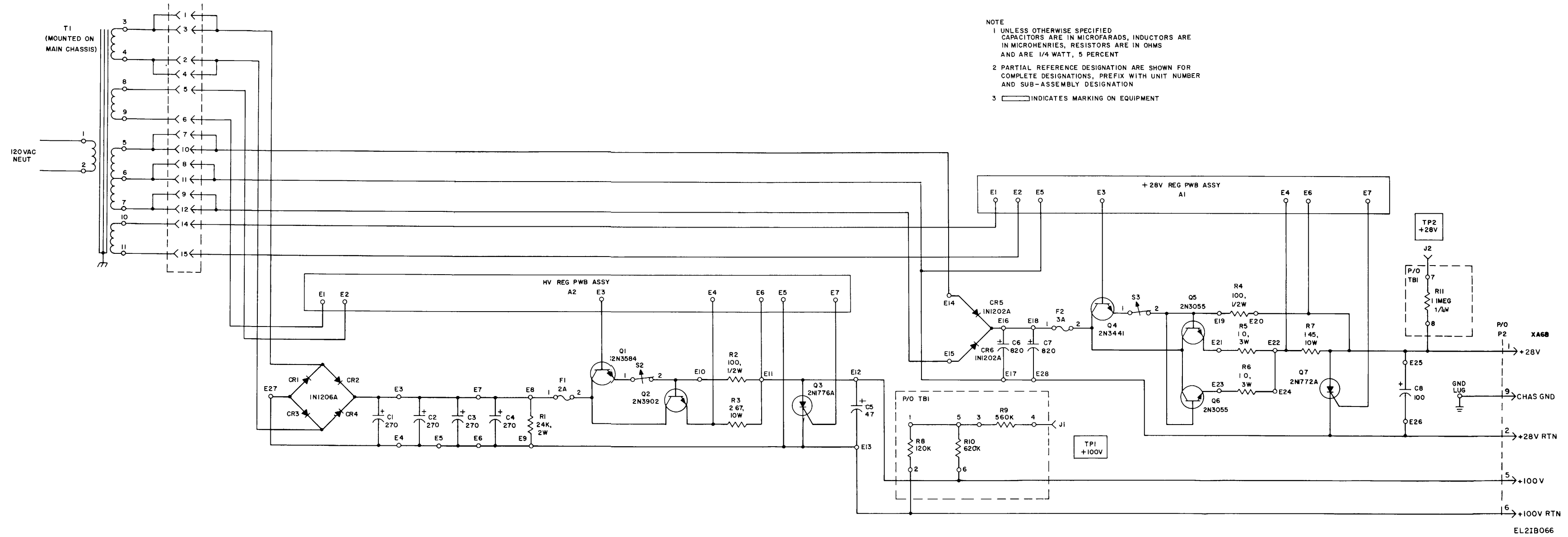


Figure 5-103. Power supply 3A6, schematic diagram.

Change 6 5-227

- NOTE:
1. UNLESS OTHERWISE SPECIFIED:  
CAPACITORS ARE IN MICROFARADS, INDUCTORS ARE IN MICROHENRIES, RESISTORS ARE IN OHMS AND ARE 1/4 WATT, 5 PERCENT.
  2. PRECISION VOLTAGE REGULATOR M38510/10201BCB.

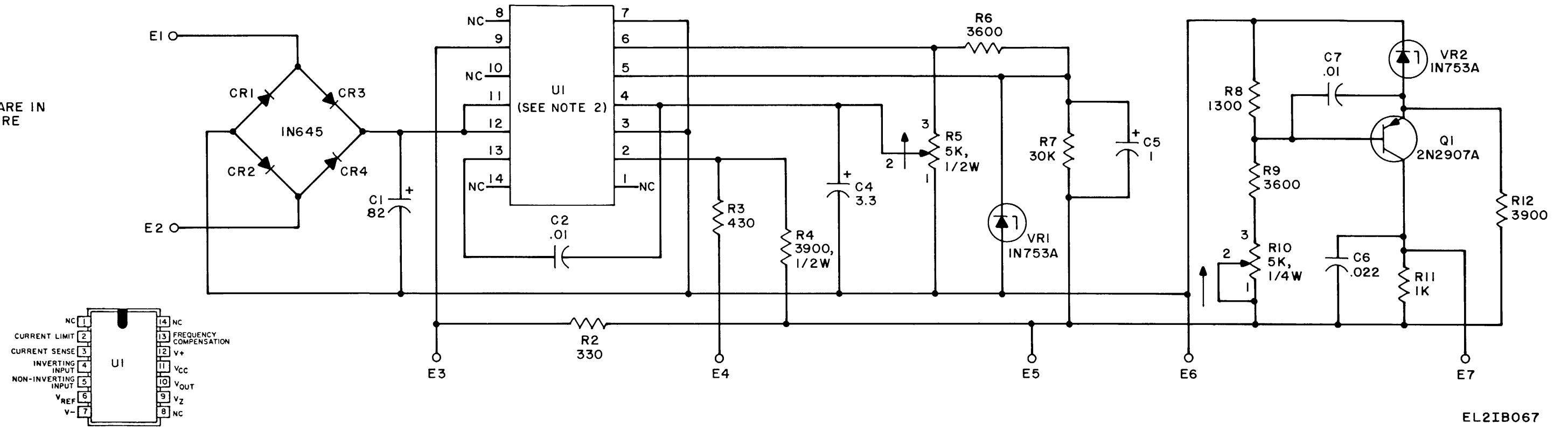
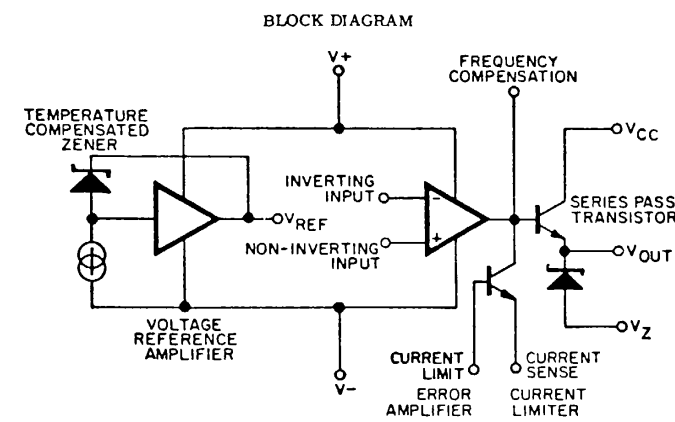


Figure 5-104. Voltage regulator (28 VDC) 3A6A1, schematic diagram.

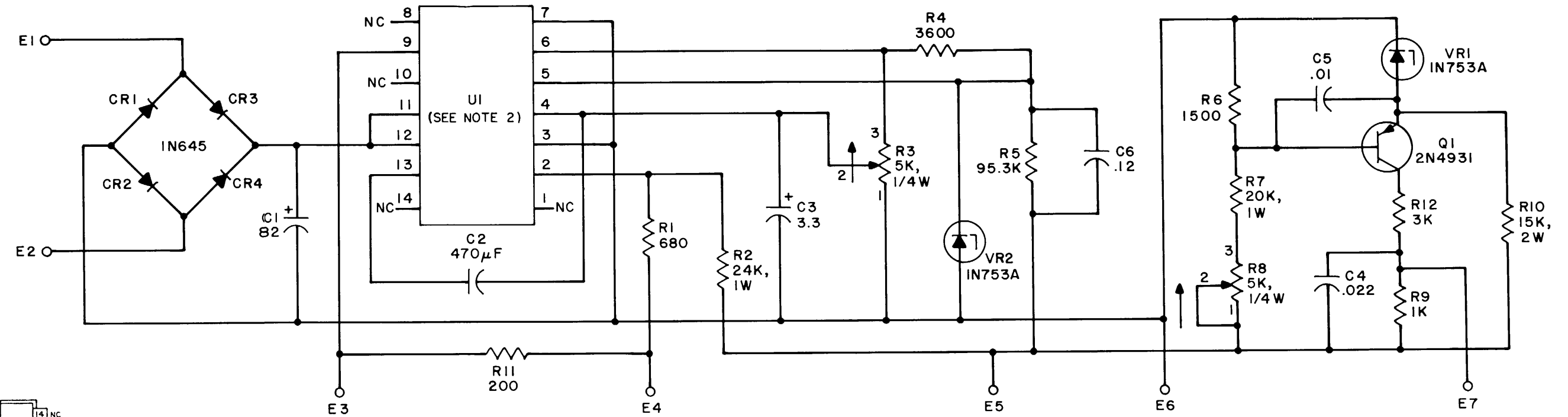
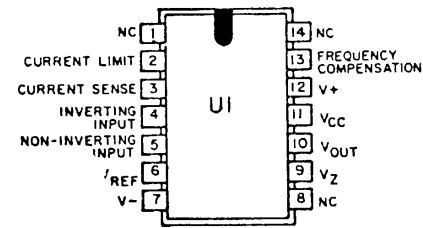
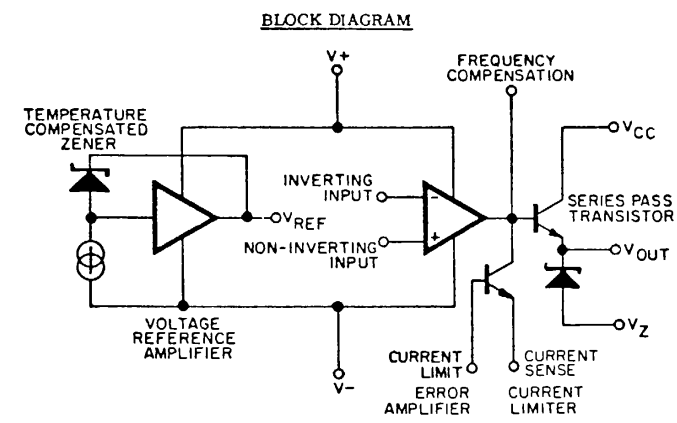
Change 6 5-229

EL2IB067



NOTE:

1. UNLESS OTHERWISE SPECIFIED: CAPACITORS ARE IN MICROFARADS, INDUCTORS ARE IN MICROHENRIES, RESISTORS ARE IN OHMS AND ARE 1/4 WATT, 5 PERCENT.
2. PRECISION VOLTAGE REGULATOR M38510/10201BCB.



EL2IB068

Figure 5-105. Voltage regulator (100 VDC) 3A6A2, schematic diagram.

Change 6 5-231

NOTES

- 1 PARTIAL REFERENCE DESIGNS ARE SHOWN FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATIONS
- 2 [ ] INDICATES MARKING ON EQUIPMENT
- 3 CONTROL, INDICATOR, SWITCH AND JACK OUTLINES SHOWING TERMINAL LOCATION ARE PROVIDED BELOW ALL VIEWS ARE FROM THE WIRING SIDE

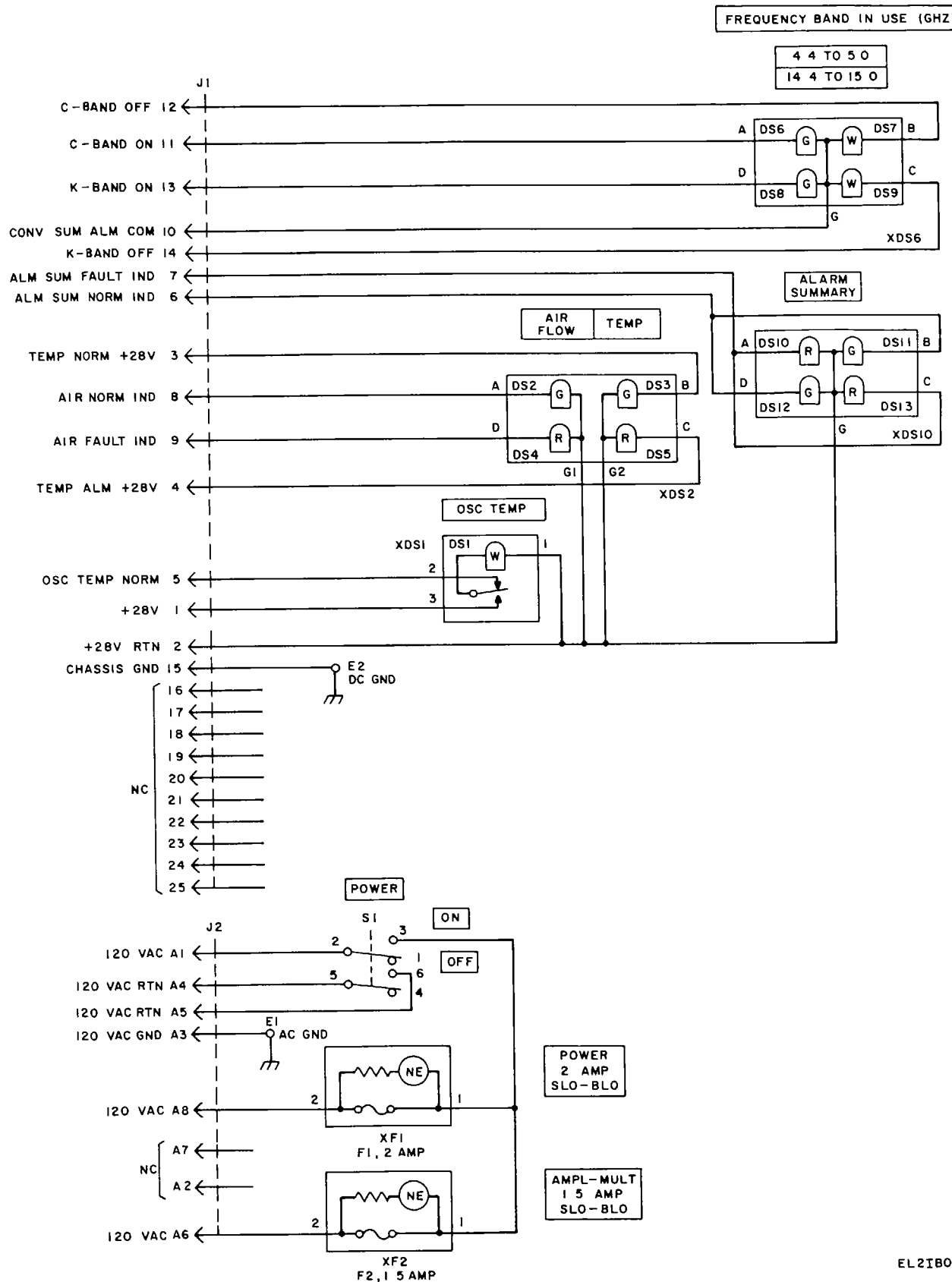
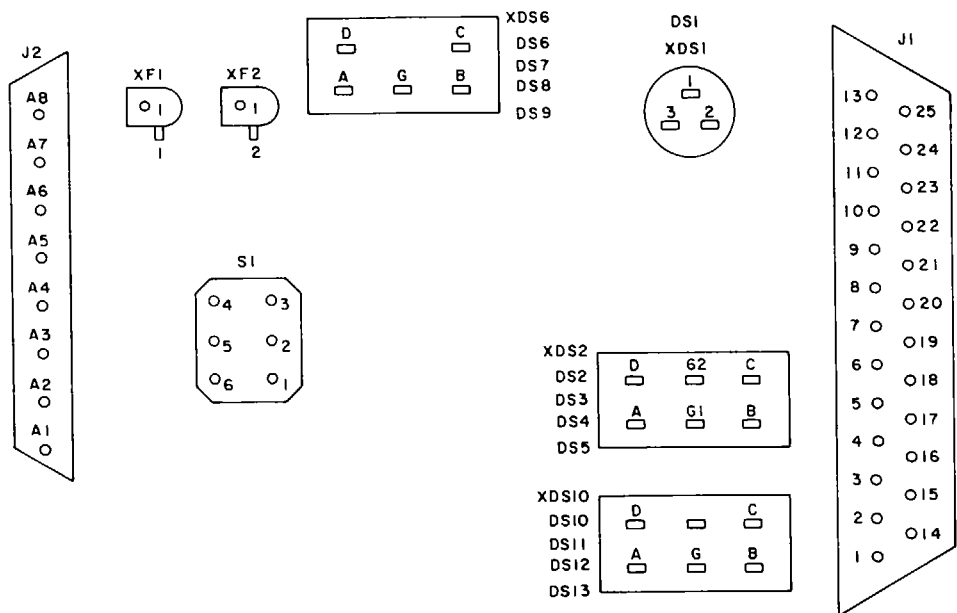


Figure 5-106. Status panel 3A8, schematic diagram.

NOTES:

1. FOR MODULE PARTS LOCATION REFER TO THE FOLLOWING FIGURES:

- A1 ALARM MONITOR (SEE FIGURE 5-108)
- A2 CONVERTER FREQUENCY ELECTRONICS (SEE FIGURE 5-109)
- A3 BP FILTER (RECEIVE)
- A4 BP FILTER (TRANSMIT)
- A5 AMPLIFIER MULTIPLIER (SEE FIGURE 5-110)
- A6 POWER SUPPLY (SEE FIGURE 5-115)
- A7 ELECTRICAL EQUIPMENT CHASSIS (SEE SHEETS 3 AND 4)
- A8 STATUS PANEL (SEE FIGURE 5-118)

2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH THE NUMBER 3.

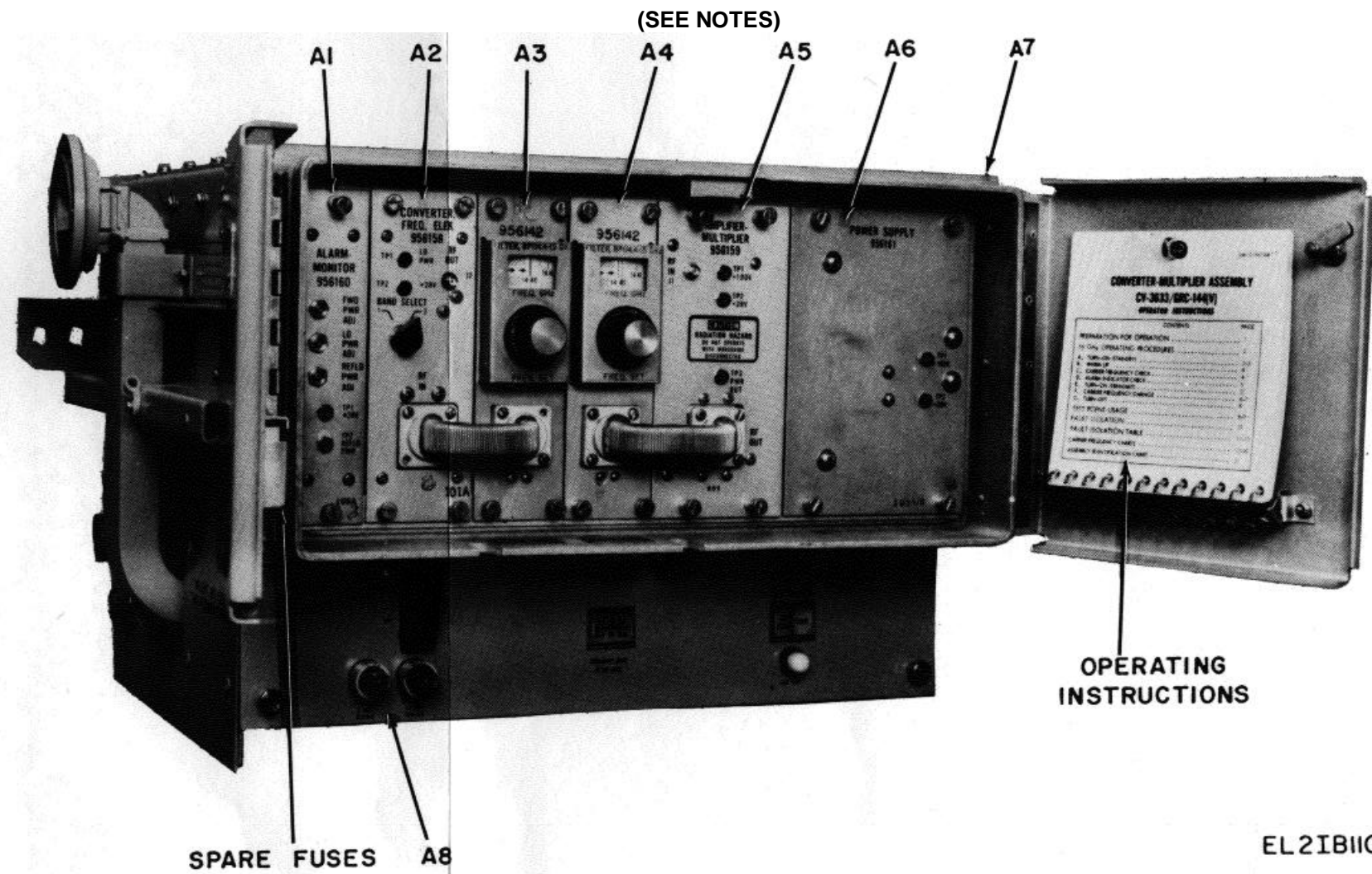


Figure 5-107 (1). Converter-multiplier assembly CV-3633/GRC-144 (V), parts location (sheet 1 of 4).

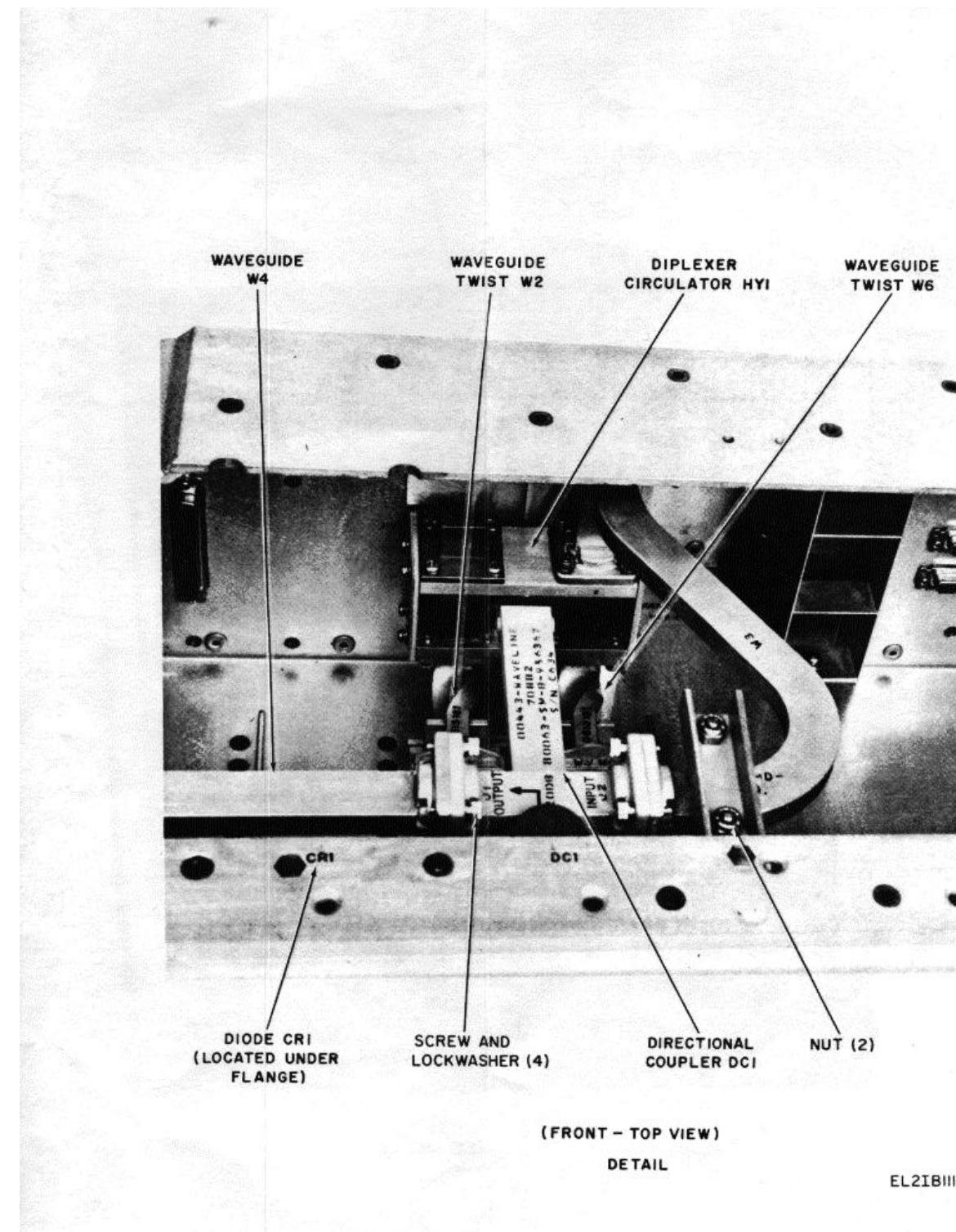
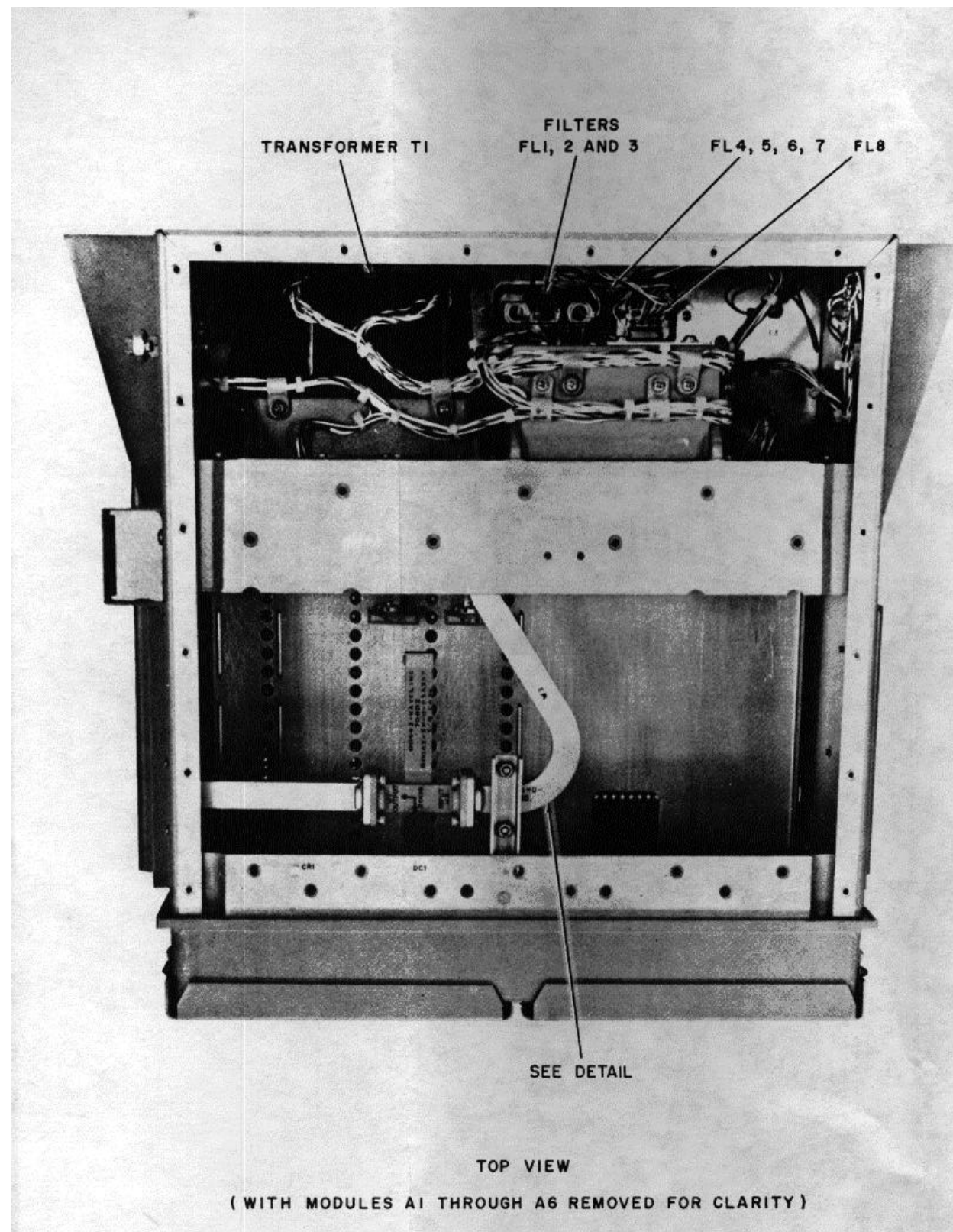


Figure 5-107 (2). Converter-multiplier assembly CV-3633/GRC-144 (V), parts location (Sheet 2 of 4).



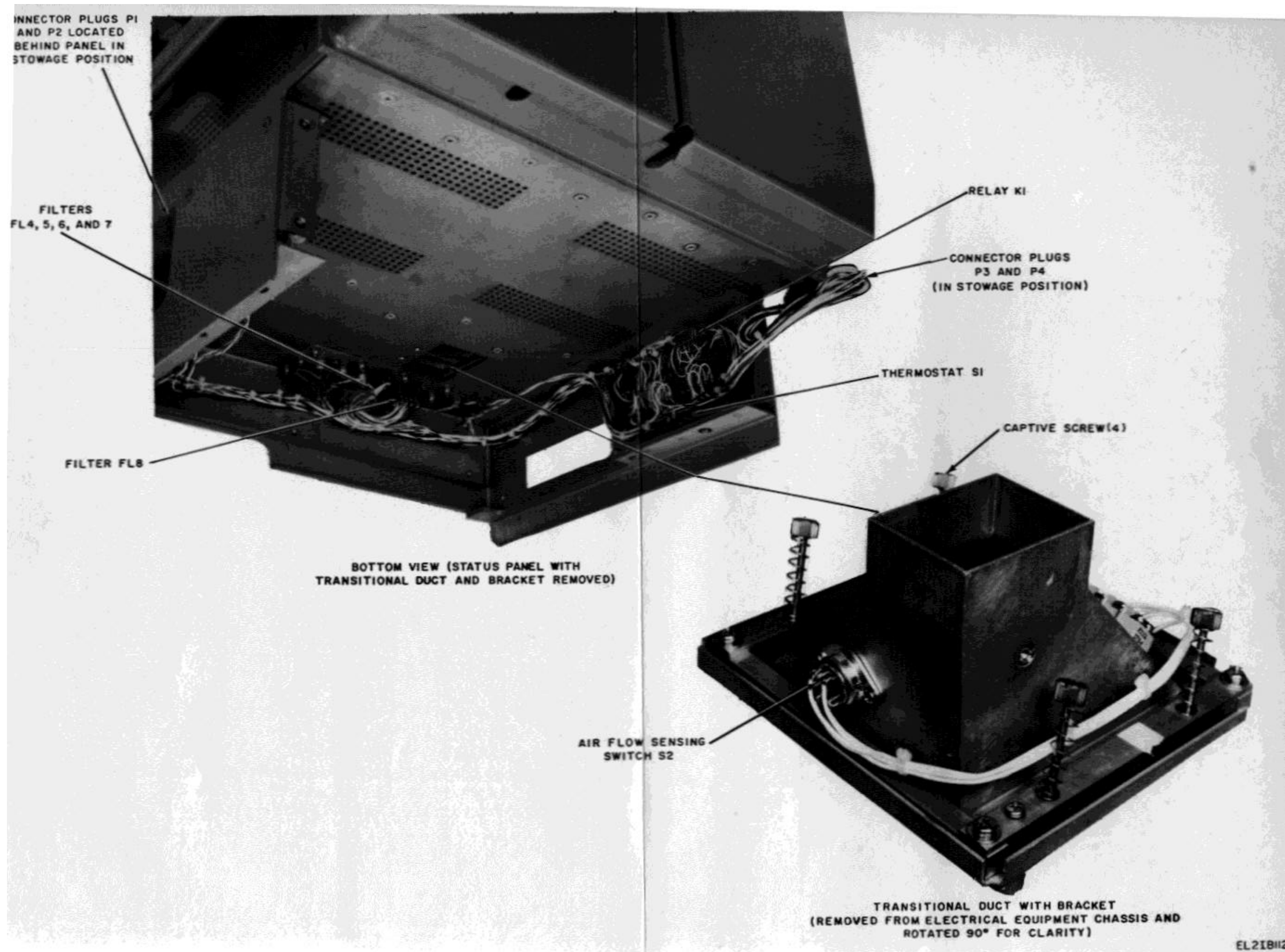
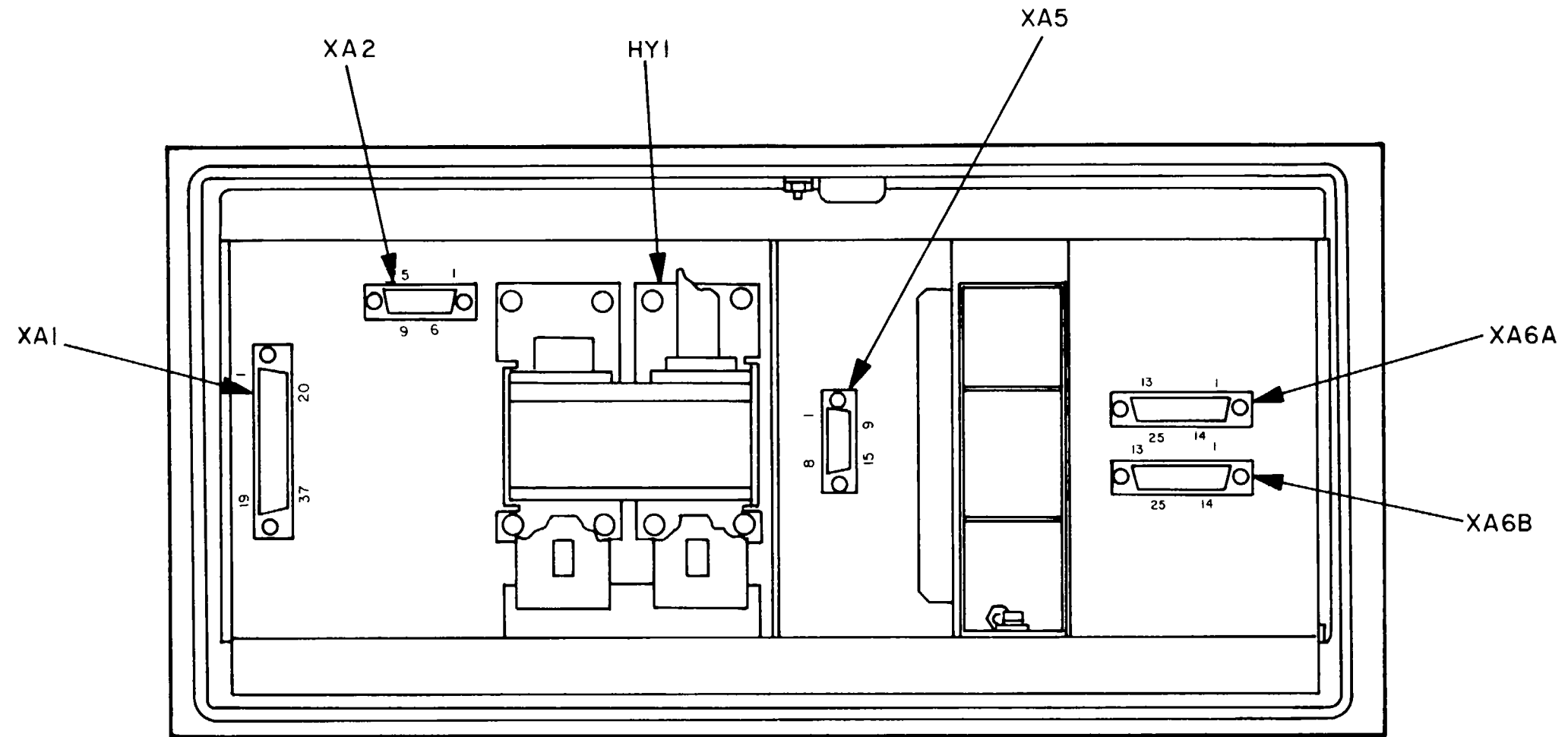


Figure 5-107 (3). Converter-multiplier assembly CV-3633/GRC-144 (V), parts location (Sheet 3 of 4).



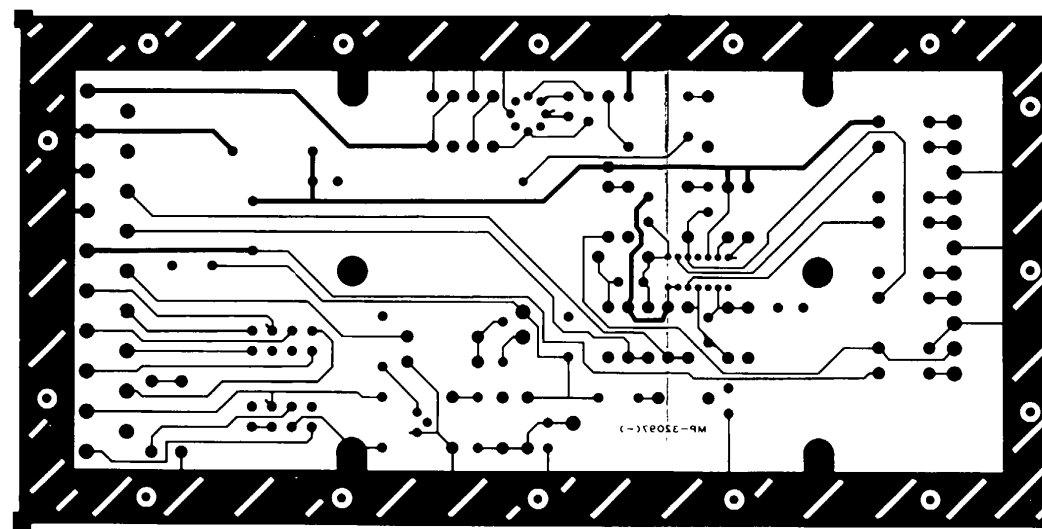
EL2IB070

Figure 5-107 (4). Converter-multiplier assembly CV-3633/GRC-144 (V), parts location (Sheet 4 of 4).

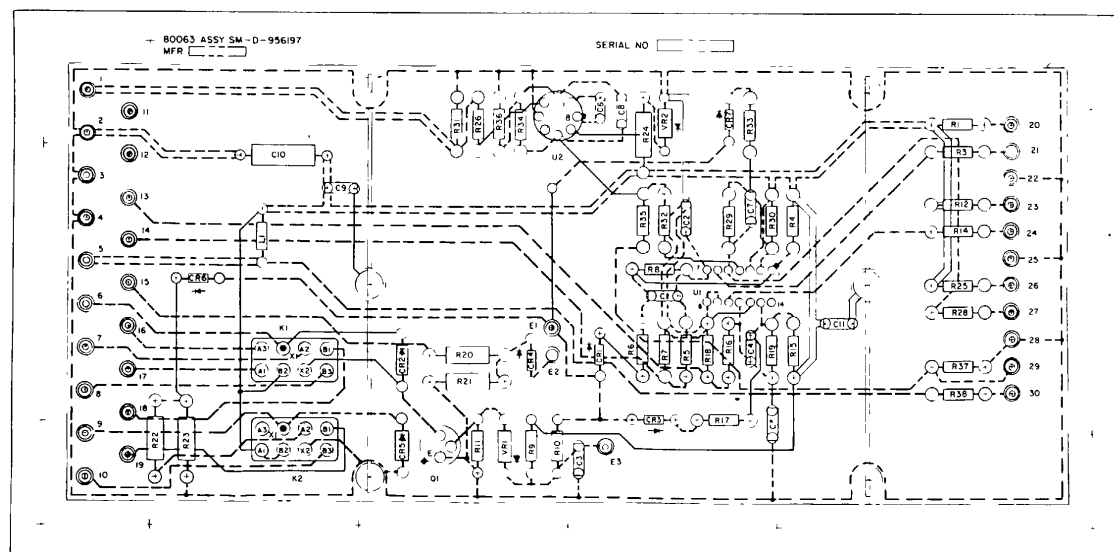
Change 6 5-241

NOTES

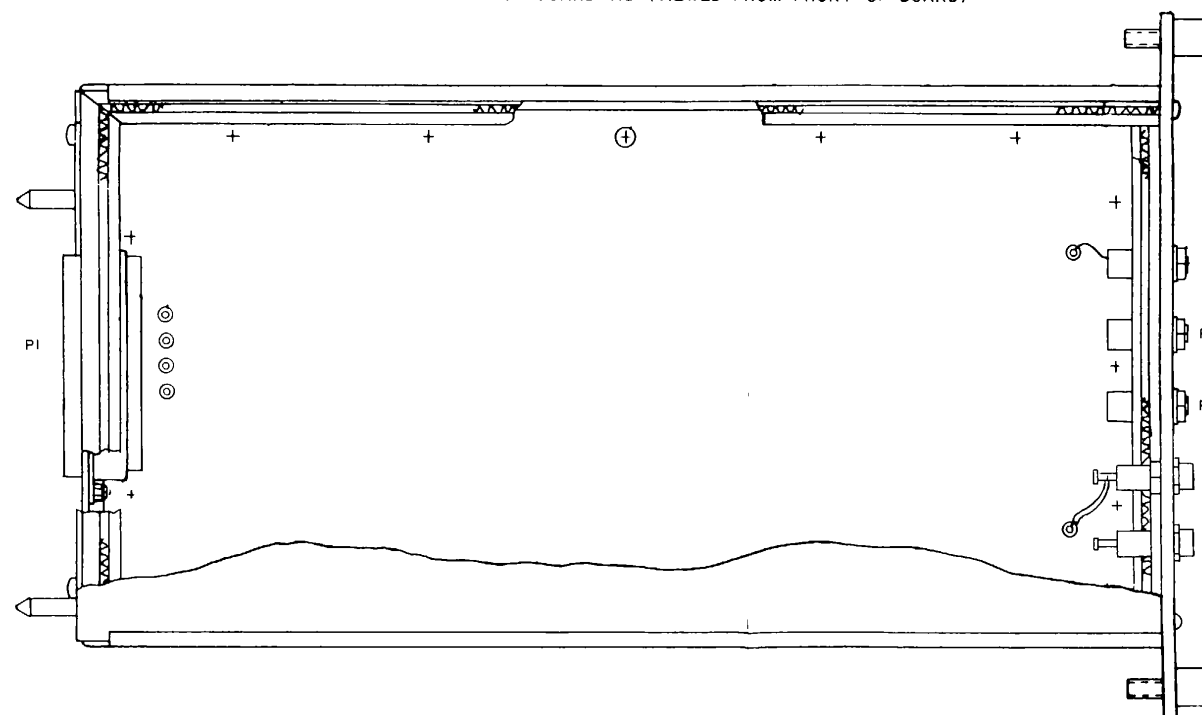
- 1 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION
- 2 ——— INDICATES WIRING ON FRONT OF BOARD  
 - - - - - INDICATES WIRING ON REAR OF BOARD



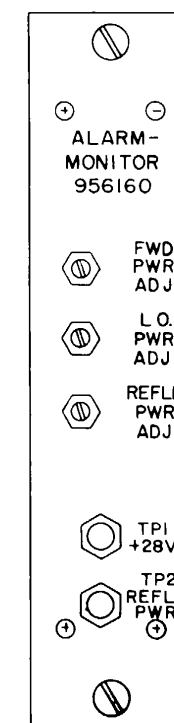
D WIRING ON REAR OF BOARD A8 (VIEWED FROM FRONT OF BOARD)



C PARTS AND WIRING ON FRONT OF BOARD ASSEMBLY



B FRAME AND PANEL ASSEMBLY WITH PARTS



A FRONT VIEW  
EL21B071

Figure 5-108. Alarm monitor 3A1, parts location and printed wiring diagram.

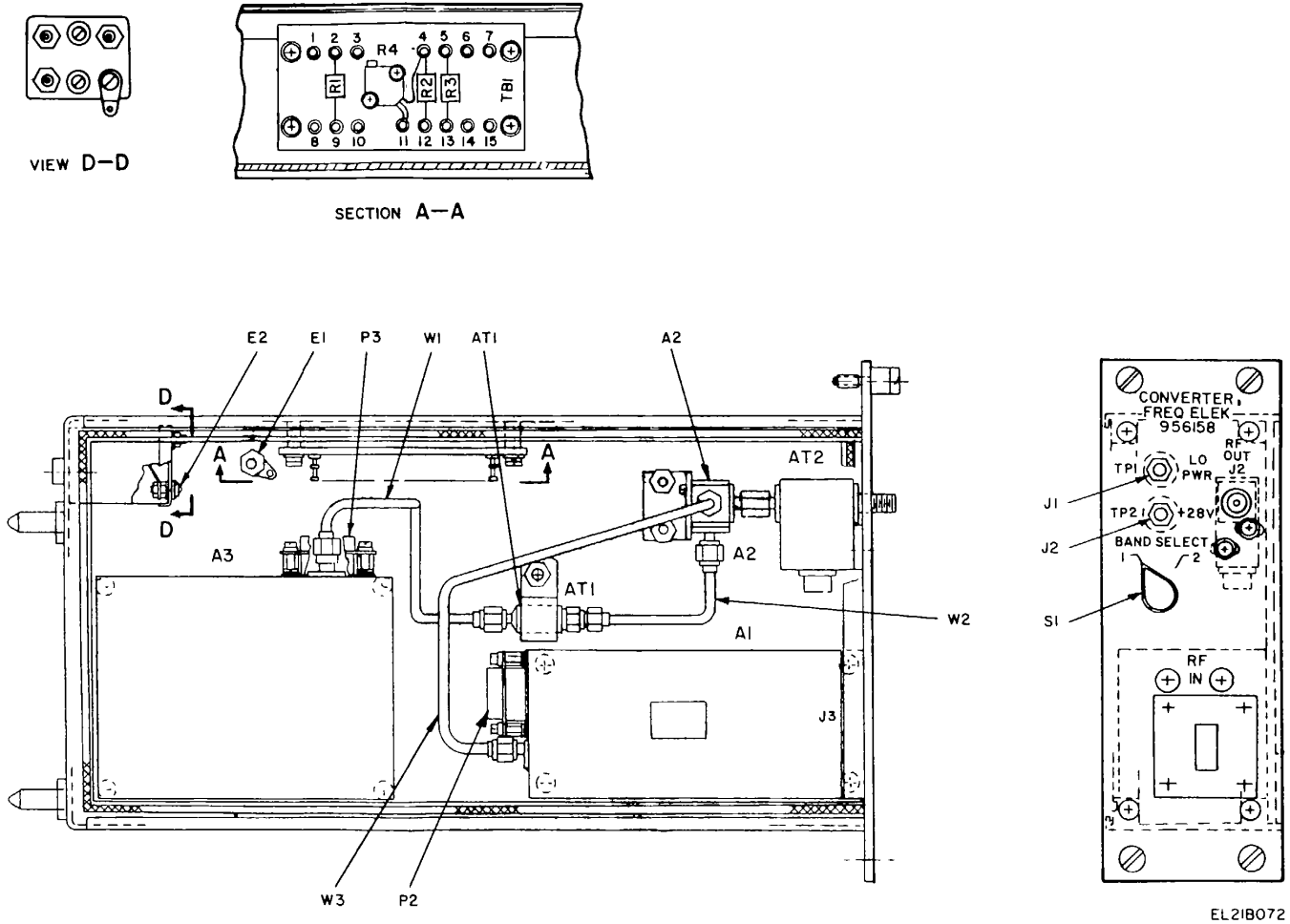
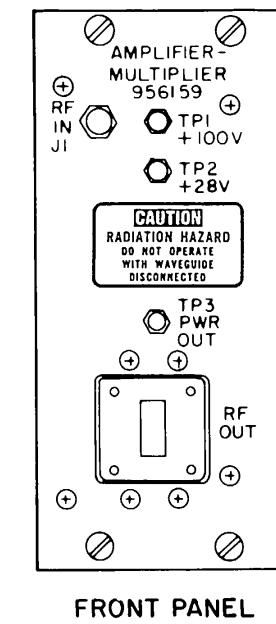
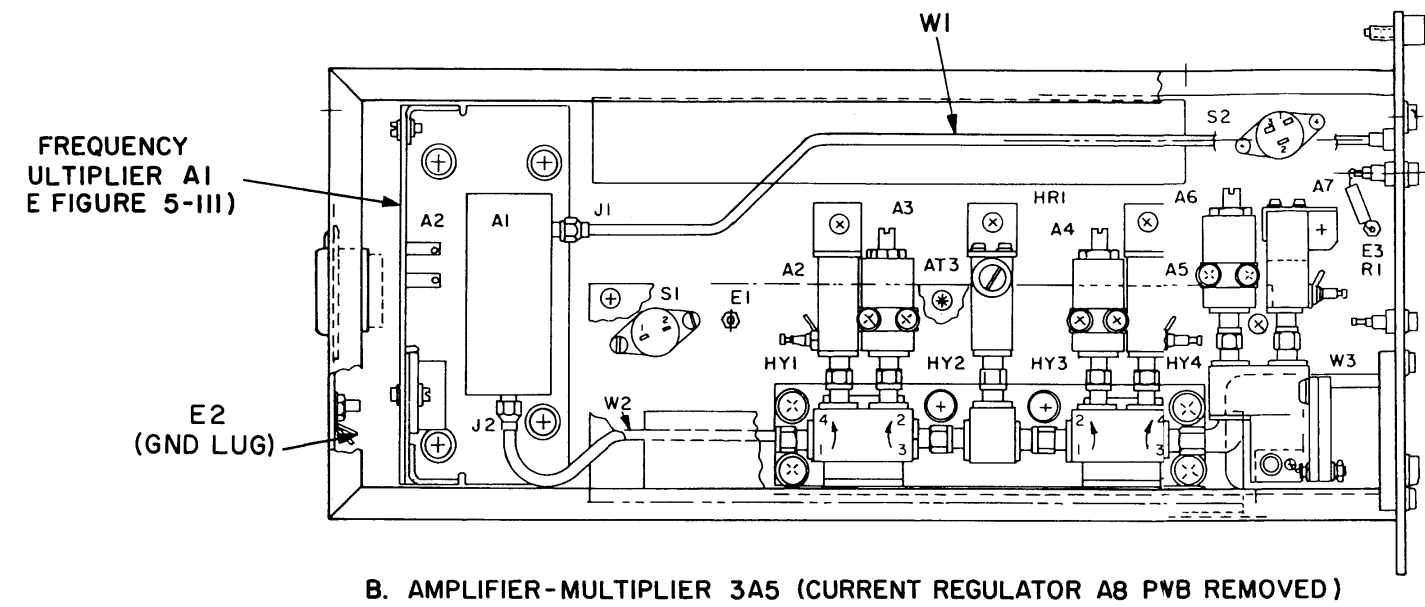


Figure 5-109. Converter-frequency electronic 3A2, parts location diagram.

Change 6 5-245





WIRE LIST

REF. NO	AWG	COLOR	FROM	TO
1	20	GRAY	PI-1	S1-1
2		WHT-GY	PI-2	E1
3		RED	PI-3	A8E1
4		BLACK	PI-4	A8E2
5		W-R-BLU	PI-5	A1E1
6		WHITE	PI-7	S2-3
7		WHITE	PI-8	S2-1
8		WHITE	PI-9	A8E7
9		BLACK	PI-10	E2(GND LUG)
10		BLACK	PI-11	E2(GND LUG)
11		P/OHRI	HR-1	E1
12		P/OHRI	HR-1	S1-2
13		WHITE	A8E3	A2E1
14		WHITE	A8E4	A5E1
15		WHITE	A8E5	A7E1
16		WHITE	A8E6	J2
17		WHITE	A8E8	HY4-DET OUT
18		WHITE	A8E9	J4
19	20	BLACK	HY4-GND	E2(GND LUG)
20	20	BLACK	A8E2	E2(GND LUG)
21	20	BLACK	PI-6	E2(GND LUG)
22	20	BLACK	A1E2	E2(GND LUG)
23	20	W-R-BLU	A1E1	E3
24	20	W-R-BLU	E3	S2-2

NOTE:  
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION

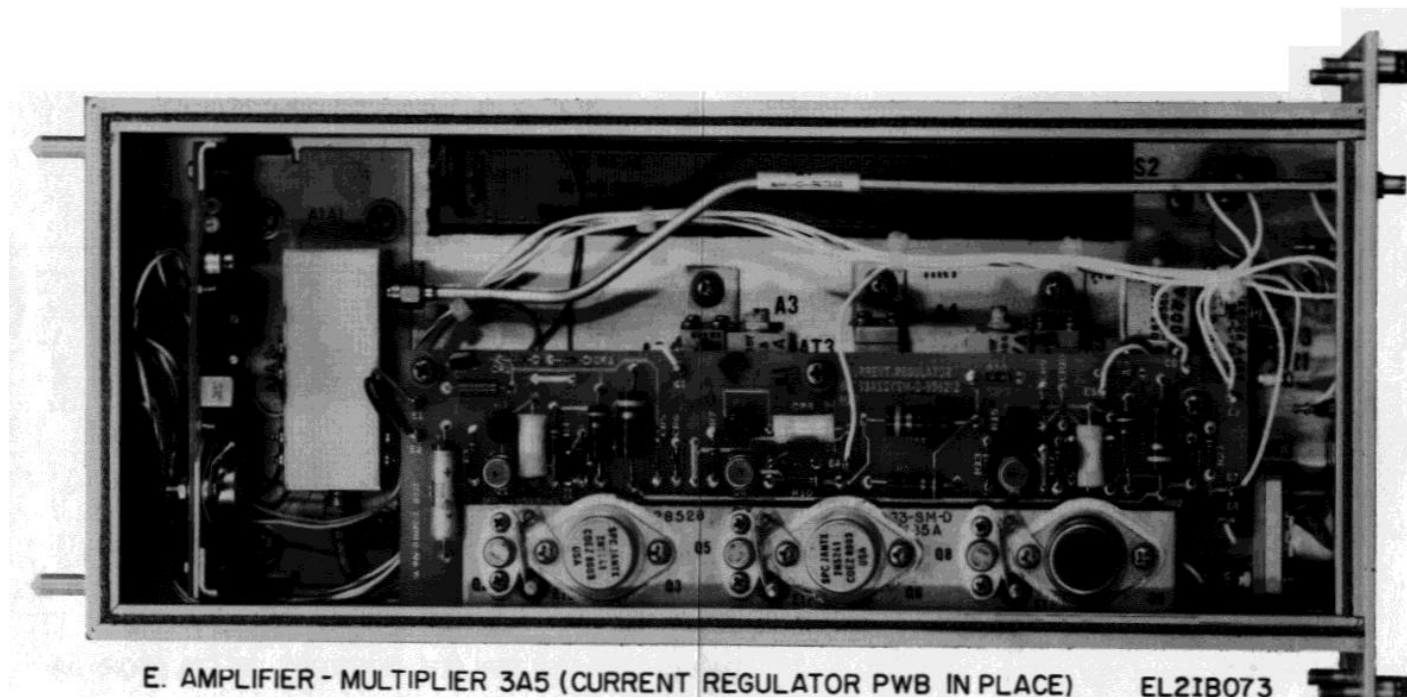
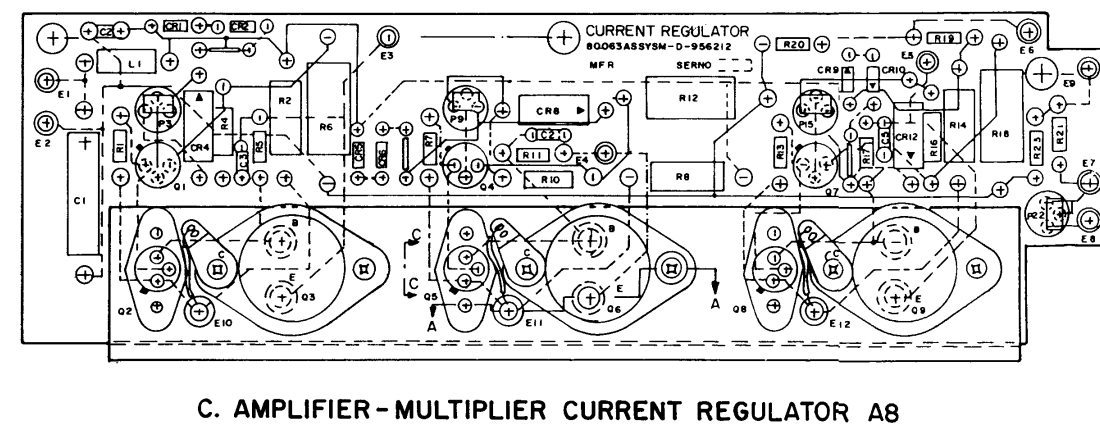
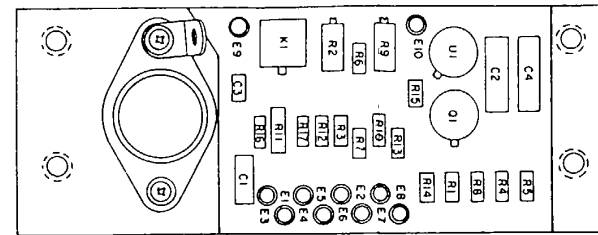
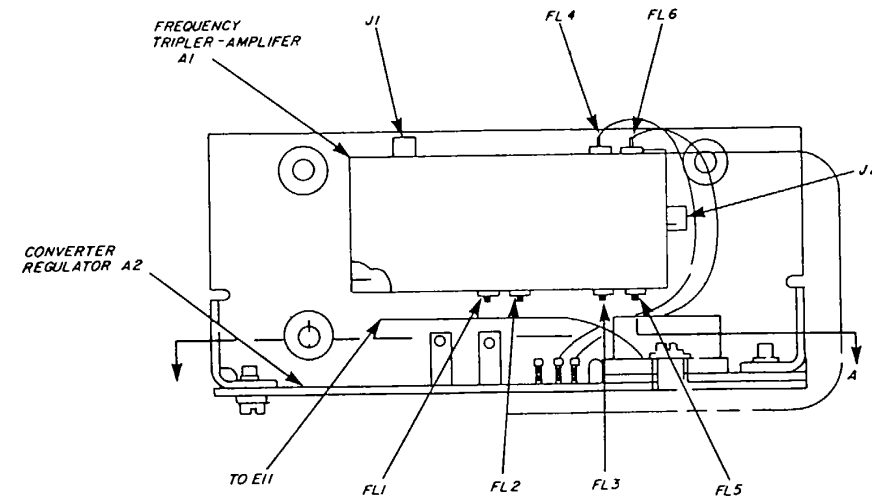


Figure 5-110. Amplifier multiplier 3A5, parts location diagram



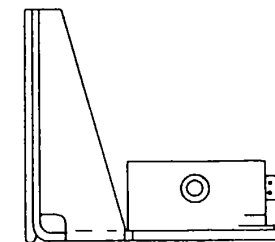
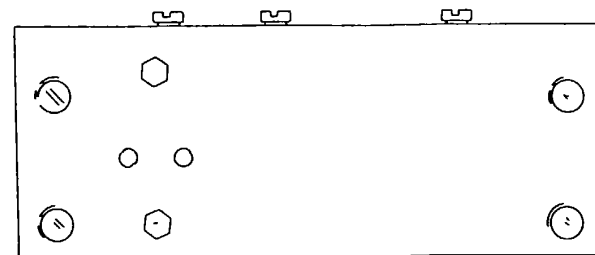
NOTE:

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION



WIRE LIST

REF NO	AWG	COLOR	FROM	TO
1	24	RED	A2E3	A1 FL2
2	24	ORN	A2E4	A1 FL4
3	24	WHT RED	A2E5	A1 FL6
4	24	GRN	A2E6	A1 FL5
5	24	BLU	A2E7	A1 FL3
6	24	WHT/BLU	A2E8	A1 FL1
7	24	BLK	A2E2	A1 E1
8	24	RED	A2E11	VRI-LUG



EL2IB153

Figure 5-11. Frequency multiplier 3A5A1, parts location diagram

Change 6 5-249

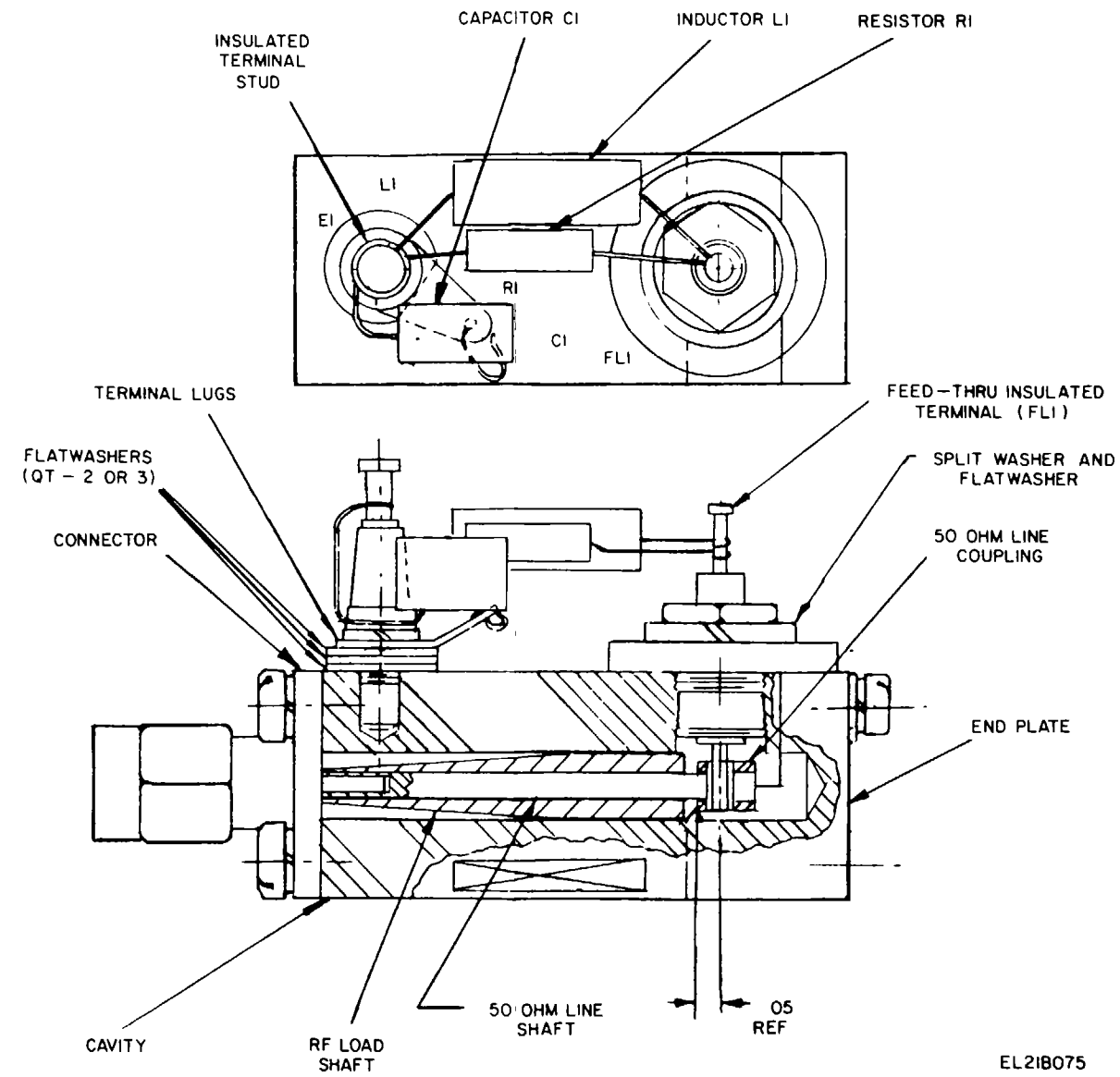


Figure 5-112. Bias "T" cavity assembly 3A5A2, 3A5A5 and 3A5A7, parts location diagram.  
Change 6 5-251

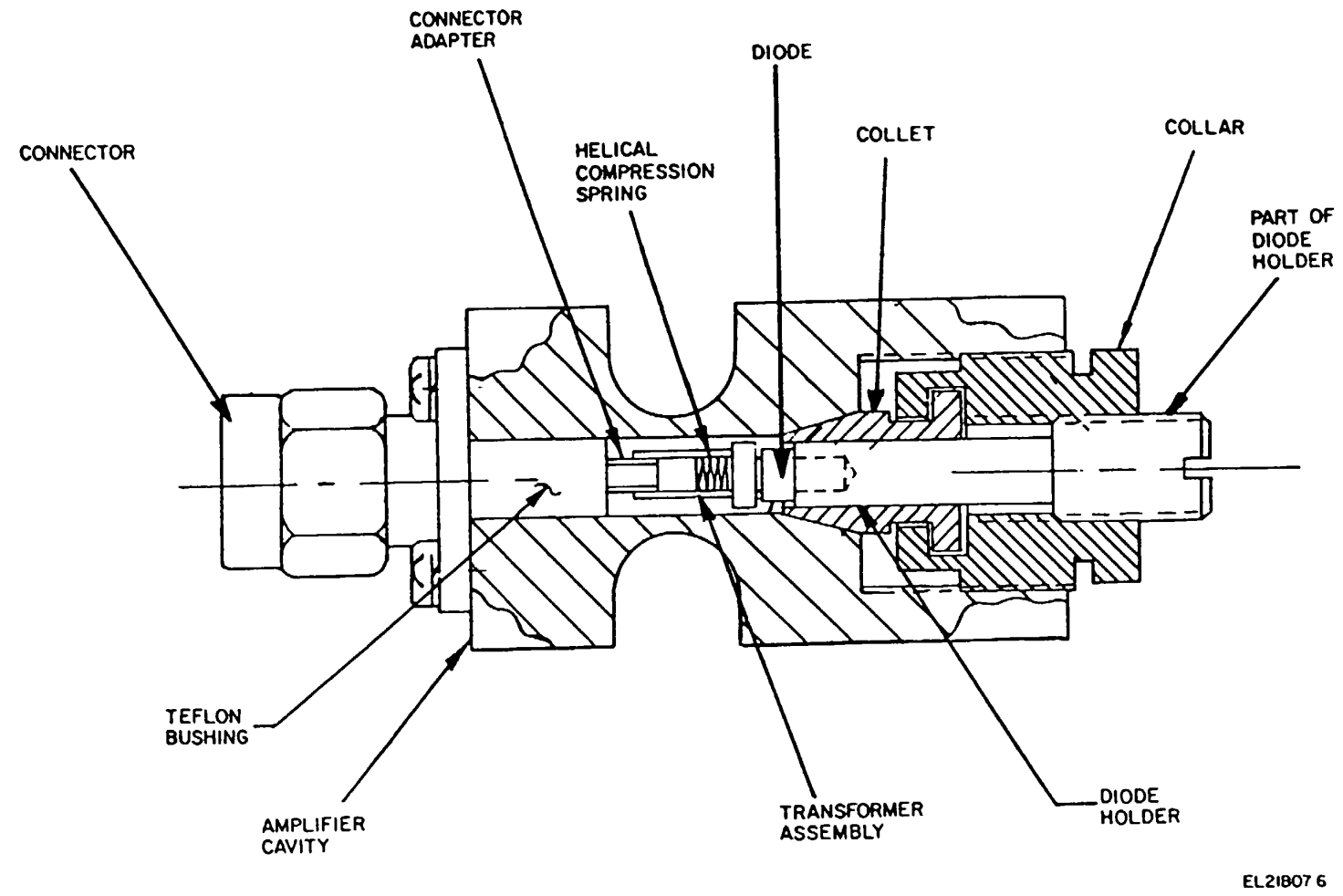
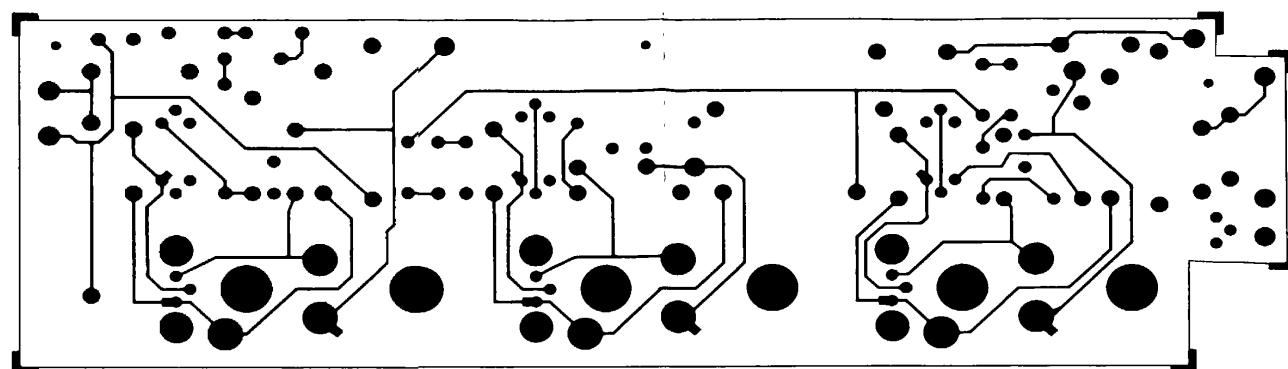
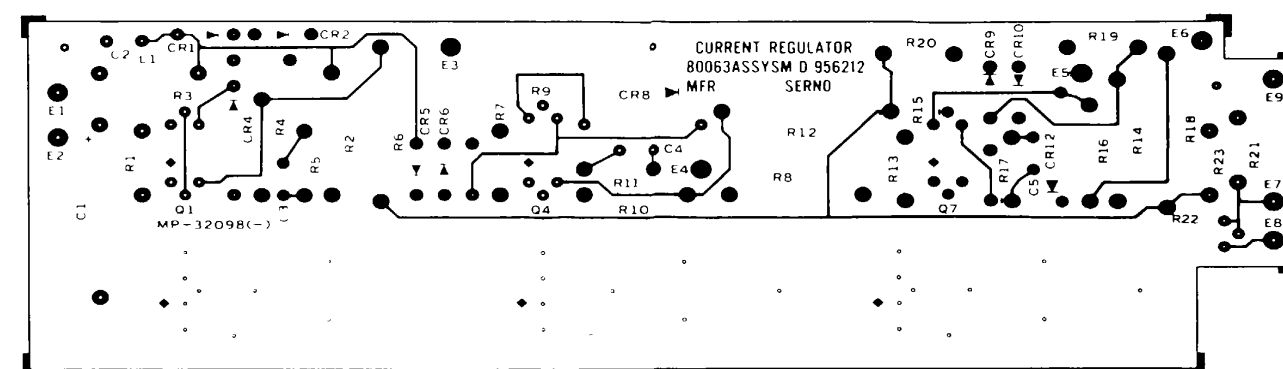


Figure 5-113. Impatt amplifier 3A5A3, 3A5A4 and 3A5A6, parts location  
Change 6 5-253



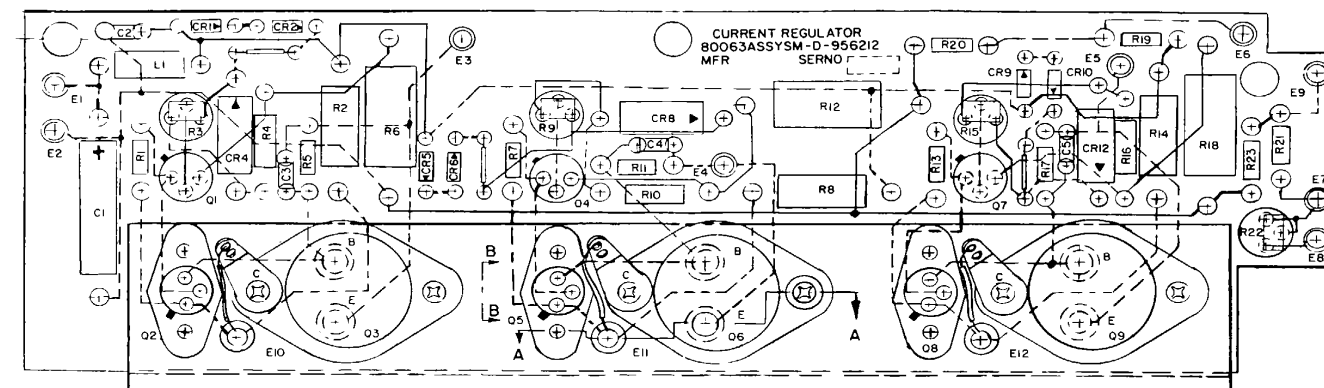
D WIRING ON REAR OF BOARD A8 (VIEWED FROM FRONT OF BOARD)



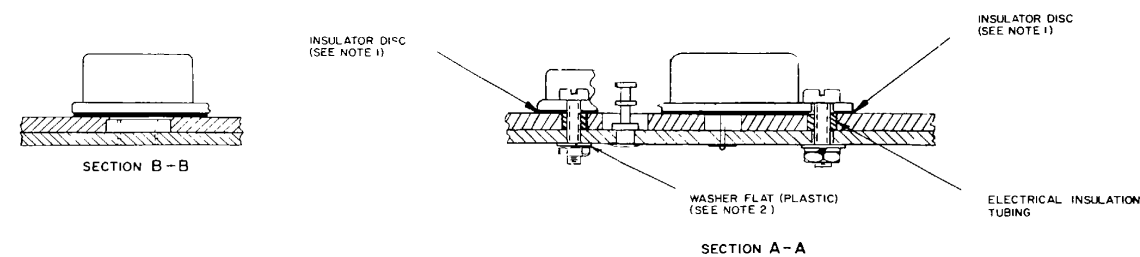
C WIRING ON FRONT OF BOARD A8 (VIEWED FROM REAR OF BOARD)

NOTES

- 1 APPLY A SMALL AMOUNT OF SILICONE COMPOUND TO BOTH SIDES OF INSULATOR DISC
- 2 APPLY A SMALL AMOUNT OF SEALING COMPOUND TO THREADS BEFORE TIGHTING
- 3 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION
- 4 ——— INDICATES WIRING ON FRONT OF BOARD  
 - - - - - INDICATES WIRING ON REAR OF BOARD



A REFERENCE DESIGNATIONS AND COMPONENTS OF BOARD A8 (956212)



B SECTIONAL VIEWS

EL2IB121

Figure 5-114. Current 3A5A8, parts and location and printed wiring diagram.

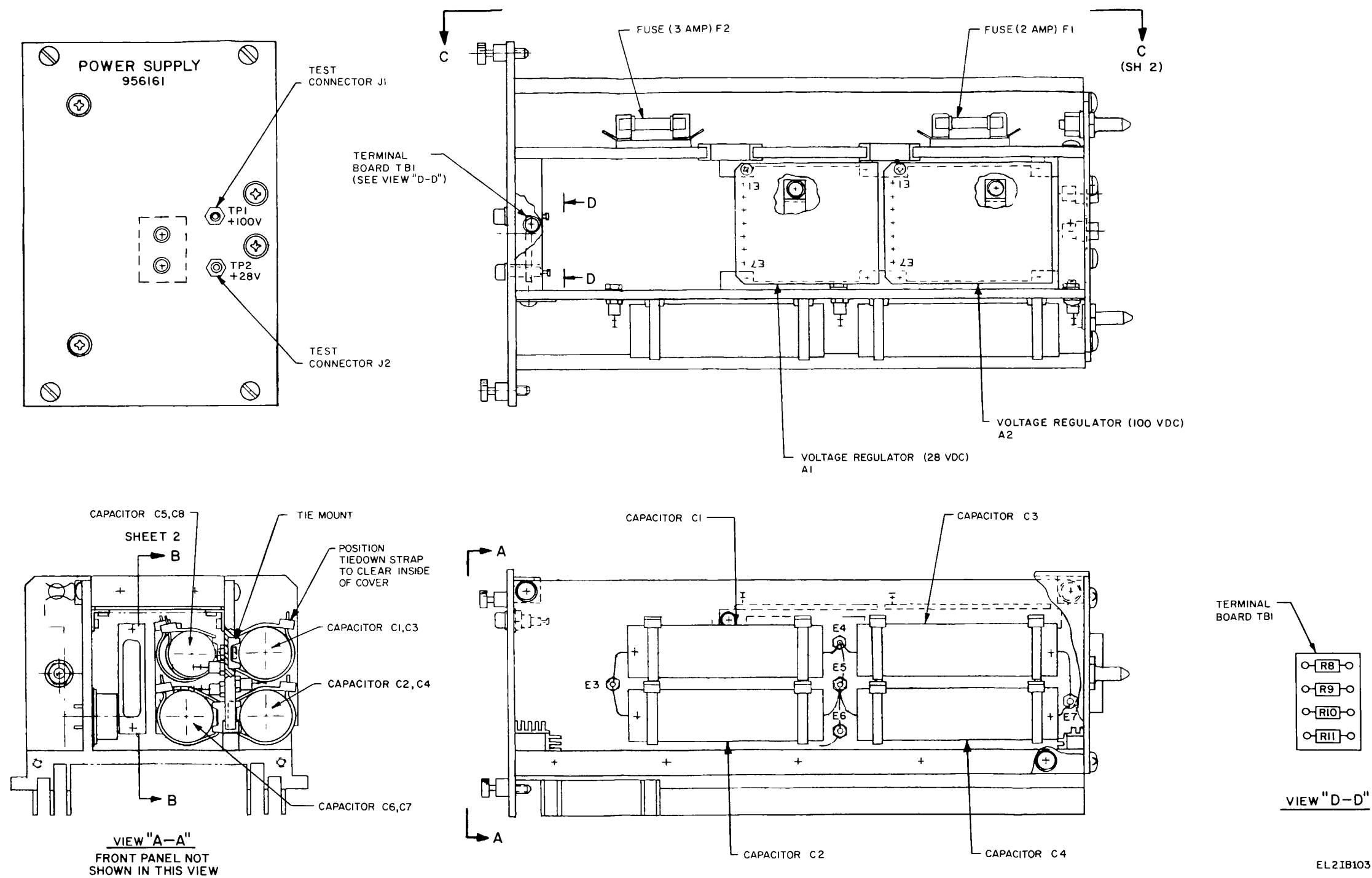
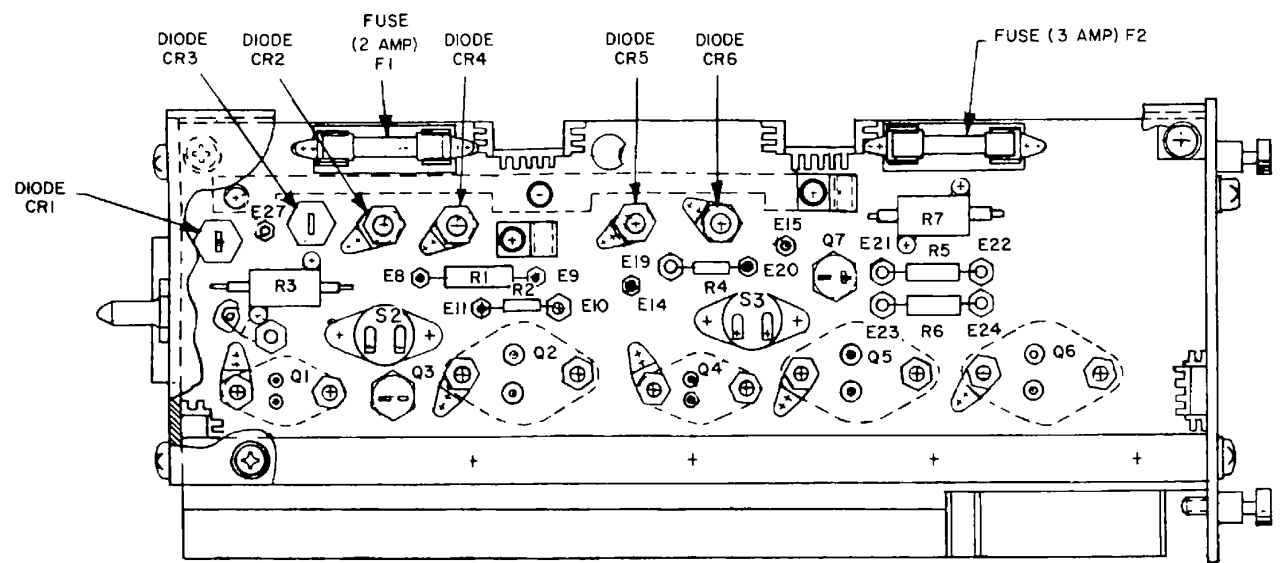
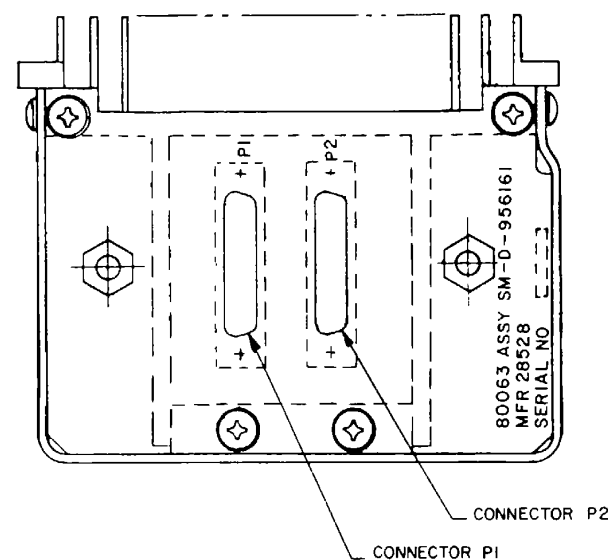


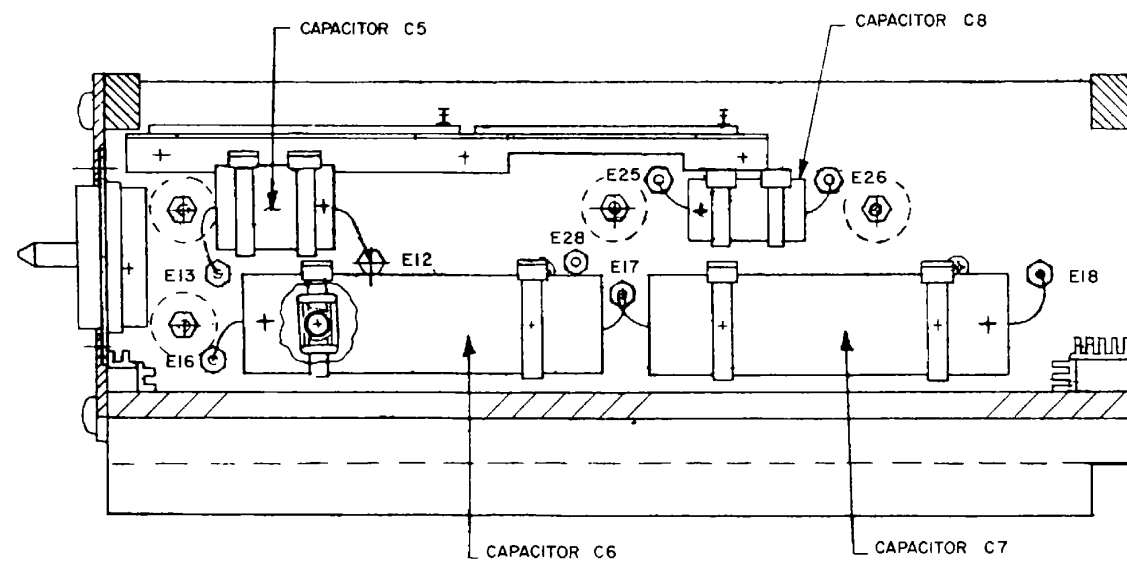
Figure 5-115 (1). Power supply 3A6, parts location diagram (sheet 1 of 2).



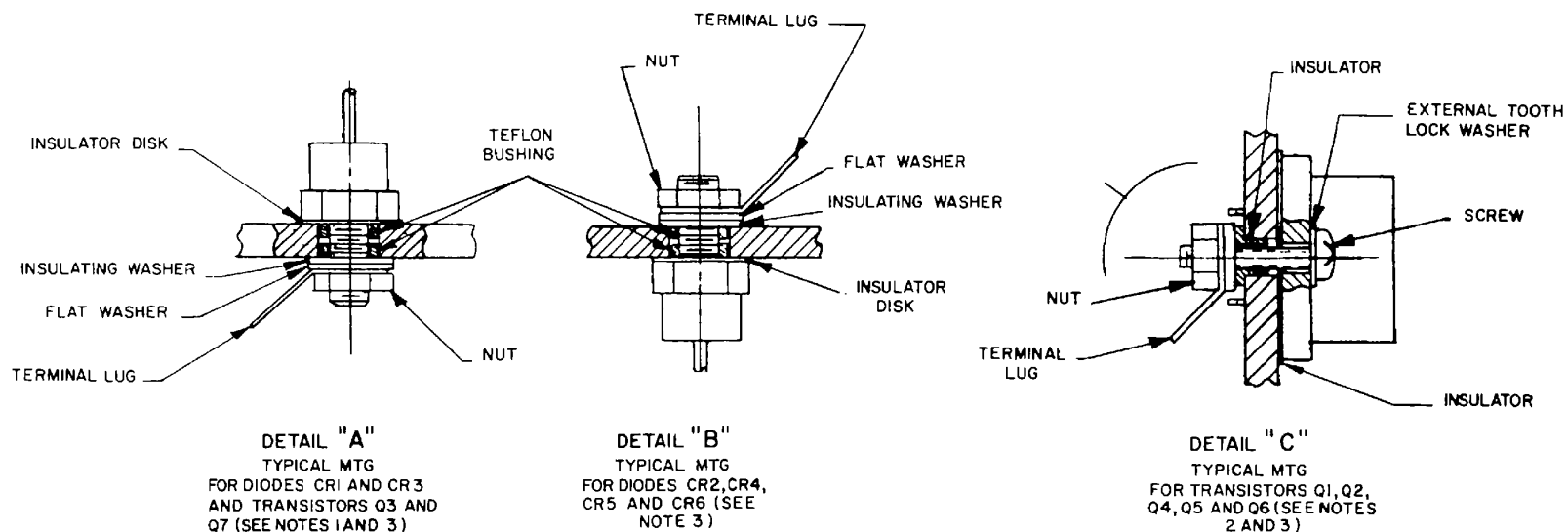
VIEW "C-C" ROTATED 180° FOR CLARITY



- NOTES
- 1 DISCARD HARDWARE SUPPLIED WITH Q7 AND Q3
  - 2 DISCARD MICA INSULATOR SUPPLIED WITH Q1 AND Q4
  - 3 ADD COATING OF SILICONE COMPOUND TO BOTH SIDES OF INSULATOR DISK WHEN REPLACING DIODES OR TRANSISTORS
  - 4 PARTIAL REFERENCE DESIGNATION ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION

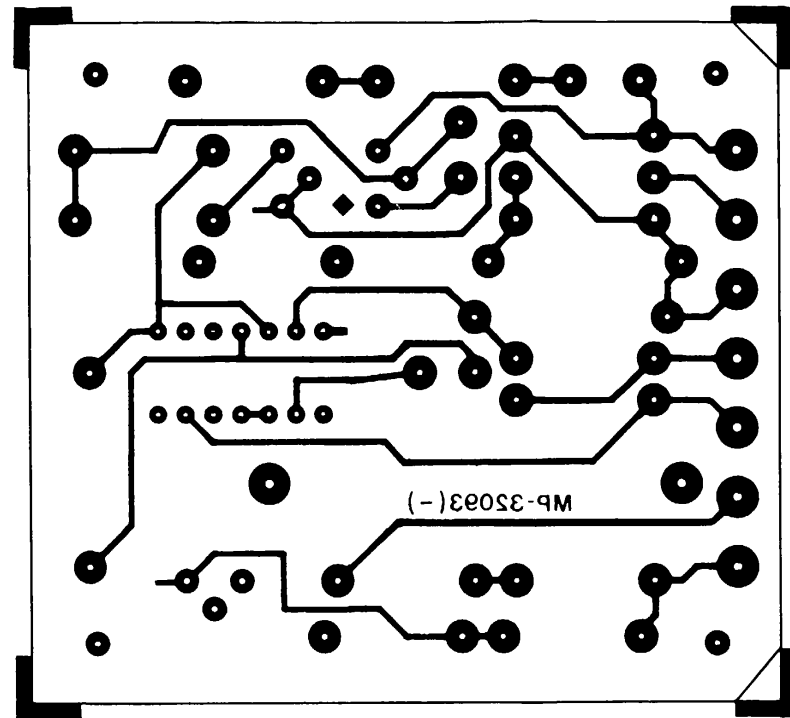


SECTION "B-B"

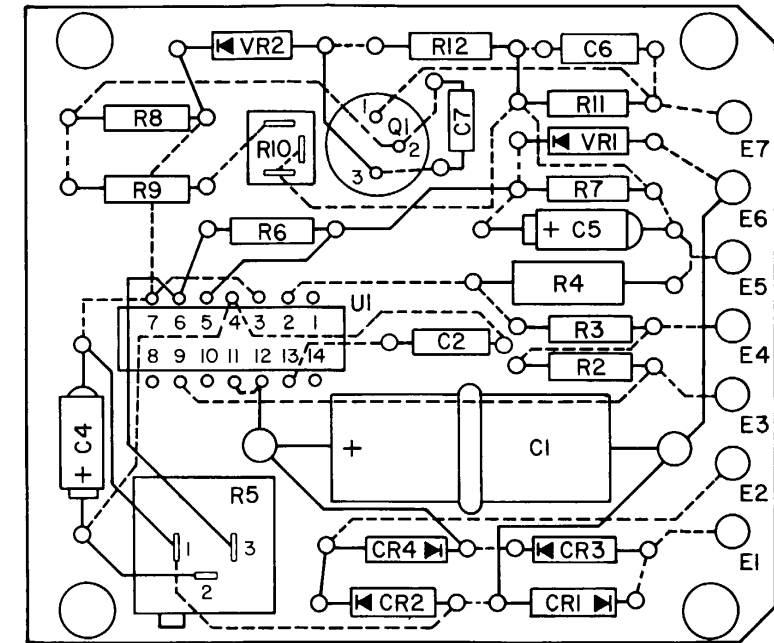


EL2IB104

Figure 5-115 (2). Power supply 3A6, parts location diagram (Sheet 2 of 2).



B. WIRING ON REAR OF BOARD A1 (VIEWED FROM FRONT)



A. COMPONENTS AND WIRING OF BOARD A1 (956189)

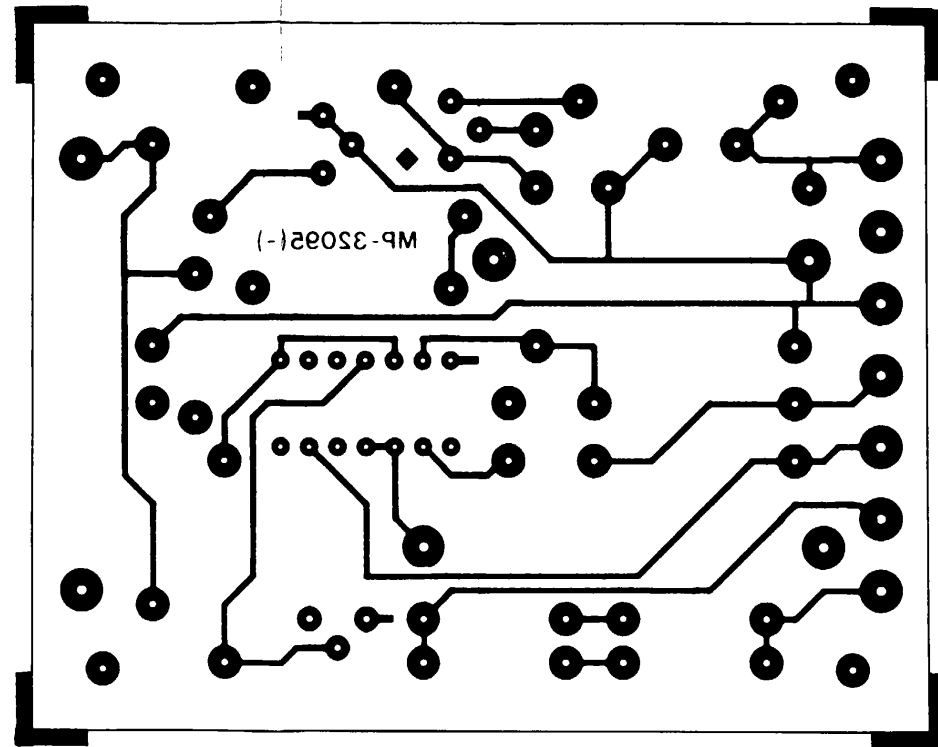
EL 21B082

NOTES:

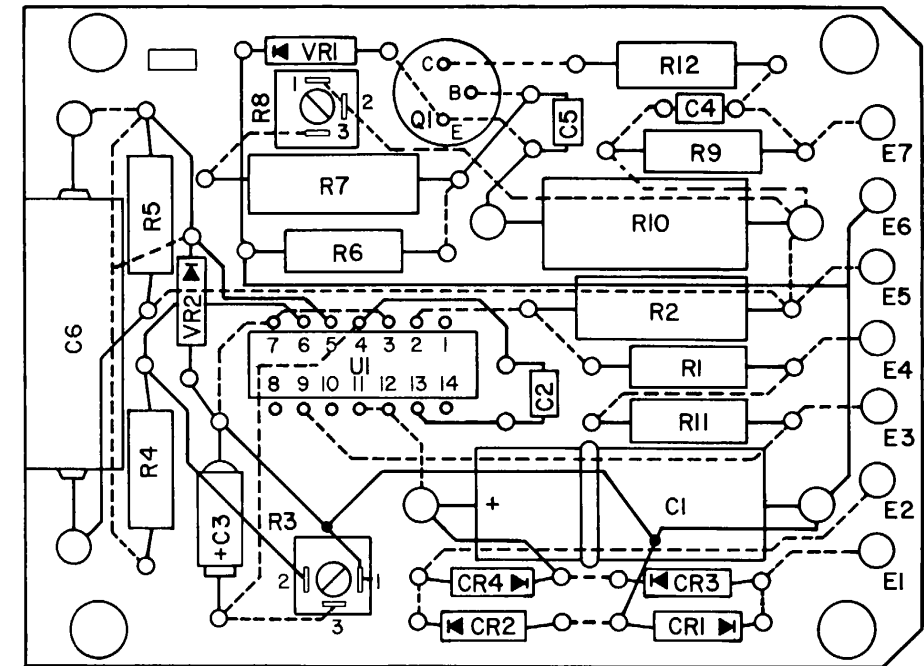
1. PARTIAL REFERENCE DESIGNATION ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.
2. ——— INDICATES WIRING ON FRONT OF BOARD  
 - - - - - INDICATES WIRING ON REAR OF BOARD

Figure 5-116. Printed wiring board, voltage regulator (28 VDC) 3A6A1 parts location and printed wiring diagram.





B. WIRING ON REAR OF BOARD A2  
(VIEWED FROM FRONT)



A. PARTS AND WIRING OF BOARD A2 (956192)

EL2IB083

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.
2. ——— INDICATES WIRING ON FRONT OF BOARD  
----- INDICATES WIRING ON REAR OF BOARD

Figure 5-117. Printed wiring board, voltage regulator (100 VDC) 3A6A2, parts location and printed wiring diagram.

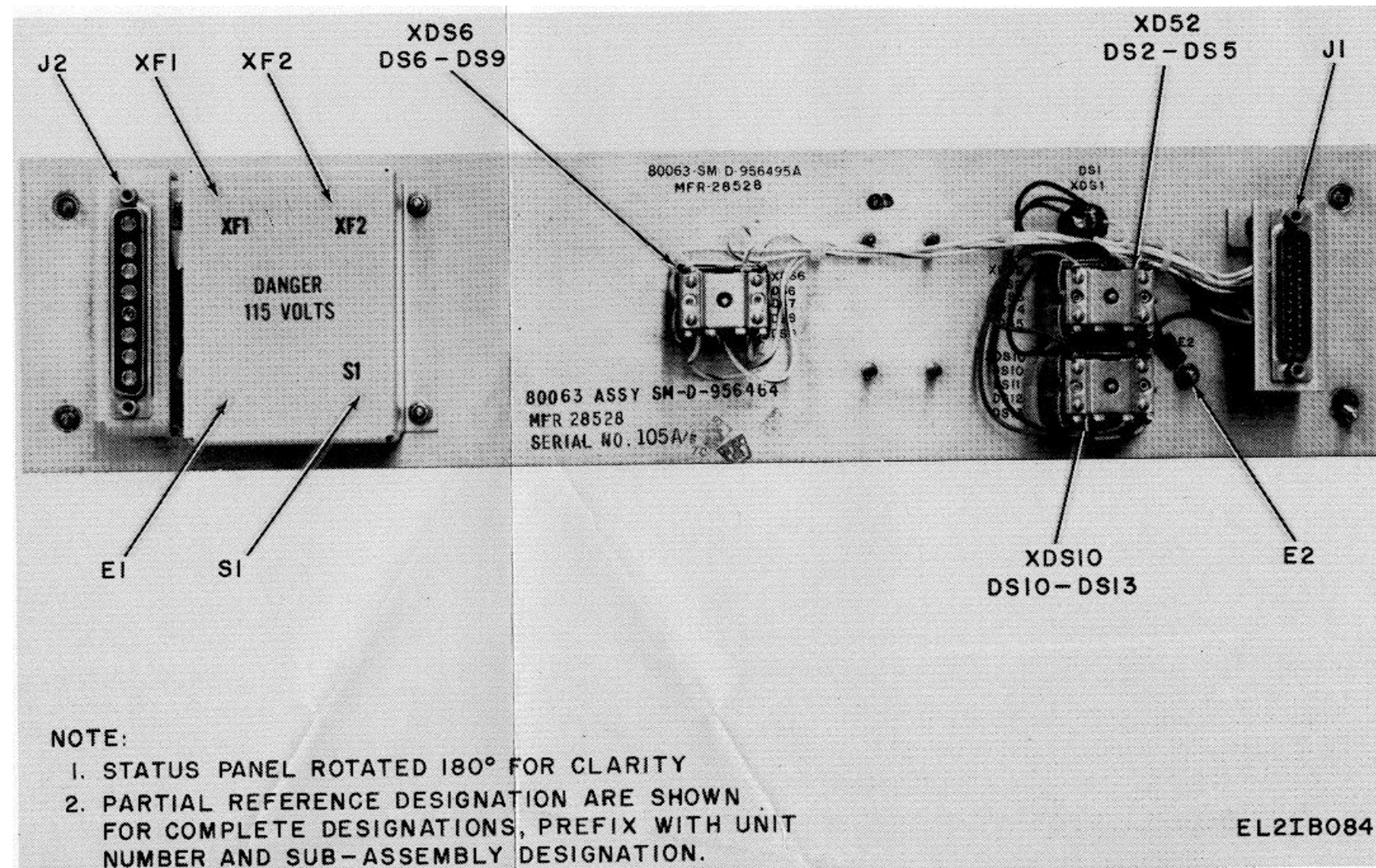
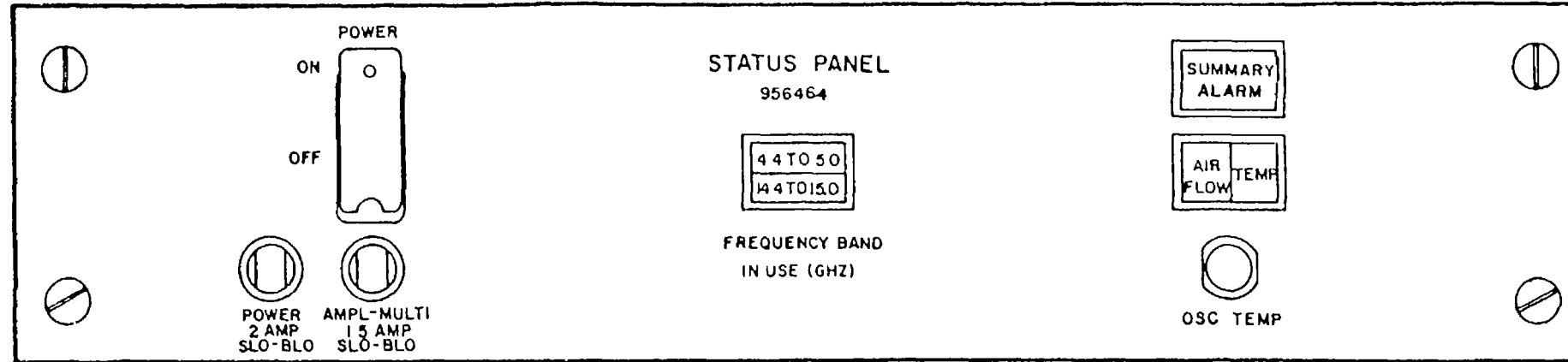


Figure 5-118. Status panel 3A8, parts location diagram..

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